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DIRECT SUPPORT AND GENERAL SUPPORT
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FOR

SATELLITE COMMUNICATION TERMINAL AN/TSC-54
(DETAILED CIRCUIT ANALYSIS)
(NSN 5895-00-937-4993)

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TM 11-5895-389-34-2/NAVELEX 0967-LP-377-7021/TO 31R5-2TSC54-22-2, 5 January 1978 is changed as follows:

1. A vertical bar appears opposite changed material.
2. Remove and insert pages as indicated in the page list below:

Remove	*Insert*
i through v	i through v
3-21 and 3-22	3-21 through 3-22.3
3-119 through 3-124	3-119 through 3-124.1
Figure FO 3-10	Figure FO 3-10
None	Figure FO 3-10.1
Figure FO 3-11 (*sheets 1 and 2*)	Figure FO 3-11
Figure FO 3-54	Figure FO 3-54

3. File this change sheet in the front of the manual for reference purposes.

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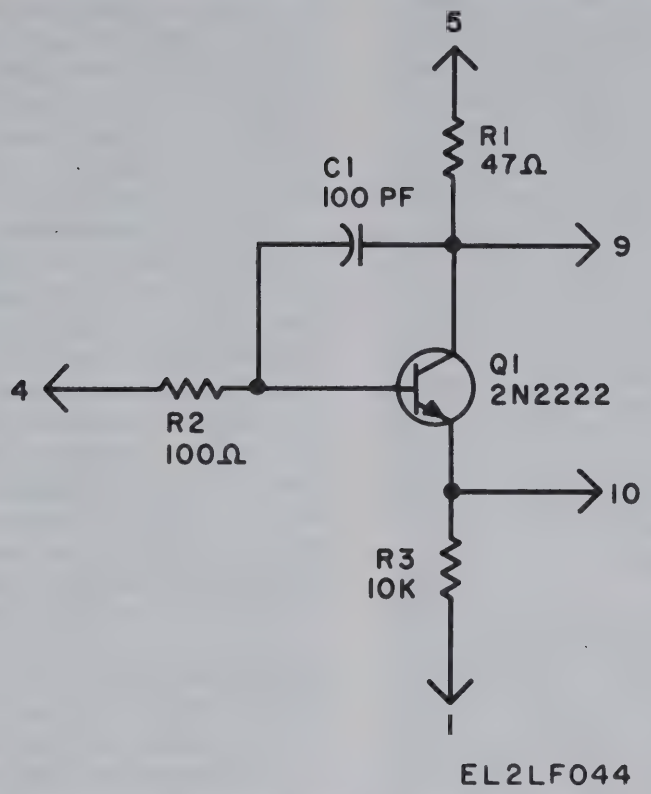

Figure 3-23. Impedance amplifier 1A2A5A24A45, schematic diagram.

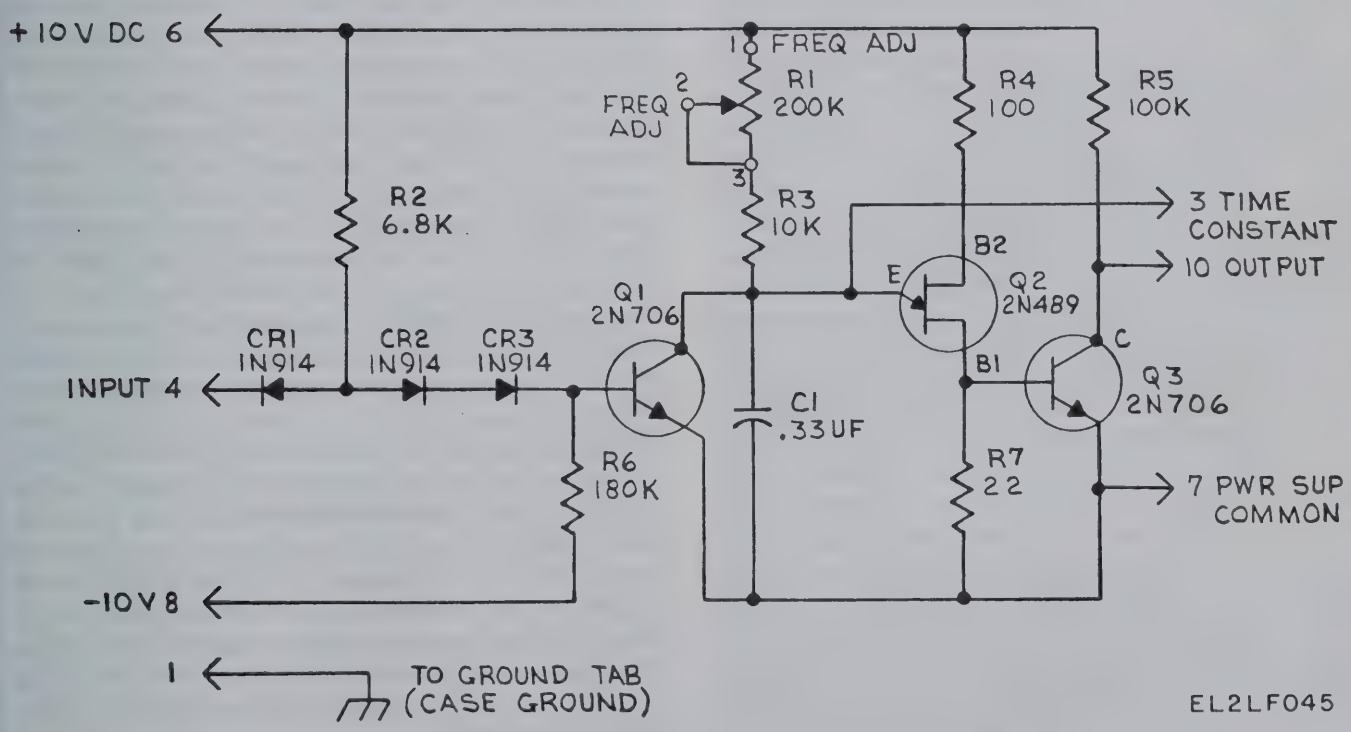

Figure 3-24. Variable time delay 1A2A5A24A47, schematic diagram.

3-13. Rf Power Monitor and Control 1A2A27 Circuit Analysis

(figs. FO 3-10, FO 3-10.1 and FO 3-54)

a. The following subparagraphs describe the rf power monitor and control circuits of the common power meter circuits, including on-line transmitter output power assembly 1A2A27A4.

b. Rf transmission line switch 2A3S2 (fig. FO 3-54) permits selection of either the LPA or HPA for monitoring by on-line transmitter output

power assembly 1A2A27A4. Switch 2A3S2 selects the attenuated rf output from HPA directional couplet 2A3DC6 (50 dB) or LPA directional coupler 2A3DC100 (40 dB). Each directional coupler rf output is routed through a variable attenuator (2A3A10AT18 for HPA, 2A3AT100 for LPA) to the rf transmission line switch 2A3S2. The selected rf signal is then routed to rf transmission line switch 2A3A10S5. Control of switch 2A3S2 is by a +28 vdc input from the LPA routed to on-line transmitter output power assembly 1A2A27A4 (fig. 3-10.1). The command (which is present only when the LPA is on line) is routed through normally closed contacts of HPA OFF LINE-METER ZERO switch 1A2A27A4S2 to rf transmission line switch 2A3S2 (fig. FO 3-54). With LPA on line, the rf is routed from the No. 2 input to the IN port of switch 2A3S2 to switch 2A3A10S5.

c. Switch 2A3A10S5 provides a meter zeroing attenuation for on-line transmitter output power assembly 1A2A27A4 meter/relay M1 (fig. 3-10.1). When switch 1A2A27A4S2 is held in the METER ZERO position, +28 vdc (at 1A2A27A4J4—pin J, to 1A2A27A4S2 5-4 contacts) is sent to switch 2A3A10S5 (fig. FO 3-54), disconnecting the selected rf monitoring sample from switch 2A3S2 and terminating the rf power head input with 2A3A10AT22. METER ZERO potentiometer 1A2A27A4R1 can then be used to zero the meter; R1 is connected to 40 dB autorange power meter amplifier 2A3A10A18 as an external zeroing drive. If switch 1A2A27A4S2 is not pressed, the rf from switch 2A3S2 is routed through the J1-J3 connectors to rf transmission line switch 2A2A10S2. Switch 2A3S2 and switch 2A3A10S2 are rf transmission line switches. Switch 2A3S2 contains a relay that connects the 1-IN ports together (when deenergized) or the IN-2 ports together (when energized). The METER ZERO position of switch 1A2A27A4S2 energizes the relay to connect the appropriate ports. Switch 2A3A10S2 has a double wound solenoid that connects the J1-J2 and J3-J4 ports (switch position 1) or the J1-J4 and J2-J3 ports (switch position 2). Each half of the solenoid is separately energized by 28 vdc which is applied by a switch; one solenoid input sets up position 1 and the other sets up position 2.

d. Switch 2A3A10S2 (fig. FO 3-54) is controlled by RANGE switch S1 in on-line transmitter output power assembly 1A2A27A4 (fig. 3-10.1). RANGE switch S1 performs two functions: Control of rf switch 2A3A10S2 and dc power application to range indicators of the on-line transmitter. When RANGE switch S1 is set to the upper position, a pad bypass command is sent to rf transmission line switch 2A3A10S2, connecting the 1-4 ports and 2-3 ports. In this configuration the rf level from switch 2A3A10S5 is routed through switch 2A3A10S2 to rf power head 2A3A10A22. If RANGE switch 1A2A27A4S1 is set to the lower position, ports 1-2 and 3-4 of rf switch 2A3A10S2 are connected together, putting attenuator 2A3A10AT3 (5 dB) into the line ahead of the rf power head and isolator 2A3A10CP14.

e. RF power head 2A3A10A22 (fig. 3-54) provides 40 dB autorange meter amplifier 2A3A10A18 with dc levels related to average power absorbed by the head. Refer to paragraph 3-13.1 for detailed analysis of amplifier 2A3A10A18.

f. RF power monitor and control panel 1A2A27 (fig. FO 3-10) provides a means of continuously monitoring transmitter forward power output from 10 W to 10 kW (10μW to 10 mW full scale). The rf power meter on this panel allows the operator to set the transmitter power, at any frequency, to within 0.2 dB over the power range of 10 W to 10 kW for the HPA, or 1 W to 3 kW for the LPA.

g. On-line transmitter output power assembly 1A2A27A4 (fig. FO 3-10.1) allows the operator to set the high and low power automatic alarm points to within 0.5 db of the power meter reading. Alarm DS1 is triggered by the level setting through relay contacts of meter/relay assembly M1. The meter relay assembly is powered by 120 vac and controlled by the detected rf level at 40 dB autorange power meter amplifier A2A3A10A18. Threshold levels set by upper and lower level trip point adjustments on the meter face establish the point at which the relay of the meter/relay assembly will be energized. When energized (rf level being transmitted has exceeded or fallen below the preset level), the parallel-connected relay contacts close, and +28 vdc is connected through the 5-6 contacts of switch 1A2A27A4S2 (in its center position to the alarm). Four indicator ranges are provided to indicate the range level of the signal from 40 dB autorange meter amplifier 2A3A10A18. These ranges (+10, 0, -10, and -20 dBm) are displayed on indicator assemblies A1-A5 according to the status of relay K4 (energized when the LPA 2A11 is on-line; deenergized when HPA is on-line). Each indicator assembly contains two sets of lamps. Selection of the particular lamp set (top or bottom) is by RANGE switch S1 setting; high range (upper lamp set) or low range (lower lamp set). Power for the lamps (15 vdc) is provided from 40 dB autorange power meter amplifier through RANGE switch S1.

3-13.1. 40 dB Autorange Meter Amplifier 2A3A10A18 Circuit Analysis

(fig. FO 3-11)

a. The selected output from rf power head 2A3A10A22 is applied to 40 dB autoranging meter

amplifier 2A3A10A18. The dc input signal from the power head is applied to modulator G1-A (fig. 3-11). The square wave output signal of the modulator is stepped-up by input transformer T1 and applied to low-noise preamplifier Q1-AR2. The square wave signal is amplified in this circuit and coupled to filter amplifier AR3, where much of the noise and other spurious signals are filtered out. The resulting sine wave signal is then amplified and coupled to phase splitter Q2, Q3. This circuit provides the phase splitting action required to provide the demodulator input. The full wave demodulator (G1-B), which is synchronously driven with the modulator, recovers the input dc signal at a greatly amplified level.

b. The output of the demodulator is applied to integrating amplifier AR4, Q4. This circuit provides additional signal gain, and also reduces the amplifier bandwidth to the degree required consistent with the selected response time (and noise level). The amplifier stage feedback capacitor determines the bandwidth of the dc amplifier and is controlled by the setting of RESPONSE switch S2. When in the NORM position, the response time of the power meter is less than 1 second and the noise is less than ±1 percent p-p of full scale on the most sensitive range. When in the FAST position, the response time decreases to approximately 100 milliseconds, but the noise increases particularly on the low ranges. The output of the integrating amplifier is coupled back to the modulator and input transformer circuit through the switch network. This feedback provides a high degree of degeneration and, thus, gain stability, and at the same time provides a means of accurate control of the overall amplifier gain.

c. The output of the integrating amplifier is also applied to the compensation network in the power head, where compensation is made for the sensitivity of the power head and for its inefficiency at the frequency of the signal under measurement. The return from the power head compensation network is applied to inverting amplifier AR1, and the output of this circuit drives meter M1 of on-line transmitter output assembly 1A2A27A4 through a second range switching network.

d. Autoranging is accomplished by the components shown in the COMPARATOR AND TRIGGER PULSE LOGIC and POWER SUPPLY/ COUNTER-DECODER areas of figure FO 3-11. Integrated circuit A101 and associated components comprise a double-ended limit detector network (comparator) which provides a nominal 3-volt output level (high) when the analog input signal is less than 0.45 volt or more than 5 volts, and a nominal 0-volt output level (low) when the analog input signal is between these two limits. The lower limit value is determined by divider R107 and R108 and the positive power supply level, while the upper limit is determined by divider R103 and R104 and the positive power supply level. The comparator network output is inverted in A105 and applied to the base of common emitter amplifier Q103. If the comparator output is a low level, Q103 output is saturated at a dc level near zero, keeping capacitor C106 discharged and inhibiting range changes.

e. The range switching rate network (Q104, R114, C106) functions as a relaxation oscillator to provide trigger pulses to a two-stage binary up-down counter for the duration that comparator A101 is in the logic high state, if capacitor C106 is not clamped (*c* above). The time constant of this network is approximately 300 μsec, which allows up to three range changes each second, if necessary.

f. Range switching is inhibited in one of the following three ways. First, when Q103 is in clamp (saturated) due to a *low* comparator output (which indicated an *in-range* condition); second, when the unit is in the most sensitive range and the analog input signal remains below 0.45 volt (power level less than 0.9 mW (*g* below); and third, when the unit is in the least sensitive range and the analog input signal remains above 5-volts (power level more than 10 mW).

g. Counter A104 and associated components comprise the range switching network; stage A is referred to as A104A and stage B is referred to as A104B. Either binary stage will complement (flip) only when a positive-going pulse is applied to the appropriate clock input terminal. Switching occurs only between adjacent ranges, and can occur in either the forward or reverse direction. The following tabulation summarizes the four possible range combinations with 0 corresponding to *low*, *1* corresponding to *high* and *A* and *B* corresponding to the A104 outputs:

A	*B*	*Range*	*Full scale power input*
0	0	1	10 μW
1	0	2	100 μW
0	1	3	1 mW
1	1	4	10 mW

h. NAND gates A103 pins 8 and 6 control the direction of switching. Their outputs are low when both inputs are high, and high under the other three possible combinations. NAND gate A103 pin 3 capacitor C106 when the unit is in range 1 and the analog input signal decreases below 0.45 volt, thereby inhibiting any additional switching. Similarly, NAND gate A103 pins 11 clamps capacitor C106 when the unit is in range 4 and the analog input signal increases above 5 volts.

i. NOR gates A102 decode the output states of A104 and drive range relay driver transistors

Q105-Q108. When switched on, each transistor energizes its corresponding relay (K1-K4), and also outputs a low level RANGE signal that drives range indicators of on-line transmitter output power assembly 1A2A27A4.

j. As an example of typical operation upon initial turn-on, the unit can be in any range. Automatic range switching occurs if required, until the proper range is reached. Assume the unit is in range 2 (A=1, B=0) and the input power level exceeds 100 μW. The analog input signal to A101 will then exceed 5 volts. First, the output of A101 goes high, unclamping Q103, causing C106 to begin to charge through R113 and R114 towards the positive supply voltage. When the peak voltage at Q104 emitter is exceeded, a pulse is generated and clocks the input of A104A through inverter-drivers A105, A104A flips to the logic zero state. During this time, the analog input signal (more than 5 volts) switches Q102 to on, resulting in a low at A103 pin 4 (which inhibits that gate) and a high at A103 pin 10 (which enables that gate). The high/low A104A transition now causes the output of gate A103 pins 3-10 to go high, and A104B flips, thereby changing output B to 1. This condition (A=0, B=1) is equivalent to range 3, and will be decoded by A102, which in turn, will switch Q107 on, energizing K3 and deenergizing K2. Assume that the analog input signal is still above 5 volts. Within approximately 300 milliseconds, another pulse from Q104 is coupled to A104A causing a transition back to logic one. This low/high transition will not result in a positive-going pulse at the clock input of A104B due to the action of gate A103 pins 8-10, and B remains at 1. This condition (A=1, B=1) is decoded as range 4. If the analog input signal continues to remain greater than +5 volts after relay K4 is energized and K3 deenergized, no additional switching will occur since C106 is now clamped by the output gate A103 pins 11-13.

k. Transistor Q101 and associated components comprise a Zener-regulated dc power supply, which provides a regulated +5-volt output for operation of integrated circuits A101 through A104.

3-14. Communications (IF) Patching Panel 1A3A22, Circuit Analysis.

(fig. FO 3-12)

The communications (if.) patching panel functions as an interconnection point for all signals to and from the AN/TSC-54 transmitting and receiving equipment. Figure FO 3-12 is a schematic diagram of the panel. Refer to the functional analysis for the basic operation of the panel.

3-15. Comm Demod 1A3A3 Circuit Analysis.

(figs. 3-25 through 3-45 and FO 3-13 through FO 3-21)

The comm demod of the AN/TSC-54 processes and detects the 70 MHz receive signal from the receiving circuits. It provides an audio output and antenna control signal. The detailed circuit analysis for the comm demod is given in *a* through *x* below.

a. The 70 MHz bandpass filter A1 (fig. 3-25) provides a 4-megahertz bandpass at 70 MHz. It is a 3-pole Butterworth configuration and has a vswr of less than 1.2 to 1 across the frequency band. Tuning is provided by variable capacitors C3, C6 and C8. Capacitors C1 and C10 are the variable elements of the impedance matching network used at the output and the input.

b. The 70 MHz to 21.4 MHz balanced mixer A2 as illustrated in figure 3-26, consists of two amplifier transmitters, Q1 and Q2, and a balanced mixer consisting of diodes CR1A and CR1B and transformer T1. The 48.6 MHz local oscillator signal is applied across resistor R1, which provides an input impedance match, and is coupled by capacitor C2 to the base of transistor Q1. Bias for transistor Q1 is developed by the voltage divider network composed of resistors R2 and R3 which are connected between -15 vdc and ground. Decoupling for the negative voltage supply is provided by inductors L6 and L7, and capacitors C8, C10, and C12. Capacitor C9 is a bypass for emitter resistor R11. The output from the collector of transistor Q1 is taken from tapped inductor L3 and is applied to the primary of transformer T1. the 70 MHz signal is applied through a resistive T attenuator and a Pi-type impedance matching filter to the center tape of the secondary winding of transformer T1. The two signals are mixed by diode matched pair CR1 and filtered by inductor L4 and capacitors C4 and C5. Resistor R6 provides the proper filter termination impedance. The 21.4 MHz intermediate frequency is coupled by capacitor C6 to the base of transistor Q2. The output signal is taken from the center tap of collector load inductor L5. Resistor R10 provides an output impedance match.

c. Demod 48.6 MHz vco A3 (fig. FO 3-14) consists of an oscillator and amplifiers and is discussed in (1), (2), and (3) below. Control of oscillator Q1 frequency is accomplished by use of varactor diode CR1. The control voltage is applied at pin 6 of jack J2. Any change in the value of varactor bias voltages causes a change in the capacitance of the diode and a corresponding change in the vco output frequency.

(1) The output from oscillator transistor Q1 is taken across resistor R1 and is coupled by capacitor C7 to the base of amplifier transistor Q2. Regenerative feedback is indictively coupled from the collector circuit of transistor Q2 by variable inductor L3 to inductor L2 in the gate circuit of transistor Q1. The output signal from transistor Q2 is applied across a divider network consisting of capacitors C8 through C10. One output from the divider is coupled by diode CR6 through resistor R17 to the inverting input at pin 2 of dc amplifier AR1.

(2) The noninverting input of dc amplifier AR1 is set to -0.8 vdc by the voltage divider consisting of resistors R20 and R21. The output of dc amplifier AR1 controls the gain of transistor Q2 through resistor R4. The combination of dc amplifier AR1, transistor Q2, and diode CR6 form an agc loop to hold the output of diode CR6 constant at -0.8 vdc. In this manner, the power output of the 48.6 MHz vco is held at a constant level over its frequency range. Resistor R18 and capacitor C15 form the feedback network around dc ampliifer AR1. The RC network determines the agc time constant. Diode CR5 and

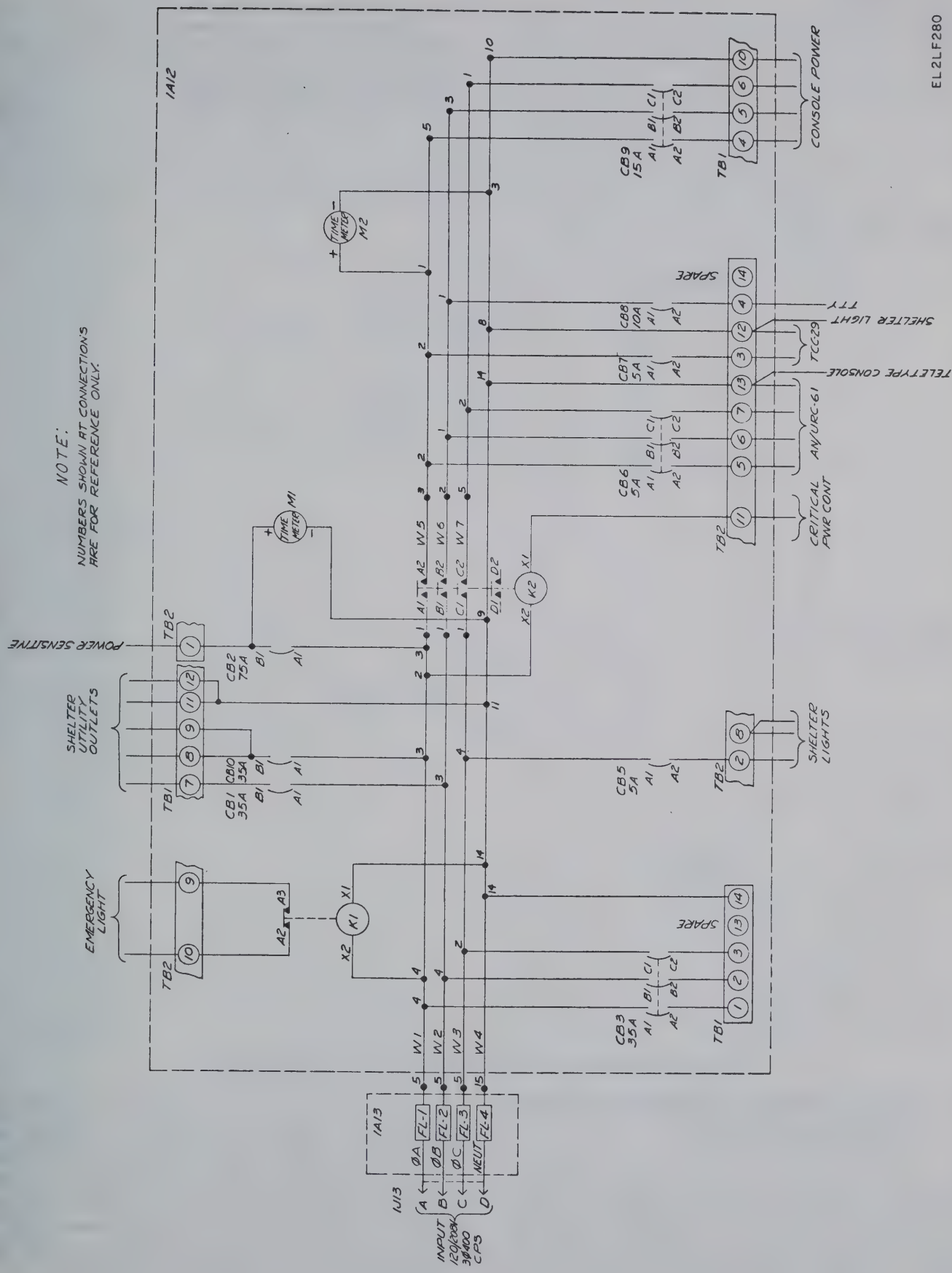

Figure 3-94. Primary power distribution assembly 1A12, schematic diagram.

LAST NO. CHART	
LAST NO.	UNUSED
BT4	
E1	
W1	

NOTES:

1 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S).

2 FOR INTERCONNECTION INFORMATION REF. WIRE LIST DWG. SM-A-778853.

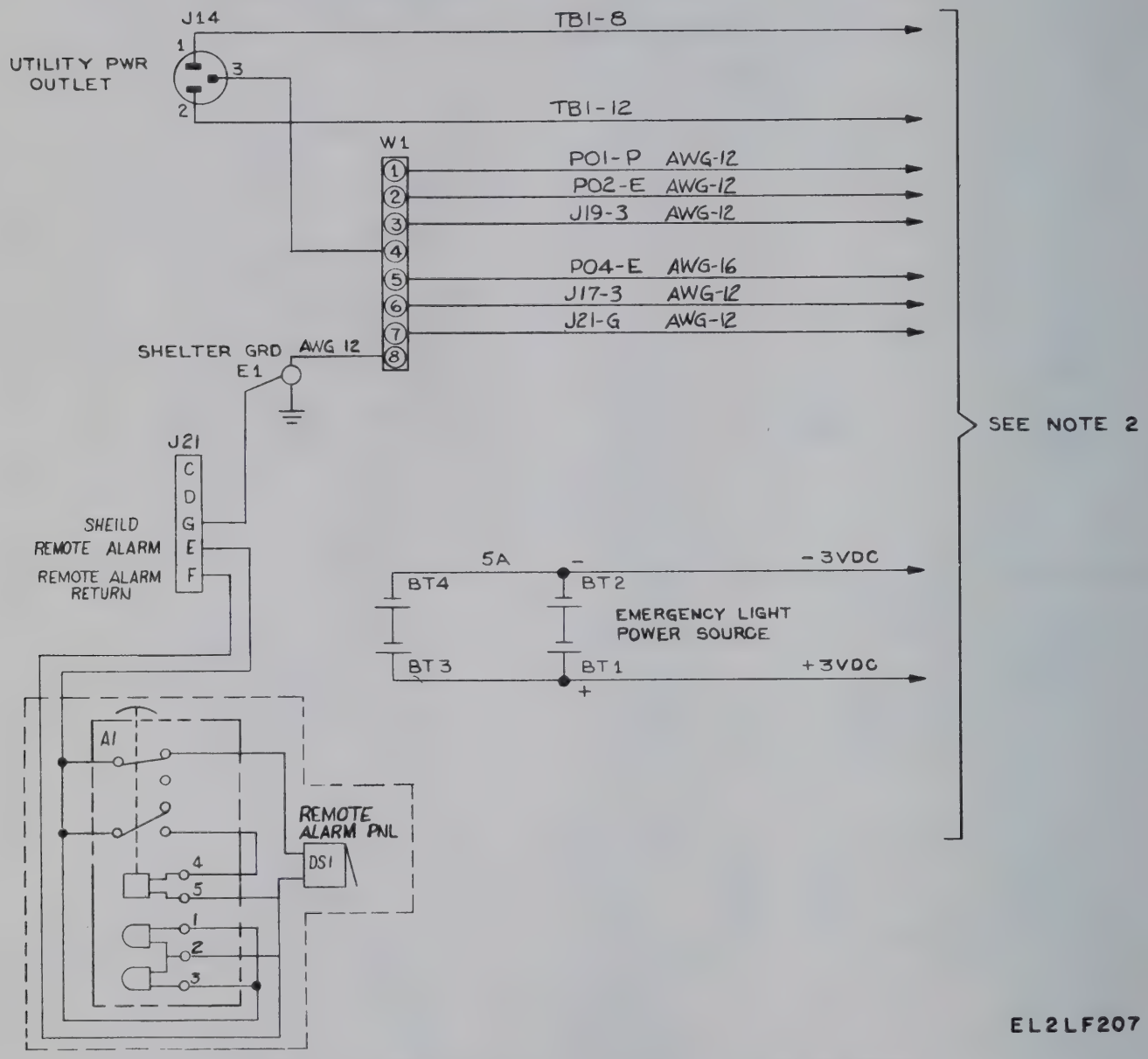

Figure 3-95. External dc power distribution box 1A14, schematic diagram.

3-31. Primary Power Distribution Panel 1A15, Circuit Analysis

(fig. FO 3-50)

The primary power distribution panel provides a distribution point for 115 vac, 3-phase power for the equipment shelter. The 3-phase power is applied to the panel at J1-A through J1-C from power distribution panel 1A12. Note also that neutral and ground are tied to J1-D and J1-E, respectively. All of the inputs are applied to terminal board TB1. From the terminal board the 115 vac is applied through circuit breakers to the output. Thermostat S1 controls shelter heat if switch S2 is OFF. When S2 is ON, the thermostat is bypassed and the shelter heater remains on regardless of the status of the thermostat.

3-32. Primary Power Monitor Panel 1A16, Circuit Analysis

(fig. 3-96)

The primary power monitor panel provides a monitor point for the frequency and voltage of the system power. The panel consists of voltage meter M1, frequency meter M2 and phase switch S1. The 3-phase primary power is applied through phase switch S1 which controls the input to voltage meter M1. Phase A is fed directly to meter M2 which provides an indication of input frequency.

3-33. Shelter Heater 1A17, Circuit Analysis

(fig. FO 3-51)

Shelter heater 1A17 provides heat for personnel comfort and equipment requirements. Heater circuit breaker CB1 on the primary distribution panel 1A15 applies 115 vac, 400 Hz, 3-phase power to thermostat S1 through relay K1 and heaters HR1 through HR6. Thermostat S1 opens at 300° F to protect the heater assembly in the event of failure and closes after opening at 270°F. Switch S2 on the primary power distribution panel bypasses the thermostat when S2 is ON. Primary power reaches fans B1 and B2 through relay K2. Redundant switches S2 and S3 provide a return path for relay K1 if the air flow is interrupted.

NOTE :

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUB-ASSEMBLY DESIGNATION (S).

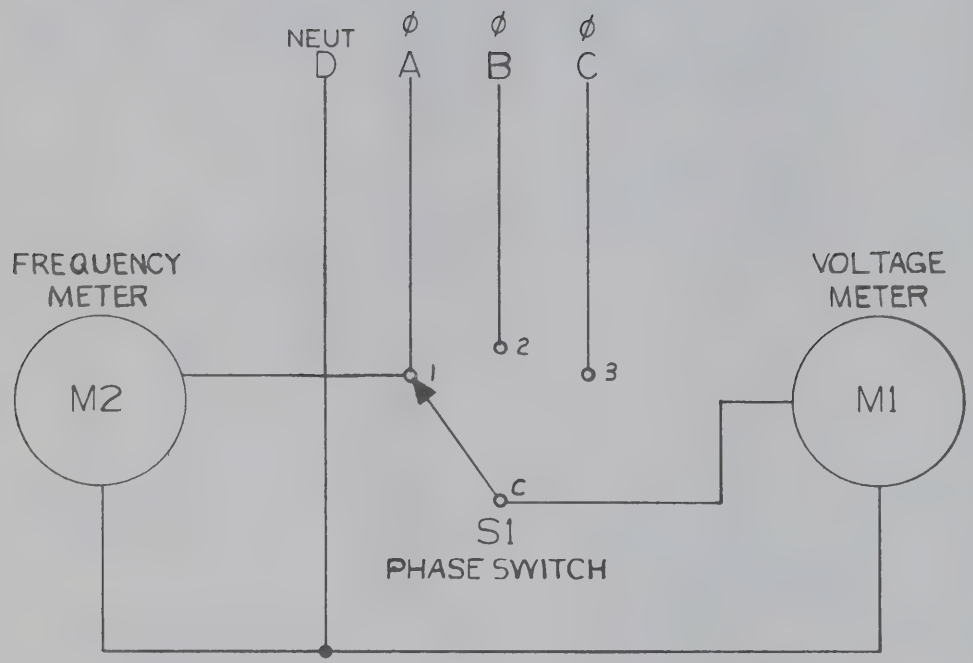

Figure 3-96. Primary power monitor panel 1A16, schematic diagram.

Section II. ANTENNA GROUP COMPONENTS

3-34. Power Supply PS1, Circuit Analysis

(fig. 3-97)

Power supply PS1 furnishes the high voltage required for operation of the AN/TSC-54 transmitter. The circuit consists of a three-phase full wave bridge rectifier for the high voltage circuit and a single-phase full wave bridge rectifier for a lower voltage output. Transformer T1 is a multitapped delta wound primary; wye round secondary. Bridge rectifier A1 rectifies the secondary voltage of transformer T1 and filtering of the output is provided by the two-section LC filter comprised of coil L1 and capacitor C1 and coil L2 and capacitor C2. The 13 KV high voltage output is applied to output terminals A and C through surge resistor R1. Resistors R3 and R4 form a voltage divider to provide an output to the beam voltmeter. The low voltage supply transformer T2 is energized through terminals E and F and the related bridge rectifier provides the necessary dc output which is filtered by the LC section consisting of capacitor C3 and inductor L3. The output is taken from terminals C and D. The link connections shown on the schematic diagram are for the 13 KV output requirement. For other output voltages the input link links can be connected to tape #4 for 12.3 KV, to #3 for 11.6 KV and to #2 for 10 KV.

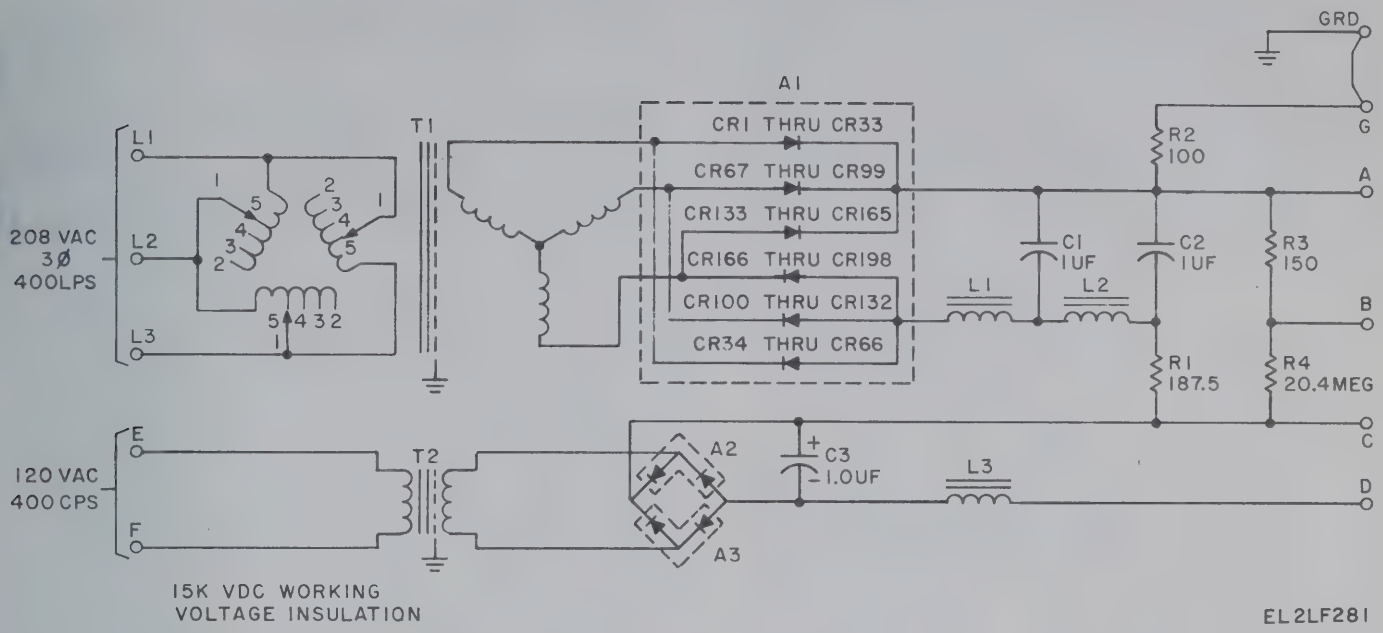

Figure 3-97. Power supply PS1, schematic diagram.

3-35. Transmitter Liquid Cooler 2A3A3

(fig. 3-98)

a. The transmitter liquid cooler 2A3A3 consists of heat transfer assembly 2A3A3A2 and rfi filter 2A3A3A1, and it is a liquid-to-air type heat transfer system utilizing an ethylene glycol and water coolant. The coolant mixture consists of 60 percent uninhibited ethylene glycol and 40 percent distilled water and is supplied at a minimum pump outlet pressure of 40 pounds-per-square-inch (psi). Coolant is pumped at a rate of 10 gallons per minute (gpm) and at a temperature of 63° C to 70° C (145° F to 158° F) while operating in ambient temperatures up to 49° C (120° F). The capacity of the system is approximately 3 gallons. Coolant carrying heat from the transmitter equipment is returned to the reservoir. The reservoir contains an air-space to allow for liquid expansion and a radiator-type pressure fill cap with a relief setting of 15 psi and the reservoir coolant level is monitored by two differential pressure switches.

b. Low liquid warning switch S2 opens and low liquid interlock switch S1 closes when the coolant is at the proper level. Switch S2 closes when the coolant level drops 3½ inches, and as a result, +28 vdc unregulated power is applied through pins J2-C and J2-B, filter FL1A1, and pin Z of connector W1P26 (fig. FO 2-4, sheet 5) to LOW LIQUID WARNING indicator DS1 (amber) on the transmitter control panel. Indicator DS1 illuminates and remains illuminated until equipment power is shut down or the coolant is replenished. When the coolant level drops 5 inches, switch S1 opens (fig. FO 2-4, sheet 3) and deenergizes low liquid interlock relay K17 which removes the transmitter and beam power. Closed contacts A2 and A3 of relay K17 apply firing current to an SCR in latch circuit number 4 (fig. FO 2-4, sheet 6 and fig. 3-100), which in turn, applies power to illuminate LOW LIQUID indicator DS20 (red).

c. The system centrifugal pump takes coolant by suction from the reservoir and discharges it under pressure to one of three flow paths. One path is through the full flow three micron filter assembly through a particle filter coolant flow switch S3 to the heat exchanger and temperature control valve. Switch S3 remains open as long as satisfactory flow of coolant is maintained through the three micron filter. When the cooland flow decreases to 7.5 gpm due to clogging of the particle filter or any other faulty condition, switch S3 closes and applies +28 vdc unregulated power through filter FL1C1 and pin P26-NN (fig. FO 1-4, sheet 5) to illuminate LOW PARTICLE FIL COOL FLOW indicator DS2 (amber). Indicator DS2 remains illuminated until equipment power is shut down. This indicated fault is normally corrected by replacement of the three micron filter. Another path is through the filter bypass valve to the heat exchanger and temperature control valve. The last path is through the backflush valve to the temperature control valve and outlet of the heat exchanger. Thus, hot coolant is supplied direct from the pump to the temperature control valve and cold coolant is applied from the heat exchanger to the valve.

d. Cooling is achieved in the heat exchanger by the fan drawing ambient air through the heat exchanger and exhausting it out through the fan orifice. The temperature control valve senses the

output coolant temperature and automatically mixes hot and cold coolant to provide a constant flow of fluid between 63° C and 70° C (145° F and 158° F) to the transmitter equipment. The coolant temperature and pressure are sensed at the output of the temperature control valve, and the values are displayed on gages located on the heat transfer system panel.

e. A portion of coolant (1/6 gallon per minute) from the pump is directed through a conductivity cell and a flow meter to the deionizer. The deionizer removes ions, minerals and oxygen from the coolant. The treated coolant is returned to the reservoir through a 0.35 micron filter, a second conducting cell and a flow control orifice.

f. The coolant from the temperature control

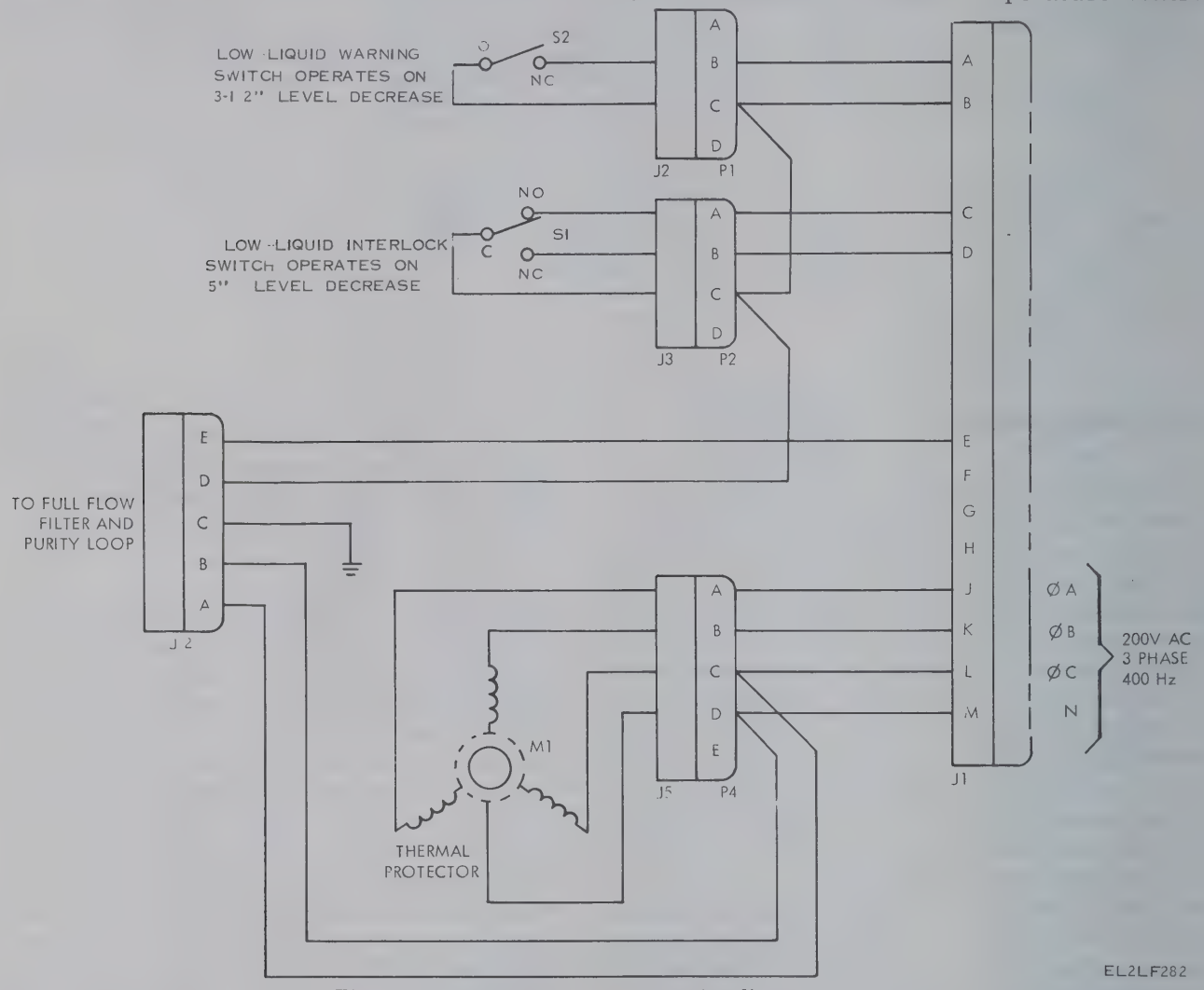

Figure 3-98. Heat transfer system, wiring diagram.

valve is applied to a manifold for distribution to the transmitter equipment. The coolant temperature is monitored by thermostatic switches S1 and S2 (fig. FO 2-4, sheet 3). If the coolant temperature is below 68° ± 3° C (154° ±5° F), high coolant temperature switch S1 is closed and system coolant high temperature relay K21 is energized. When coolant reaches an abnormally high temperature of 73° ±2° (163.5° ±3.5° F), switch S1 opens and relay K21 deenergizes. Closed contacts A2 and A3 of relay K21 apply firing current to an scr in latch circuit number 4 (fig. FO 2-4, sheet 6) which in turn applies power to illuminate HIGH COOL TEMP indicator DS21 (red).

g. If the coolant temperature is above 1° ±2° C (34° ±4° F), low coolant temperature switch S2 is open. When the coolant temperature drops below —4.5° ±2° C (24° ±2° F), switch S2 closes and initiates two actions. First, +28 vdc unregulated power is applied through diode CR5 (fig. FO 2-4, sheet 5) to illuminate LOW COOL TEMP indicator DS4 (amber) on transmitter control panel 2A3A7 and througb filter FL13A2 in primary power distribution panel 2A3A14 to illuminate LOW COOLANT TEMPERATURE indicator DS7 (amber) on rf power monitor and control panel 1A3A27 (fig. FO 2-4, sheet 3) in transmitter exciter 2A3A10. Relay K1 applies power to heater HR1 and the coolant

from the manifold is heated to compensate for extreme cold ambient temperatures. A pressure relief valve on the heater is set to operate at 200 psi.

h. Coolant flow through the transmitter equipment is monitored by flow switches S3 through S6 (fig. FO 2-4, sheet 3). Fluid must flow through waveguide and dummy load switch S2 and body and magnet switches S3 and S6 at a rate in excess of 1 gallon per minute. Flow through collector switch S5 must exceed 5 gpm. When the coolant flow through switch S3 or S6 drops below .5 gpm, the switch opens and body and magnet flow relay K18 is deenergized. Closed contacts A2 and A3 of relay K18 apply —28 vdc regulated power to fire an scr in latch circuit number 4 (fig. FO 2-4, sheet 6) which in turn applies power to illuminate BODY AND MAG FLOW indicator DS22 (red) on transmitter control panel 2A3A7. Liquid flow rate switches S4 and S5 (fig. FO 2-4, sheet 3) are connected in series to the +28 vdc regulated power source. Either switch (but not both) can simultaneously illuminate an associated fault indicator and deenergize flow switches relay K19. Relay K19 is energized if satisfactory coolant flow is maintained through the waveguide components, dummy load and klystron collector coolant jackets. Under normal coolant flow conditions, flow switch S4 applies +28 vdc regulated power through switch S5 to energize relay K19. If the waveguide and dummy load coolant flow drops below 1 gpm, switch S4 operates to remove +28 vdc power from collector flow switch S5 which inhibits the collector flow indicator function, deenergize flow switches relay K19 and illuminate WG AND DUMMY LOAD FLOW indicator DS23 (red) on the transmitter control panel 2A3A7 through latch circuit number 1 (fig. FO 2-4, sheet 6). If the collector coolant flow rate drops below 5 gpm, flow switch S5 (fig. FO 2-4, sheet 3) operates to deenergize flow switches relay K19 and illuminate COLLECTOR FLOW indicator (red) on transmitter control panel 2A3A7 through latch circuit number 1 (fig. FO 2-4, sheet 6). Either indicator remains illuminated until a momentary interruption of the +28 vdc power by means of fault reset switches resets latch circuit number 1.

3-36. Transmitter Control Panel 2A3A7, Circuit Analysis

(figs. 3-99 through 3-105 and FO 3-52)

The transmitter control panel of the AN/TSC-54 centralizes transmit function controls and indicators at antenna pedestal 2A3. The panel consists of metering circuits for selective monitoring of power, voltages and currents; switches for turn-on and control of power; and circuits for the display of actual and simulated faults. Operational theory discussions of the latch circuit, power sensing, power comparator, and diode switch modules of the transmitter control panel are given in *a* through *g* below.

a. Latch circuit No. 1 (fig. 3-99) has three identical silicon-controlled rectifier (scr) circuits individually capable of being switched to a continuous "on" state by a fault signal. Once turned "on", the circuit conducts, driving an indicator lamp or relay, until the current path is externally interrupted by means of a reset switch. The following discussion is limited to the scr CR3 circuit which is typical of the three circuits contained in the module.

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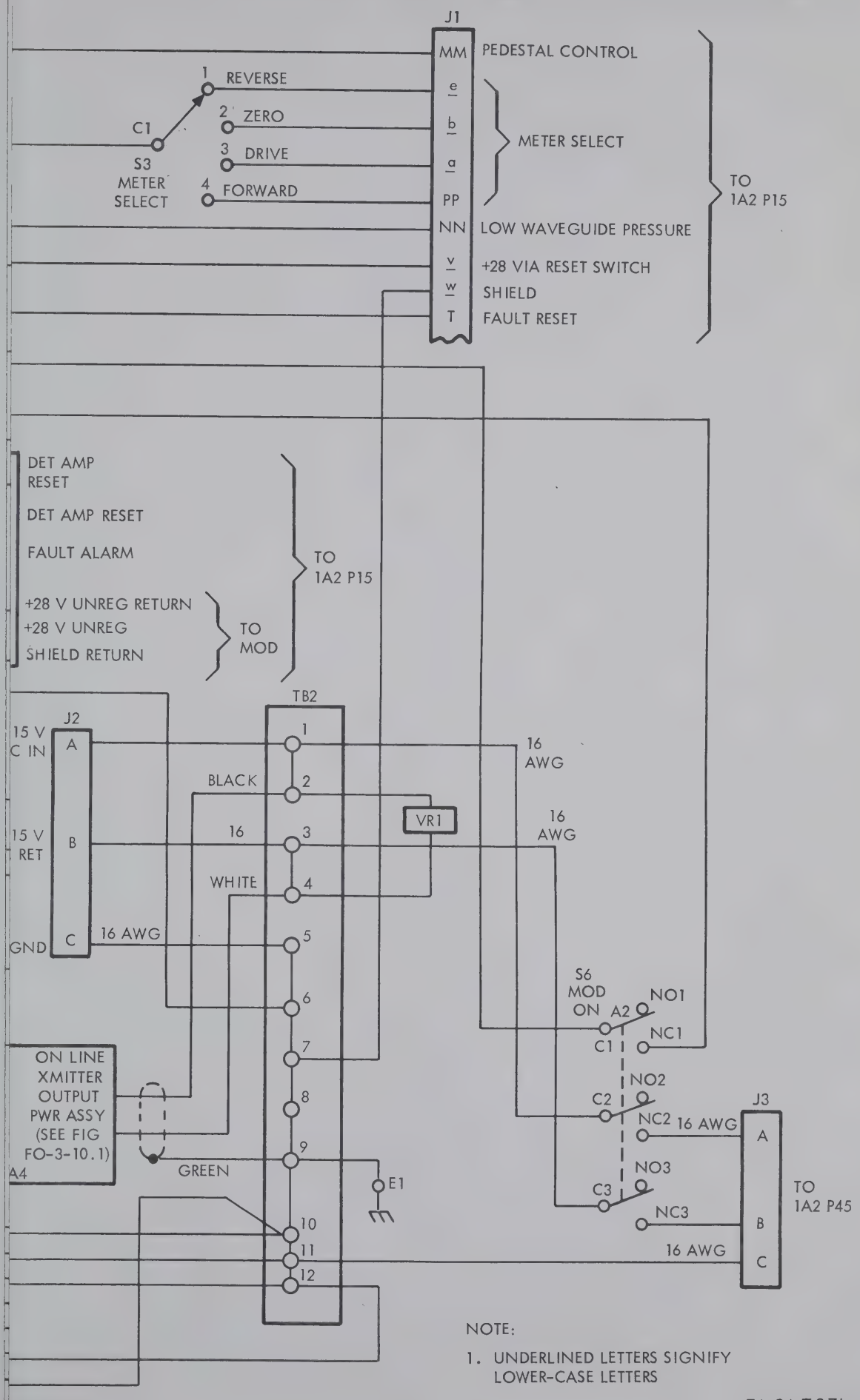


NOTE:

1. UNDERLINED LETTERS SIGNIFY LOWER-CASE LETTERS

EL2LF271

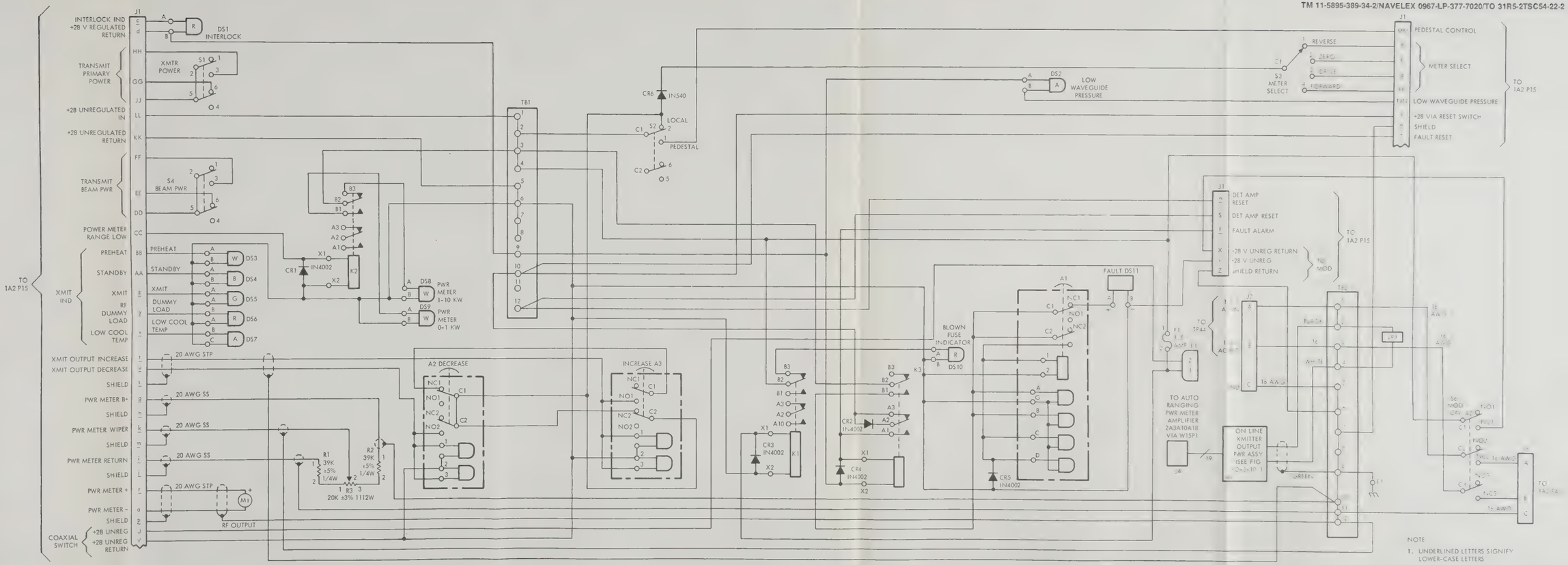
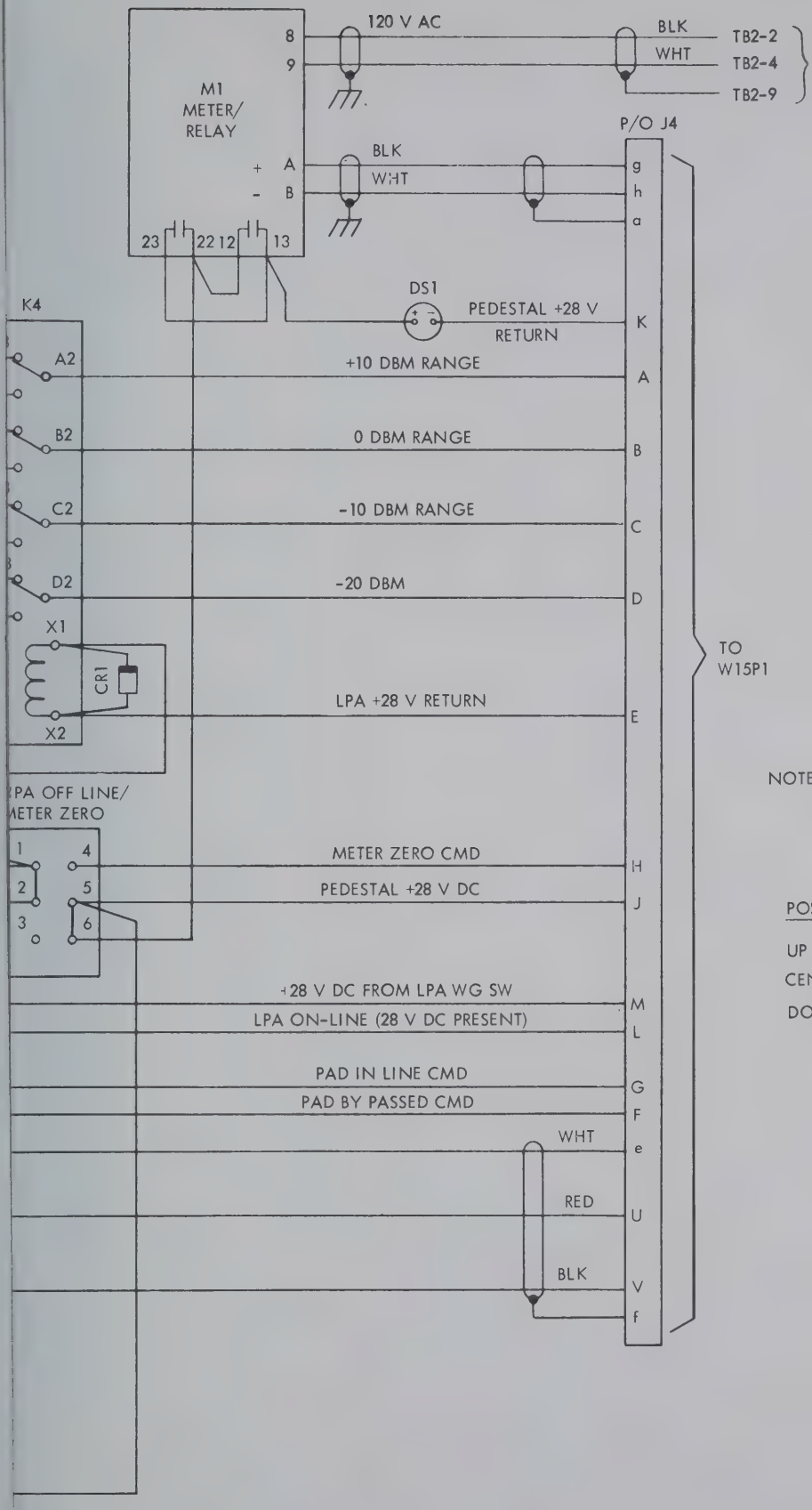


Figure FO 3-10. Rf power monitor and control 1A2A27, schematic diagram.



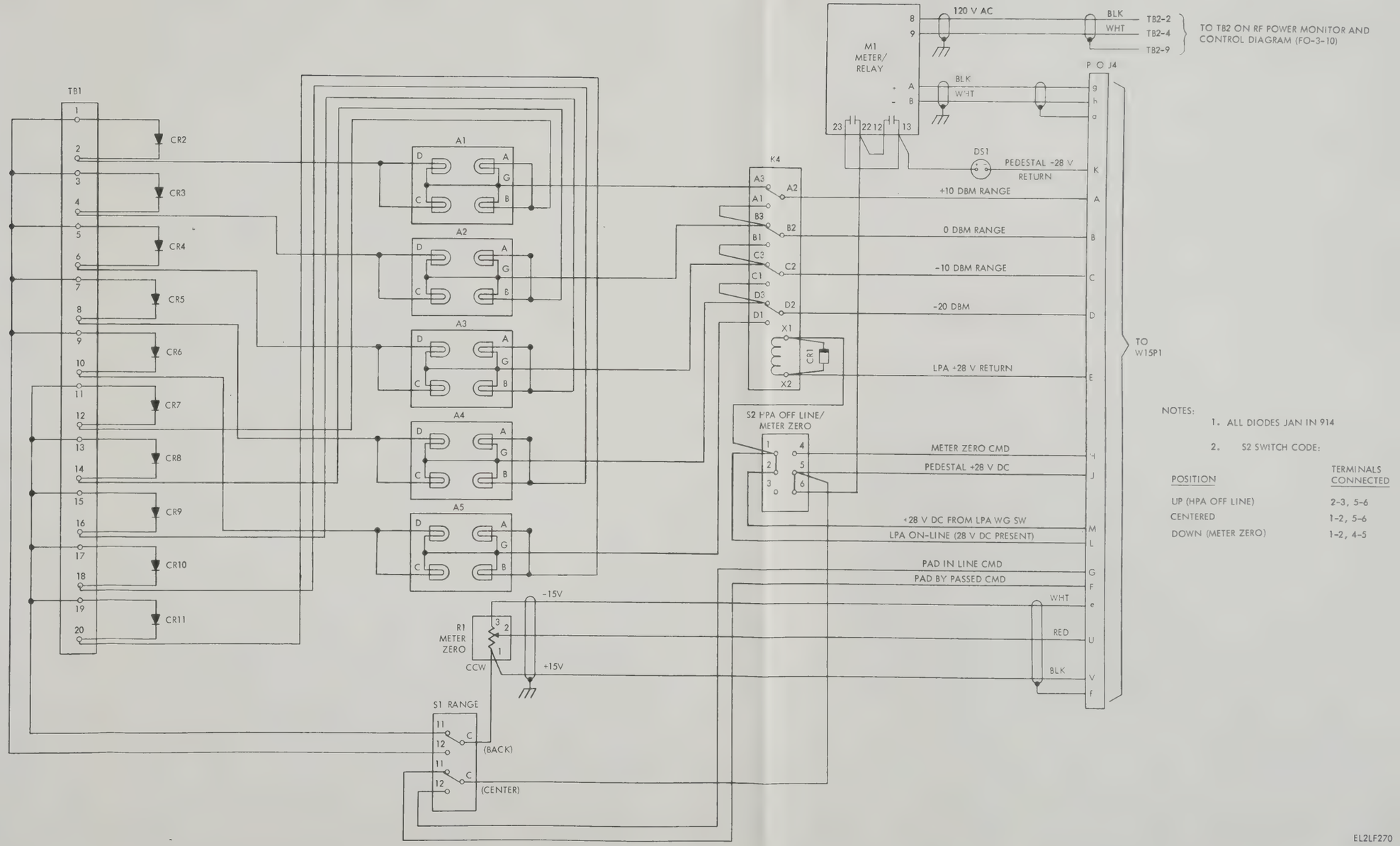
NOTES:

1. ALL DIODES JAN IN 914
2. S2 SWITCH CODE:

POSITION	TERMINALS CONNECTED
UP (HPA OFF LINE)	2-3, 5-6
CENTERED	1-2, 5-6
DOWN (METER ZERO)	1-2, 4-5

EL2LF270

ly 1A2A27A4, schematic diagram.



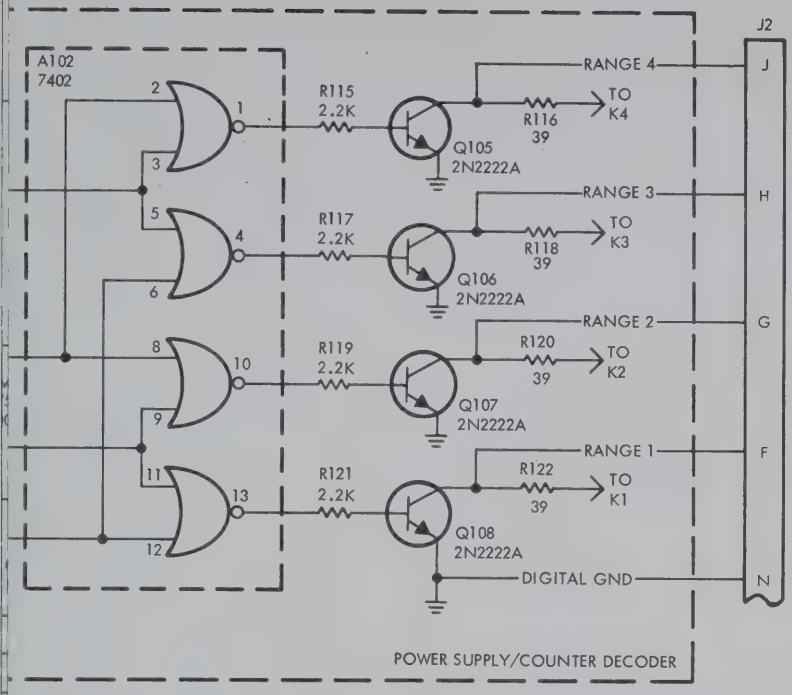
NOTES:

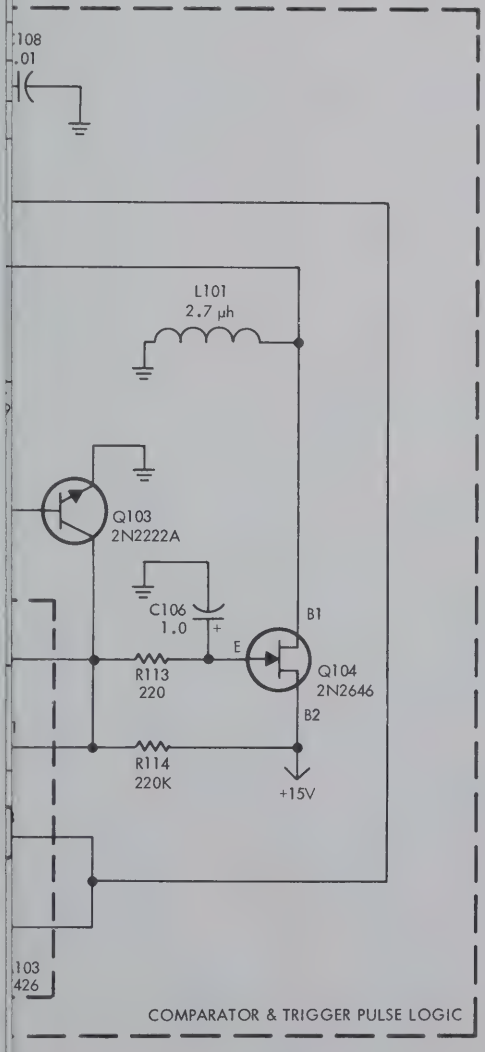
1. ALL DIODES JAN IN 914
2. S2 SWITCH CODE:

POSITION	TERMINALS CONNECTED
UP (HPA OFF LINE)	2-3, 5-6
CENTERED	1-2, 5-6
DOWN (METER ZERO)	1-2, 4-5

EL2LF270

Figure FO 3-10.1. On-line transmitter output power assembly 1A2A27A4, schematic diagram.





NOTES:

1. UNLESS OTHERWISE SPECIFIED

   RESISTANCES ARE GIVEN IN OHMS
   CAPACITANCES ARE GIVEN IN MICROFARADS

2. WAVEFORM OBSERVED WHEN AR4 IS REMOVED & K4 IS ACTIVATED.

3. A102, A103, A104 & A105 - PIN 14 IS +5V, PIN 7 IS GROUND

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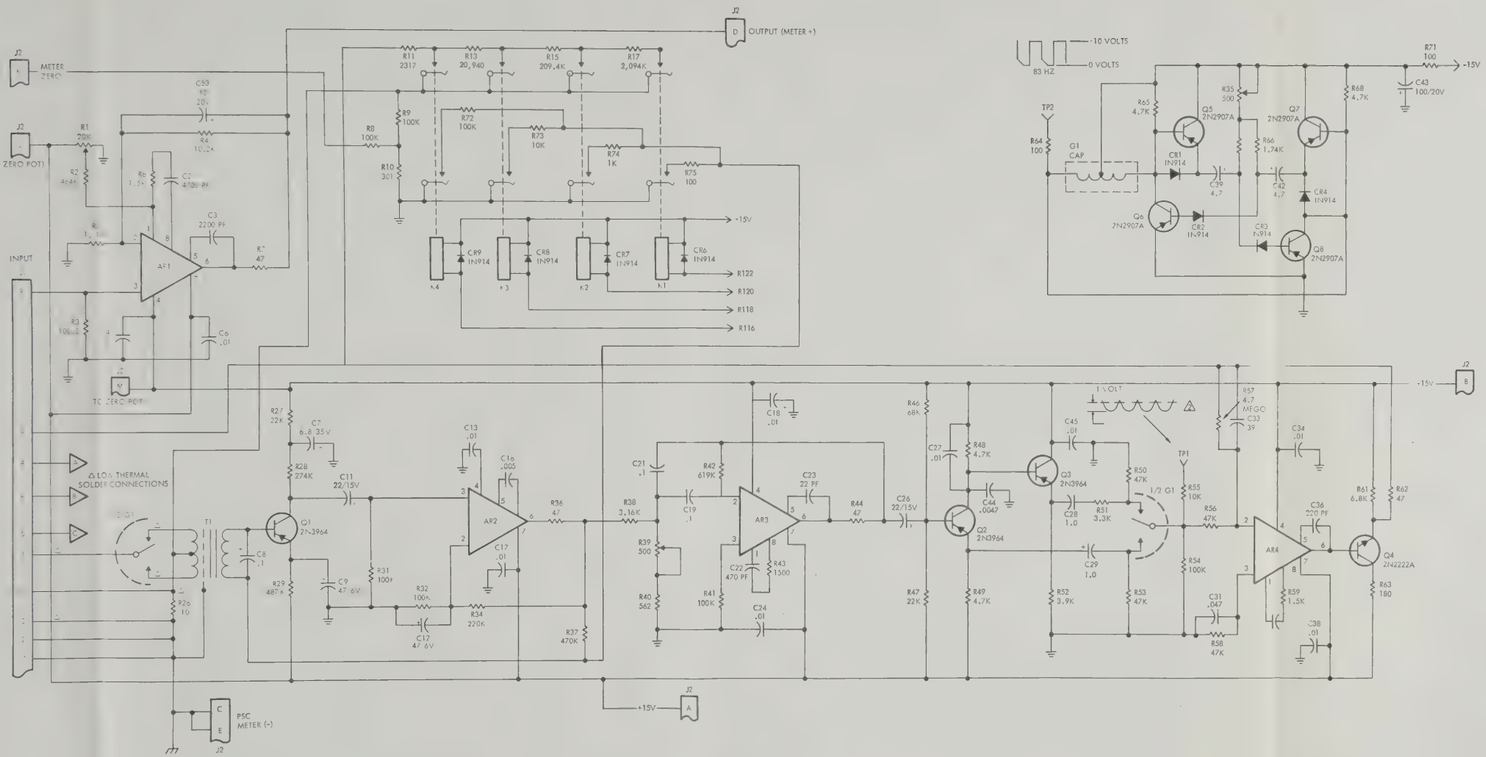

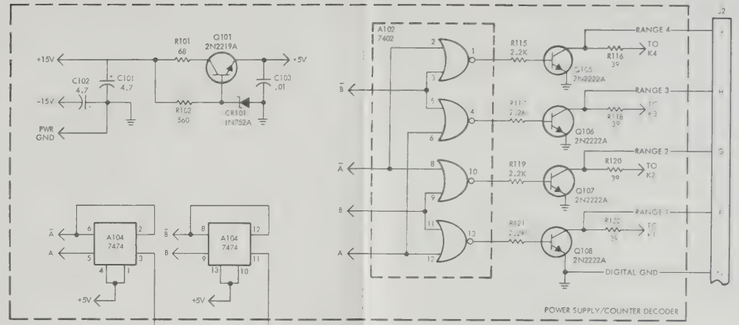

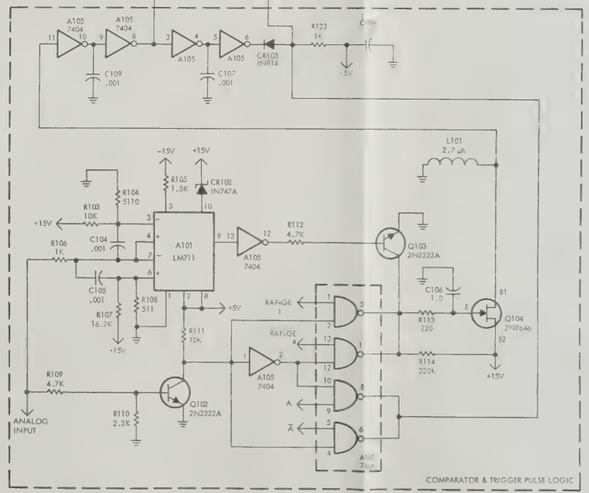

NOTES

1. UNLESS OTHERWISE SPECIFIED

   RESISTANCES ARE GIVEN IN OHMS
   CAPACITANCES ARE GIVEN IN MICROFARADS

2. WAVEFORM OBSERVED WHEN AR4 IS REMOVED & K4 IS ACTIVATED.

3. A102, A103, A104 & A105 - PIN 14 IS +5V, PIN 7 IS GROUND

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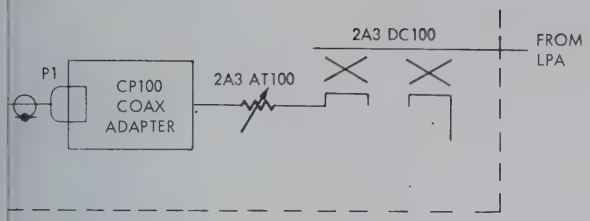
Figure FO 8-11. 40-dB autoranging meter amplifier 2A8A10A18, diagram.



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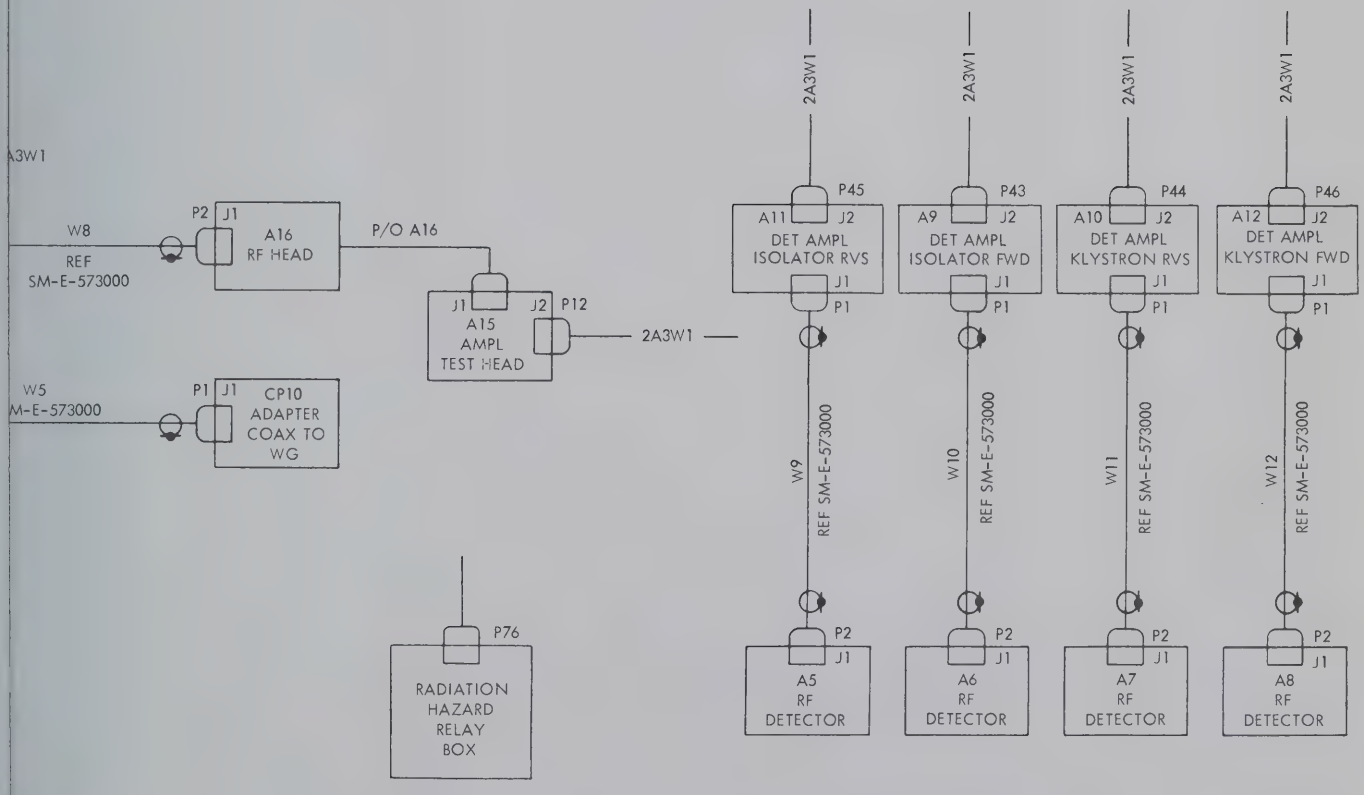

ing diagram.

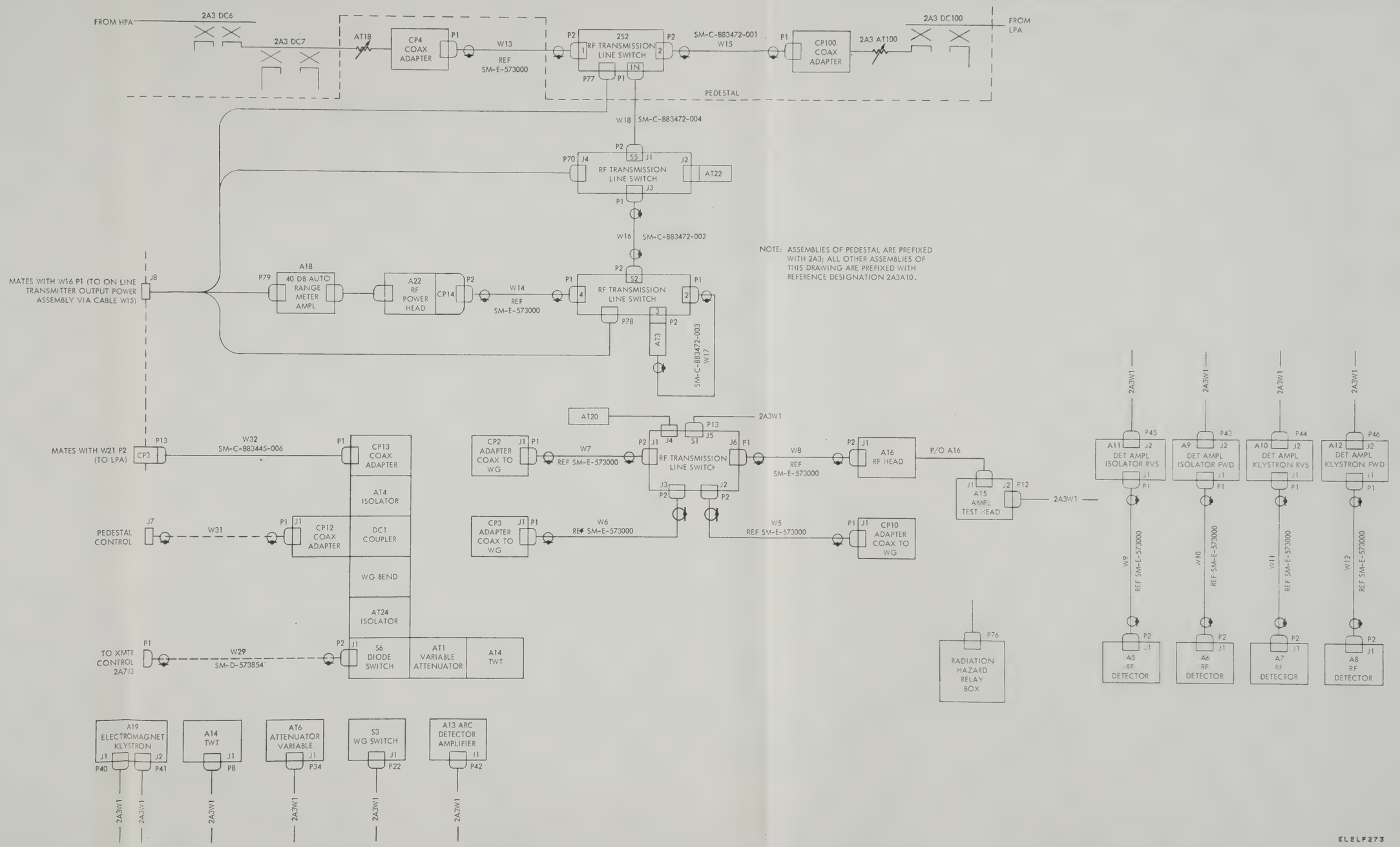

Figure FO 3-54. Transmitter/exciter, cabling diagram.

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DEPARTMENTS OF THE ARMY,
THE NAVY, AND THE AIR FORCE
WASHINGTON, DC, *17 March 1980*

Direct Support and General Support Maintenance Manual SATELLITE COMMUNICATION TERMINAL AN/TSC-54 (DETAILED CIRCUIT ANALYSIS) (NSN 5895-00-937-4993)

TM 11-5895-389-34-2/NAVELEX 0967-LP-377-7090/TO 31R5-2TSC54-22-2, 5 January 1978, is changed as follows:

1. Remove old pages and insert new pages as indicated below.
2. New or changed material is indicated by a pointing hand, a shaded area, or a vertical bar in the margin of the page.

	Insert
iii through v	iii through v
3-109 and 3-110	3-109 through 3-110.1
Fig. FO 3-2 (sheet 2)	Fig. FO 3-2 (sheet 2)
None	Fig. FO 3-49.1

3. File this change sheet in the front of the publication for reference purposes.

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current characteristics to automatically adjust the current demanded from the drive amplifier because of varying load conditions. When the drive signal is removed, diode CR1 and capacitor C1 provide negative bias to the bases of transistors Q1 and Q2 to assure rapid turn off. Diode CR2 permits reactive currents to flow when the output voltage and current are out of phase. All drive current to the power block, including the current which flows in the output stage of the driver amplifier, is useful load current.

f. The 120 vac ±10%, 60 Hz, single-phase output power (fig. FO 3-48) is applied to the AN/UGC-77 teletypewriter through 10A circuit breaker CB2 and output power connector J2. Output power is also supplied to convenience outlet J3 through 10A circuit breaker CB3. The maximum load current that can be applied to either utility power or output power connector is 10A. Maximum total load current that can be drawn from the system is 17 amperes, continuous at unity power factor or 21.3A under 0.8 power factor.

g. Inrush limiter A8 (fig. FO 3-48) contains resistor R4 which protects the 2.0 kw static frequency converter from input surges. After a delay of approximately 200 milliseconds, relay K1 energizes to bypass resistor R4. Protection against low input voltage is also provided by A8 and output voltage does not appear until the input line is approximately 185 vac.

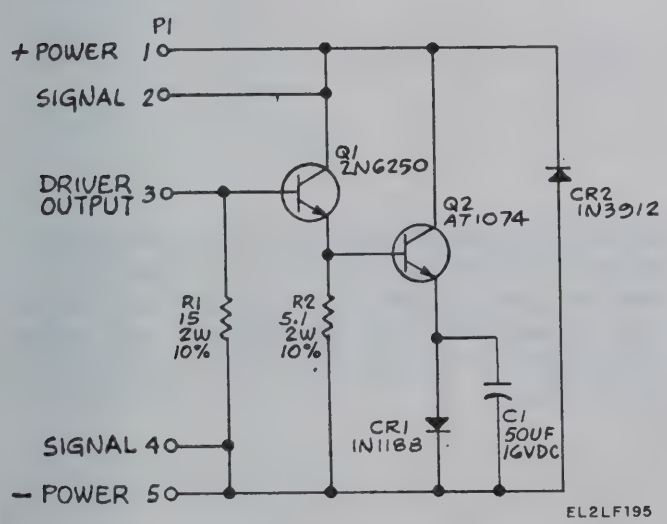

Figure 3-92. Power blocks A1, A2, A3, and A4, schematic diagram.

3-28.1 OBN Monitor Panel 1A3A24 (figs. 3-92.1 and FO 3-49.1)

The OBN monitor panel provides an on-line indication of the received signal quality for eight channels. An alarm is generated when the signal on any one of the eight channels goes out of tolerance. The channel to be monitored is selected by CIRCUITS switch S1. The monitor panel also contains a TTNR meter, visual and audible alarm indicators, channel isolator, TTNR fault detector, and meter circuit.

a. The power for all active elements in the panel circuitry, excluding fault indicator switch Q1, is supplied through the voltage regulator and level converter. This converts +28 v to +15 v.

b. The channel isolator first ensures that only the active channels are being tested in the fault detector immediately following this stage. The output of the voltage regulator is routed to the channel isolator to deactivate the unused channels. The channel isolator also contains a manually operated switch which permits only a single channel to be monitored by the meter circuit.

c. The circuitry for triggering the alarms is contained in the TTNR fault detector. It is comparison circuit of which one set of inputs are the OBN signals from the channel isolator. The other inputs are taken off a +8 v reference voltage. The +8 v is generated from the +15 v supply by the dc level converter. When the OBN level exceeds the reference voltage level, the output of the TTNR fault detector changes state, triggering the visual and audible alarms.

d. The conversion of the noise voltage level to a visual reading of TTNR is performed by the buffer amplifier, –11 v reference generator, summer, and two temperature-compensated log amplifiers. The buffer amplifier converts the single-channel noise signal from the channel isolator to a value near 0 volt under normal conditions. The –11 v reference generator provides the reference voltage to the buffer amplifier. The output rises with any increase in the input OBN signal level. The output of the buffer amplifier is added to an adjustable reference voltage by the summer to provide a +8 v input to temperature-compensated log amplifier 1. Temperature-compensated log amplifiers 1 and 2 operate as a differential amplifier with the TTNR meter indicating whether it is balanced. Temperature-compensated log amplifier 2 has as its input a reference voltage from the voltage regulator. Under normal conditions, a full scale reading on the TTNR meter would be caused by an unbalanced state between the two temperature-compensated log amplifiers. As the received signal quality degenerates (increase in OBN signal level), the two amplifiers will approach a balanced differential amplifier state causing a low TTNR reading to be indicated.

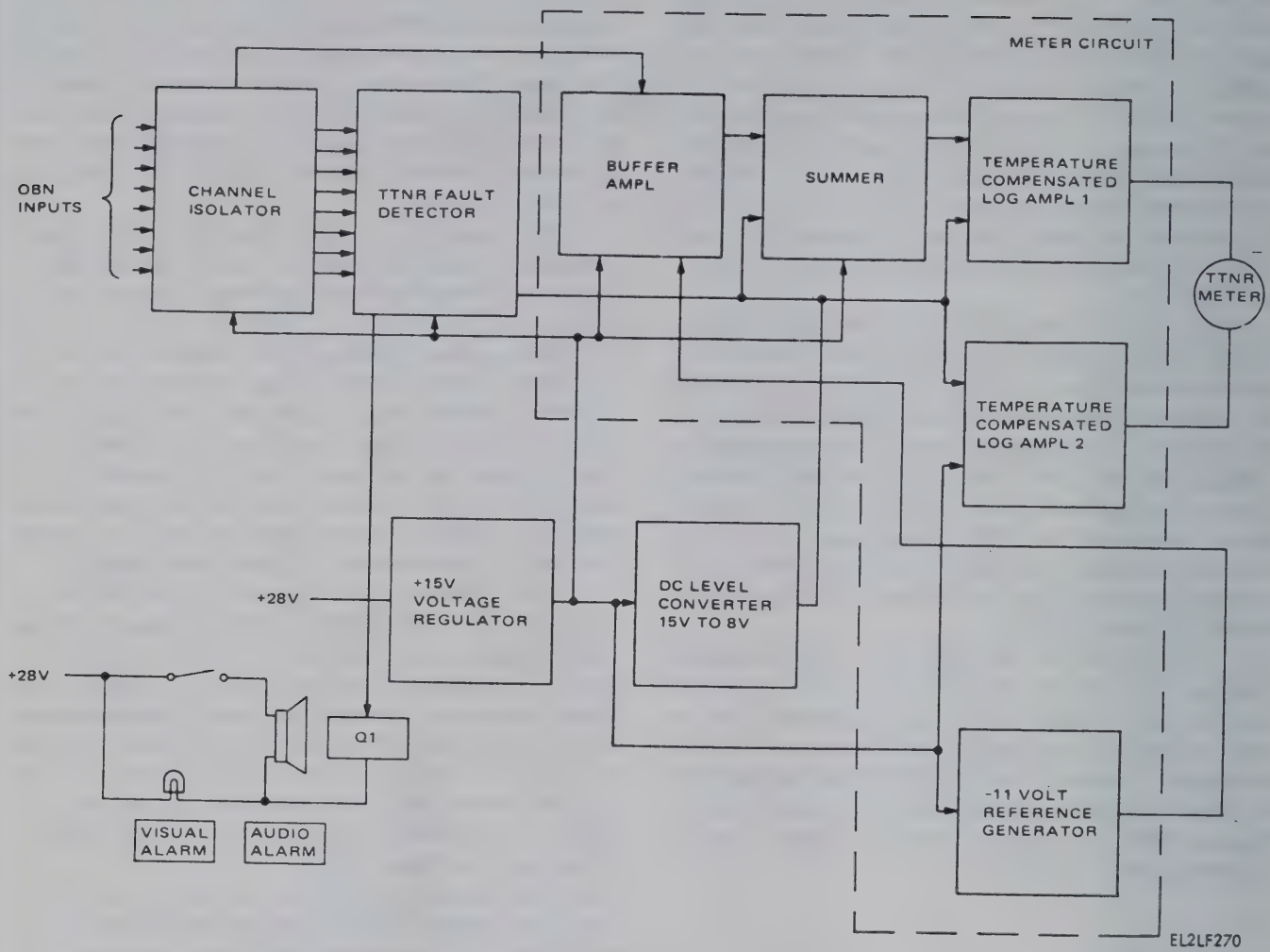

Figure 3-92.1. OBN monitor panel (1A3A24), block diagram.

3-29. External Signal Distribution Box 1A10, Circuit Analysis

(fig. 3-93)

The external signal distribution box provides the interfacing facilities between the external user and the shelter. The input and output lines are protected by spark gaps E101 through E204 and fuses F1 through F104. Filters FL1 through FL52 provide the necessary rf rejection. Filters FL51 and RL52 offer minimum impedance to frequencies between 0 and 23 kHz. Coaxial cables W105, W106, and W107 provide for transmission of the 70 MHz signal.

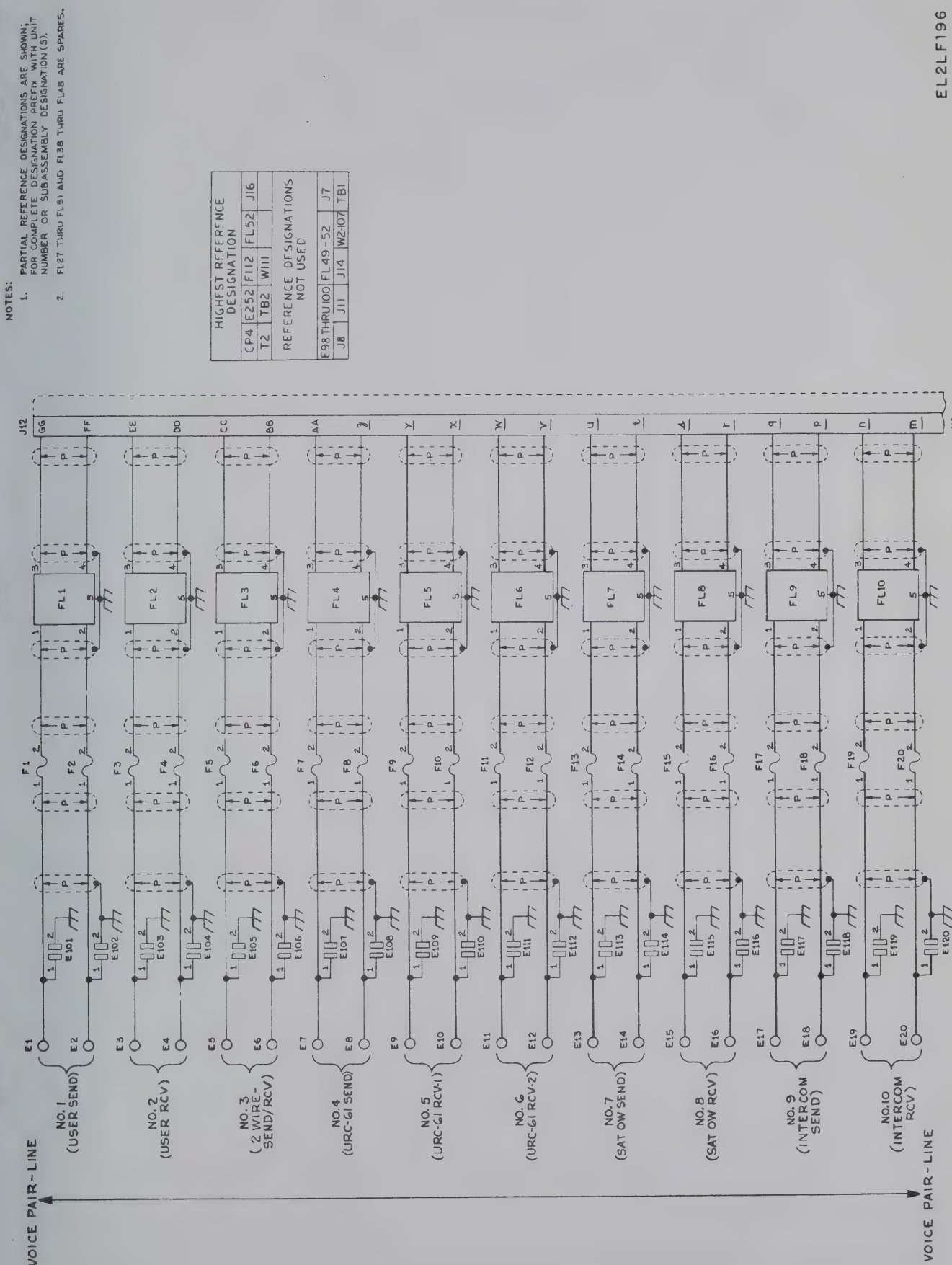

Figure 3-93.① External signal distribution box, wiring diagram (sheet 1 of 9).

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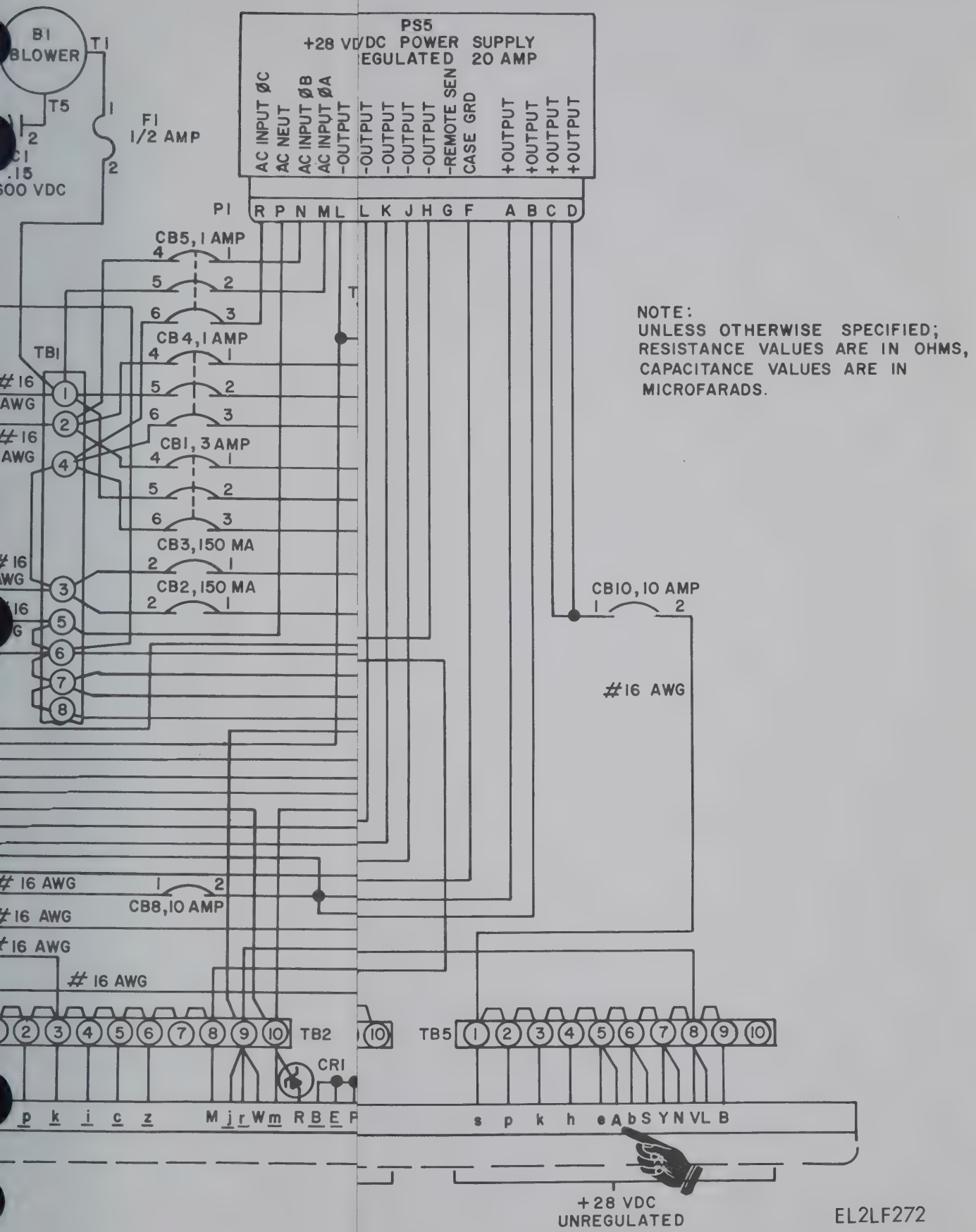

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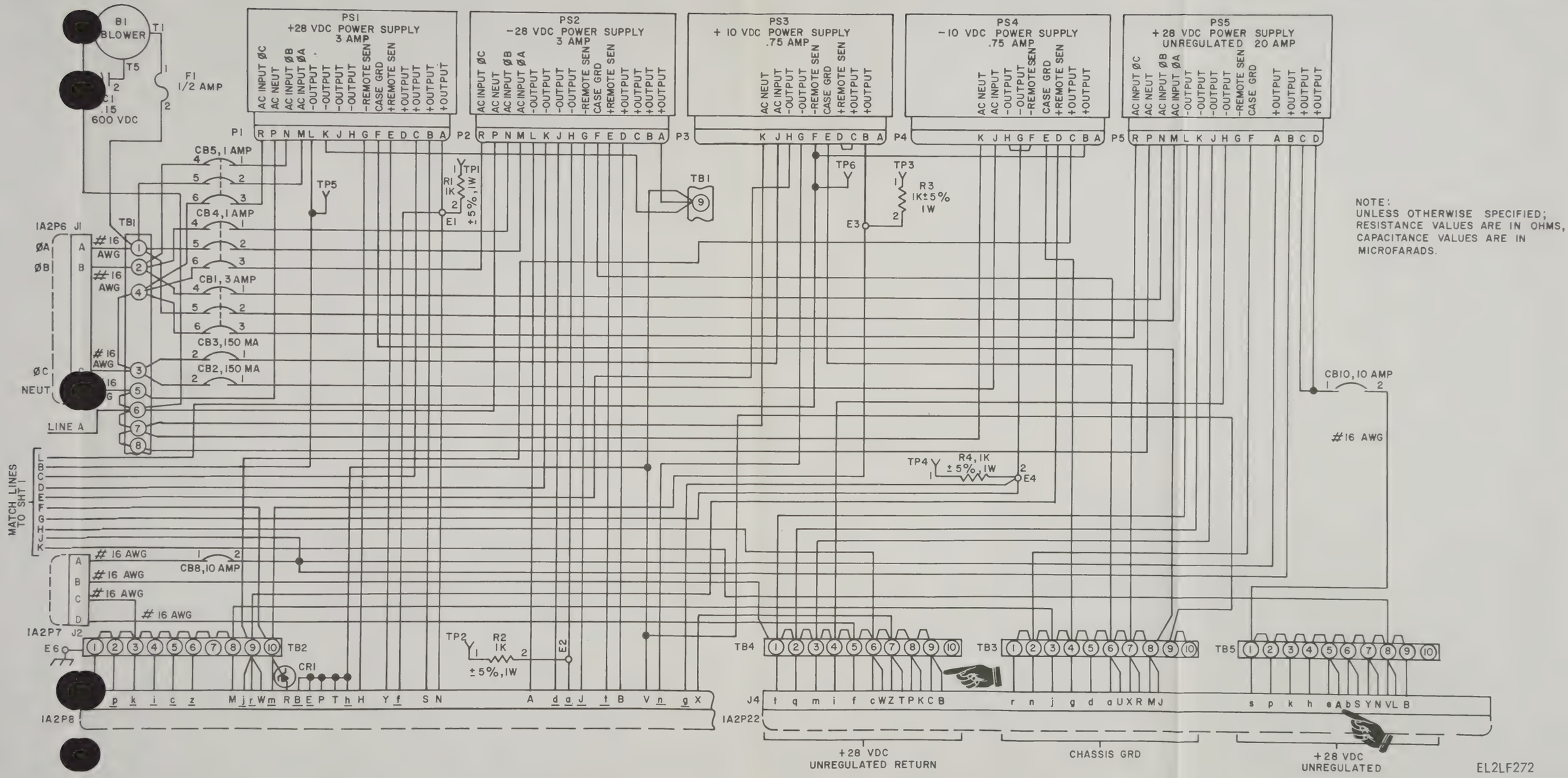
MICROFARADS.



NOTE:
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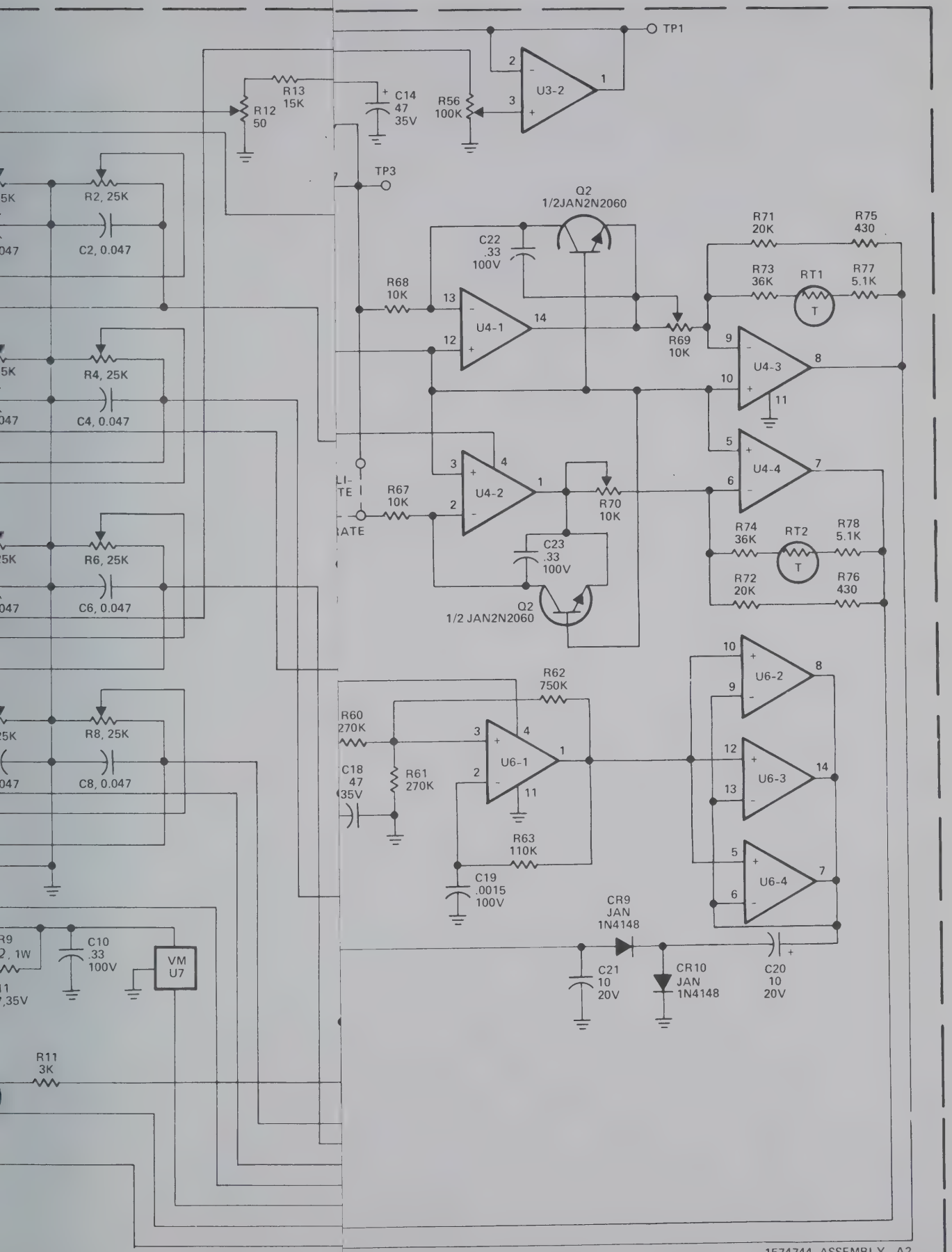
Figure FO 3-2. Power distribution panel, schematic diagram (sheet 2 of 2).


TP1
U3-2
R13
15K
R12
50
C14
47
35V
R56
100K
TP3
Q2
1/2JAN2N2060
C22
.33
100V
R71
20K
R75
430
R73
36K
RT1
R77
5.1K
R68
10K
U4-1
R69
10K
U4-3
R2, 25K
C2, 0.047
R4, 25K
C4, 0.047
R6, 25K
C6, 0.047
R8, 25K
C8, 0.047
U4-2
R67
10K
R70
10K
U4-4
R74
36K
RT2
R78
5.1K
R72
20K
R76
430
C23
.33
100V
Q2
1/2 JAN2N2060
R62
750K
R60
270K
U6-1
C18
47
35V
R61
270K
U6-2
U6-3
U6-4
R63
110K
C19
.0015
100V
CR9
JAN
1N4148
C21
10
20V
CR10
JAN
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C20
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.33
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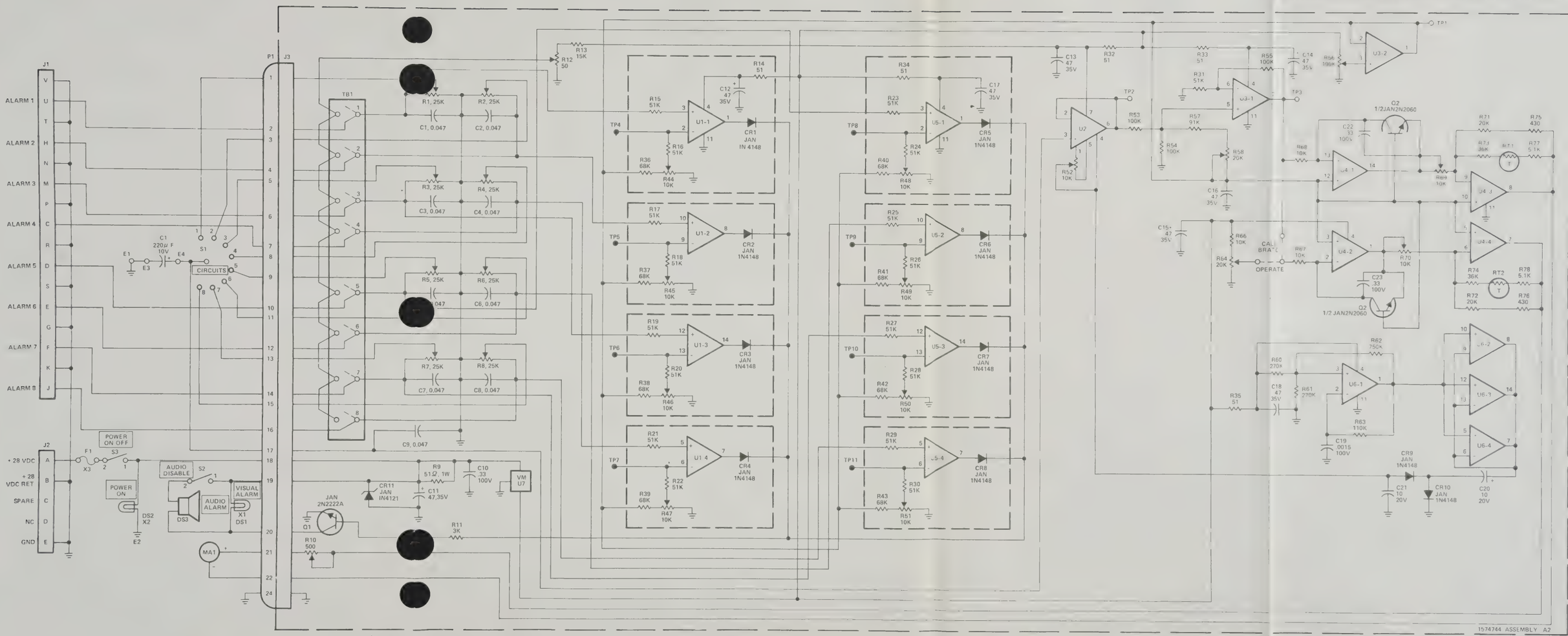

Figure FO 8-49.1. OBN monitor panel (1A3A24), schematic diagram.

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Direct Support and General Support Maintenance Manual For SATELLITE COMMUNICATION TERMINAL AN/TSC-54 (DETAILED CIRCUIT ANALYSIS) (NSN 5895-00-937-4993)

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CHAPTER 3
DETAILED CIRCUIT ANALYSIS

Section I. COMPONENTS OF OPERATIONS CONTROL VAN

3-1. General

This chapter contains a detailed circuit analysis of Satellite Communication Terminal AN/TSC-54. Many circuit stages of the AN/TSC-54 are functionally identical, differing only in reference designation, component values, or some slight circuit configuration. For purposes of this manual, these stages are considered standard circuits and each stage type described is a fundamental or basic circuit which performs an identical or logical function and is used consistently throughout the equipment. Reference designations are arbitrarily assigned to permit component identification in the general circuit descriptions. Actual reference designations and values of components may be correlated with a particular stage shown in the applicable schematic diagram.

3-2. Zero Set Control 1A2A1

(fig. 3-1)

The zero set control of the AN/TSC-54 is essentially used to position the AZIMUTH digital readout indicators to 0 degrees when the antenna is pointed toward true north. This capability is necessary to compensate for the difference between magnetic north and true north and the difficulty encountered in some locations in aligning the antenna on a true north-south line.

a. The zero set control includes a synchro, a resolver, a toggle switch, a magnetic clutch, and a handwheel. A signal proportional to antenna position is applied from the azimuth data box resolver to stator windings S1 through S4 of resolver B2. The corrected signal is taken from rotor windings R1 through R4 of resolver B2 and applied to the azimuth followup resolver. The azimuth digital indicator display, which is positioned by the followup circuit, is thus zeroed.

b. A signal from the azimuth data box synchro, also proportional to antenna position, is applied to stator windings S1 through S3 of synchro B1. The corrected output from rotor windings R1 through R3 is applied to the azimuth position indicator, zeroing it. When power ON-OFF toggle switch S1 is in the ON position, magnetic clutch A1 is energized and the AZIMUTH INDICATOR ZERO ADJUST handwheel is engaged. Thus, any rotation of the handwheel turns the synchro and resolver to set in the necessary correction factor.

3-3. Reference Frequency Generation Equipment

(fig. 3-2 through 3-7, FO 3-1)

a. Frequency distribution unit 1A2A22 operates in conjunction with cesium beam standard 1A2A24 and distribution amplifier 1A2A33 to provide accurate, stable mixing and timing signals. The unit consists of an FE-12 frequency standard, filter FL1, coaxial switch assemblies K1, K2, and K3, two-way power divider CP3, power supply PS1, and amplifier/limiters AR1 and AR2. Figure 3-2 is provided as an aid to understanding the relationship of the elements that comprise the frequency generation equipment.

b. Amplifier/limiters AR1 and AR2 (fig. 3-3 and 3-4, respectively) are similar in design, the only difference is the frequency response. AR1 contains circuits resonant to 1 MHz, while AR2 contains circuits resonant to 5 MHz. For explanation purposes, refer to the 1 MHz amplifier/limiter schematic diagram (fig. 3-3). The positive 28 vdc operating voltage is applied at J3, is coupled by capacitor C4 to a tank circuit (C5 and L3) resonant to 1 MHz. Resistors R2 and R4 lower the Q of the tank. From both ends of the tank, signals are applied to transistor array U1. The main signal path is from the bottom of the tank to the base of Q1. Limiting occurs by increasing the emitter potential of Q1. This is accomplished by the combined action of transistors Q2, Q3, and Q4, and diodes CR1 and CR2. The parallel tank in the collector circuit of Q1 (C1 and L1) is resonant to 1 MHz. Capacitor C2 decouples the rf from the +28 vdc line. The 1 MHz signal is applied from the collector of Q1, through a series tank (L2 and C3) resonant to 1 MHz, to output connector J2. The preceding explanation is applicable to 5 MHz amplifier/limiter AR2, except that the tank circuits in that assembly are resonant to 5 MHz.

c. Distribution amplifier (fig. FO 3-1, 3-5 through 3-7) 1A2A33 accepts 1 MHz and 5 MHz signals from frequency distribution unit 1A2A22. The distribution amplifier provides multiple 1 MHz and 5 MHz outputs to major units in the AN/TSC-54. The unit consists of three sections, preamplifier assembly A5, output amplifier assemblies A8 and A9 and power supply assemblies A1 and A2.

d. The 1 MHz and 5 MHz preamplifiers (fig. 3-5) are identical in design. Inputs to preamplifier as-

sembly A5 are fed across R2, C1, and R3 to the base of emitter follower Q1. The output of Q1 is fed through coupling capacitor C3 to output connections A5 (P,R,S). A portion of the output signal is developed across R7 and rectified by CR1. The rectified output is available at A5 (1,A) and is displayed on CIRCUIT CHECK meter M1.

e. Output amplifiers A8 and A9 (fig. 3-6) are similar in design, the only difference is the frequency response which is determined by the value of capacitor C9. Input signals are applied through R1 and C1 to the base of Q1. Transistor Q1 amplifies the signal and drives emitter-follower Q2. Transistor Q2 in turn drives push-pull amplifiers Q3 and Q4. The secondary winding of transformer T1 provides the 180° phase shift needed to drive Q3. The Q3, Q4 base input circuit is tuned by T1 secondary winding and C6. Base-bias for Q3 and Q4 is derived from the forward voltage drop of CR1 (17 vdc). Resistor R13 is a dc balance adjustment for Q3 and Q4 and is used to minimize second harmonic distortion in the output signal. Output signals from Q3 and Q4 are transformer coupled through T2 to output connectors P,R,S. A portion of the output signal is developed across R14 and rectified by CR2. The rectified output is available at output connection 1,A and is displayed on CIRCUIT CHECK meter M1.

f. The power supply section is comprised of power module A1 and power supply A2 (fig. 3-7). Module A1 contains the ac input connector, 115/240 vac select switch S1 and line fuse F1. The ac input is fed through the A1 to the primary of transformer T1. The signal at the secondary of T1 is rectified by CR3 and CR5 and filtered by C1. A portion of the ac signal is developed across R2 and is used to illuminate AC OPERATION lamp DS1. The filtered dc is applied through dc blocking diodes CR4 and CR6 to the input of voltage regulator U7 (7,8) and series regulator Q1. Voltage regulator U1 initially allows Q1 to conduct. The output voltage at the junction of R3 and R4 is sensed through divider R4, 5 and 6 at U1 (2). Regulator U1 controls the voltage at the base of Q1 which controls current flow through Q1 and regulates the output voltage to the load. The voltage drop across R3 is monitored by U1 (10,1) to provide current limiting protection. When the voltage drop across R3 becomes excessive, U1 detects it and biases Q1 off. Normal operation is returned when the excessive load is removed from the power supply.

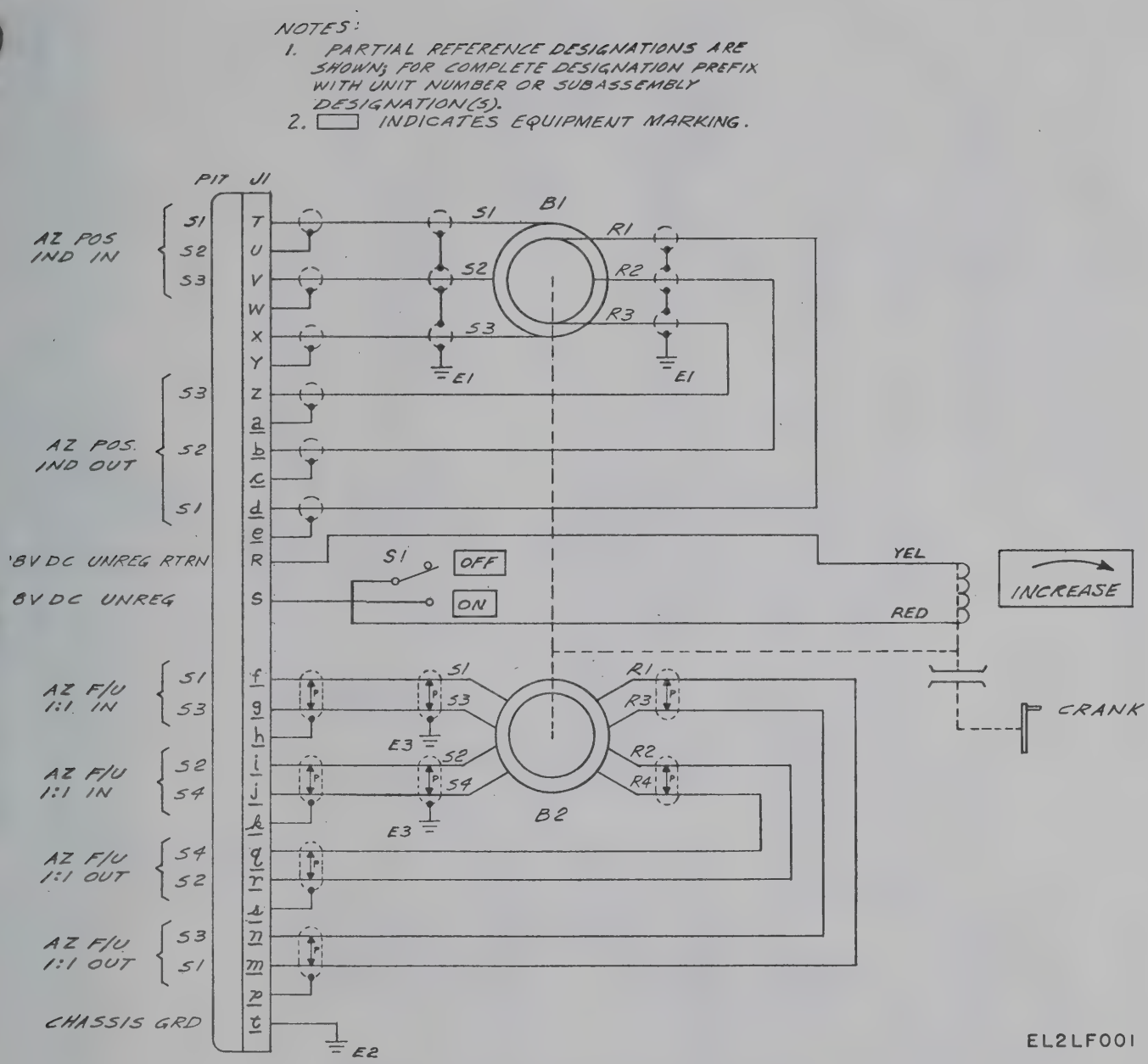


Figure 3-1. Zero set control 1A2A1, schematic diagram.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATIONS.
2. UNLESS OTHERWISE SPECIFIED, WIRE SIZE IS AWG 22 COLOR WHITE.
3. TERMINALS 1, 2 & 3 ON K1-K3 ARE FOR REF ONLY AND ARE NOT MARKED ON RELAYS.

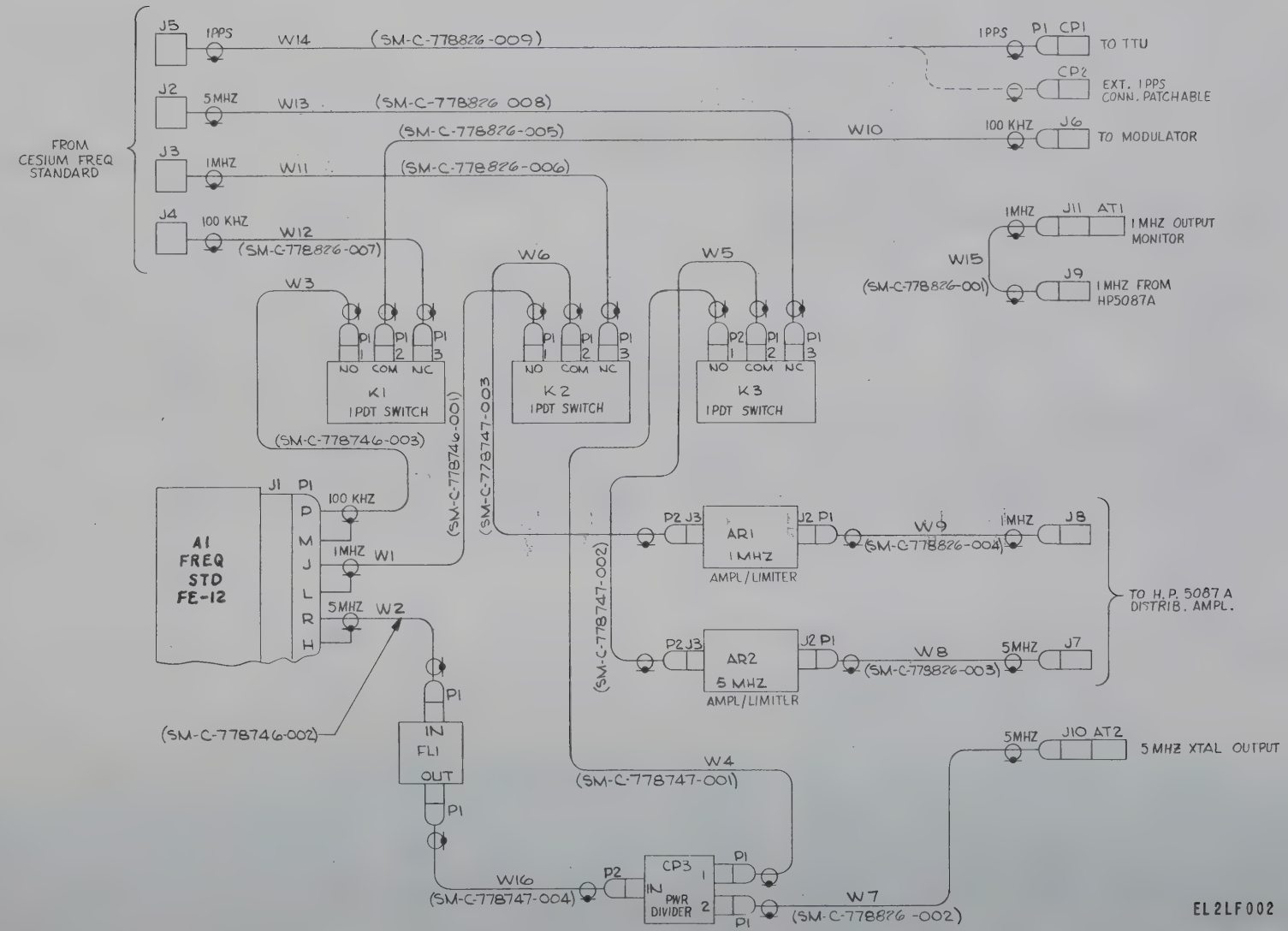


Figure 3-2. ① Frequency distribution unit 1A2A22, connection di[illegible] (sheet 1 of 2).

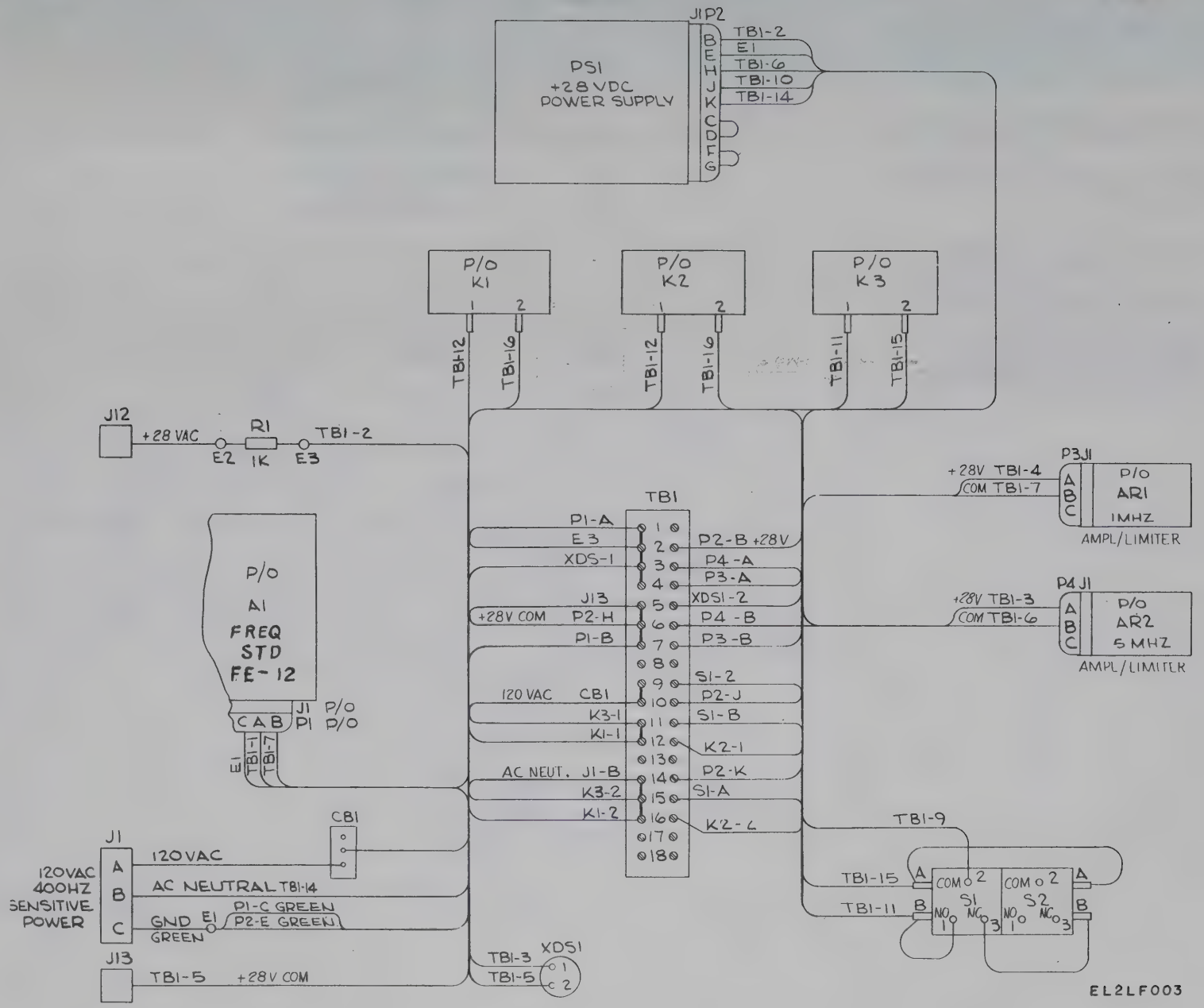
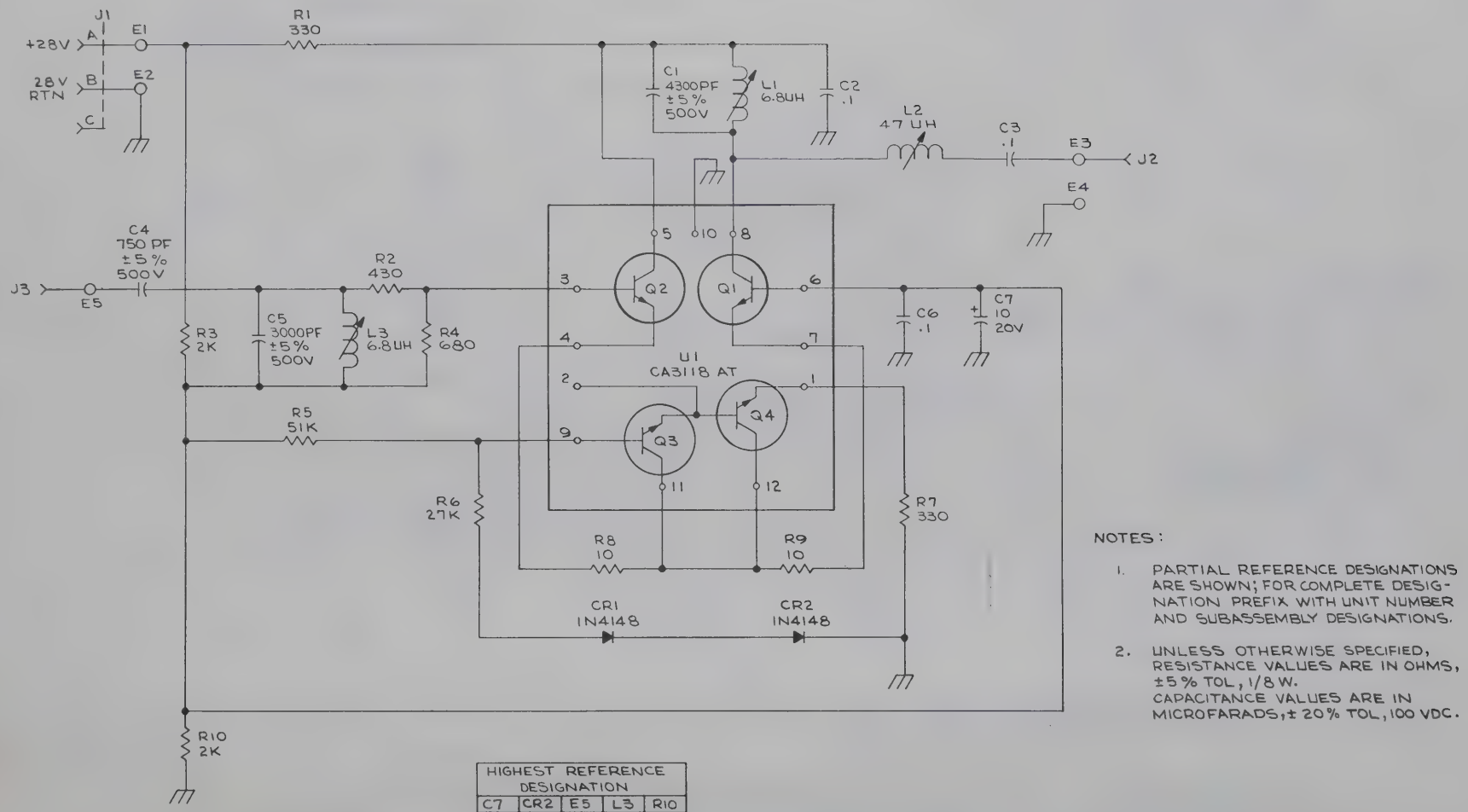


Figure 3-2.② Frequency distribution unit 1A2A22, connection diagram (sheet 2 of 2).



HIGHEST REFERENCE DESIGNATION				
C7	CR2	E5	L3	R10
U1	J3			
REFERENCE DESIGNATIONS NOT USED				

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATIONS.
2. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, ±5% TOL, 1/8 W. CAPACITANCE VALUES ARE IN MICROFARADS, ± 20% TOL, 100 VDC.

EL2LF005

Figure 3-3. 1 MHz amplifier/limiter 1A2A22AR1, schematic diagram.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATIONS.
2. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, ±5% TOL, 1/8 W. CAPACITANCE VALUES ARE IN MICROFARADS, ± 10% TOL, 100 VDC.

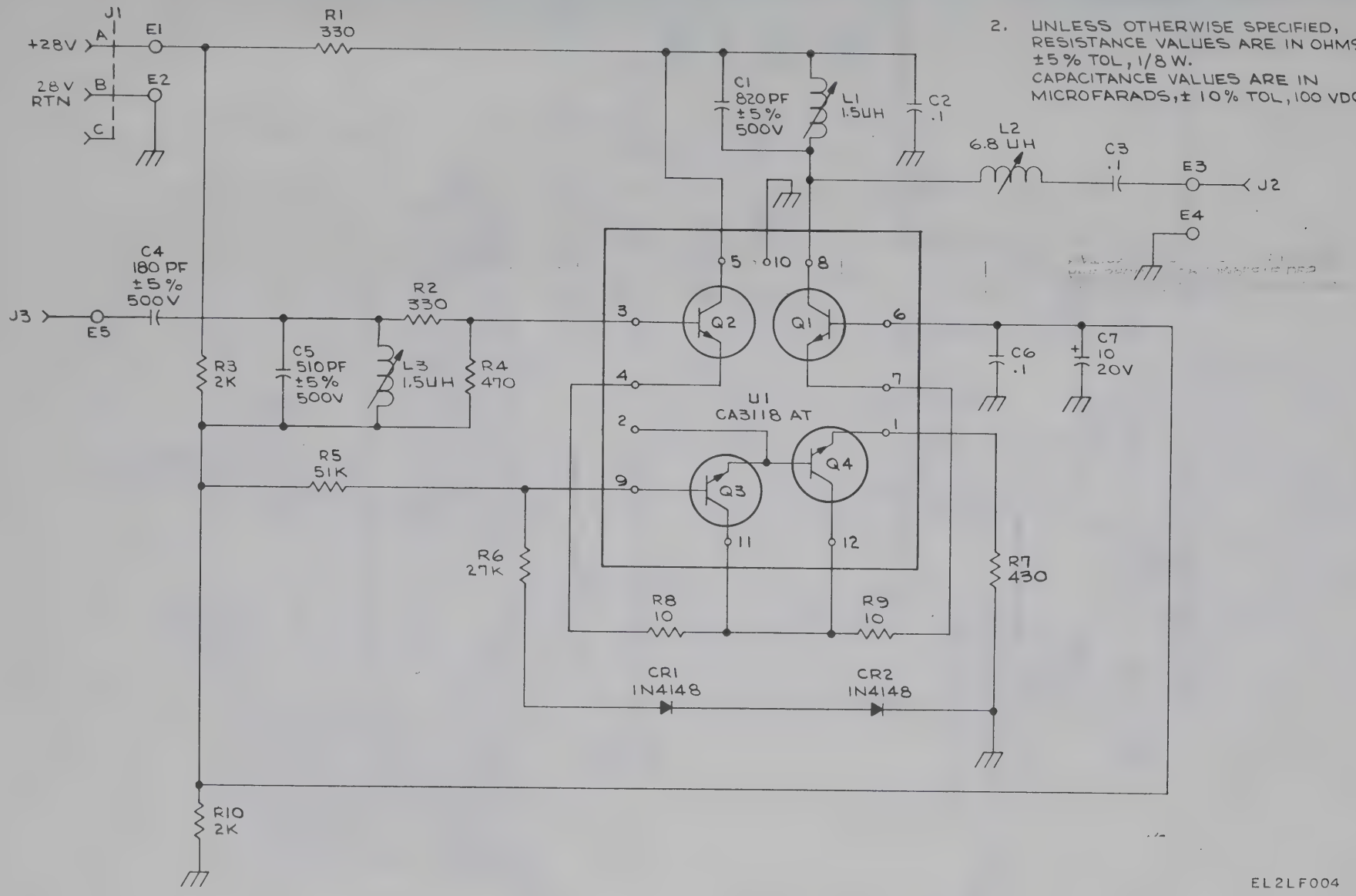
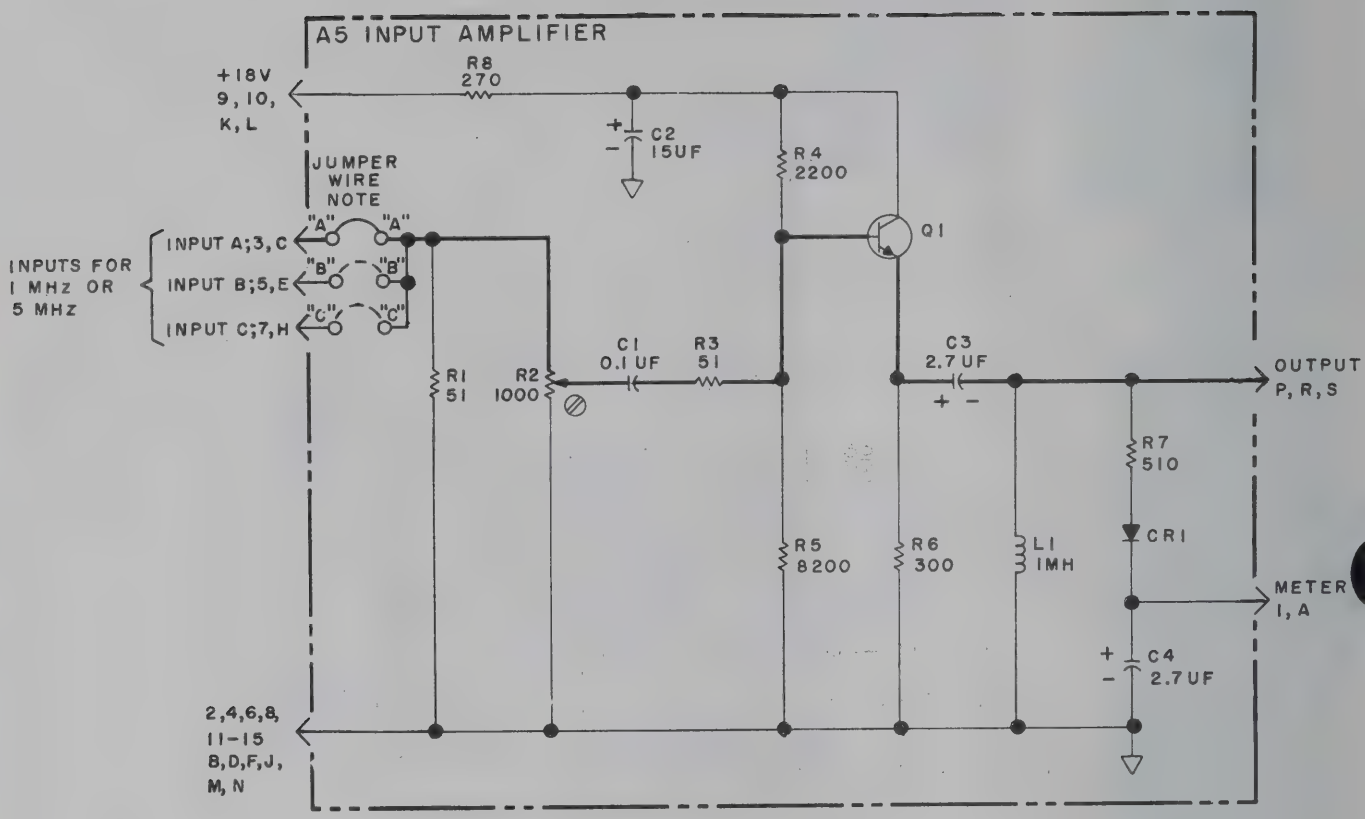


Figure 3-4. 5 MHz amplifier/limiter 1A2A22AR2, schematic diagram.



NOTES:

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN PF, INDUCTANCES ARE IN MH.
2. JUMPER WIRE FOR SELECTING INPUT SIGNAL SOURCE CONNECTION DEPENDS ON INPUT SOCKET IN WHICH BOARD IS INSTALLED AND DESIRED SIGNAL SOURCE CONNECTION SHOWN IS FOR USE IN SOCKET A WITH INPUT FROM INPUT JACK J1 (INPUT A).

EL2LF007

Figure 3-5. Preamplifier 1A2A33A5, schematic diagram.

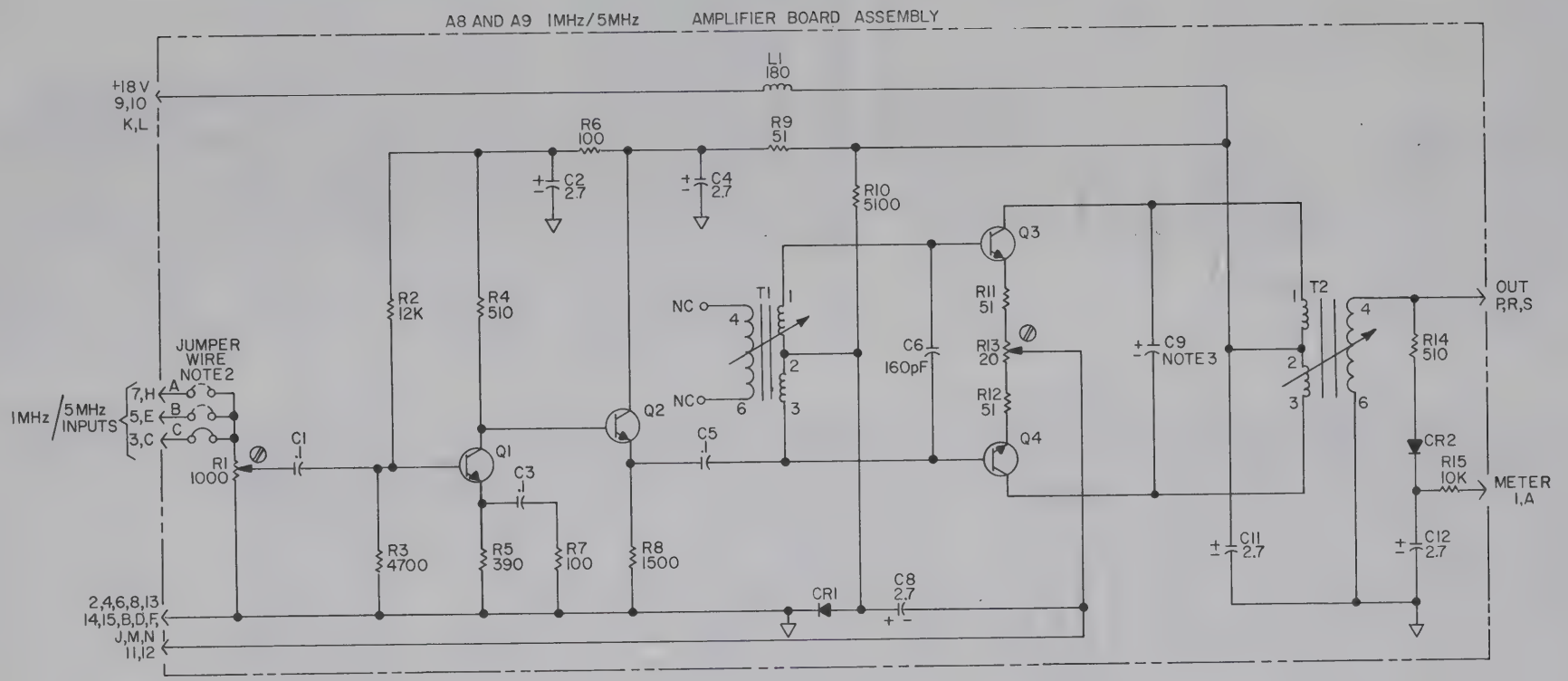


Figure 3-6. Output amplifier 1A2A33A8, schematic diagram.

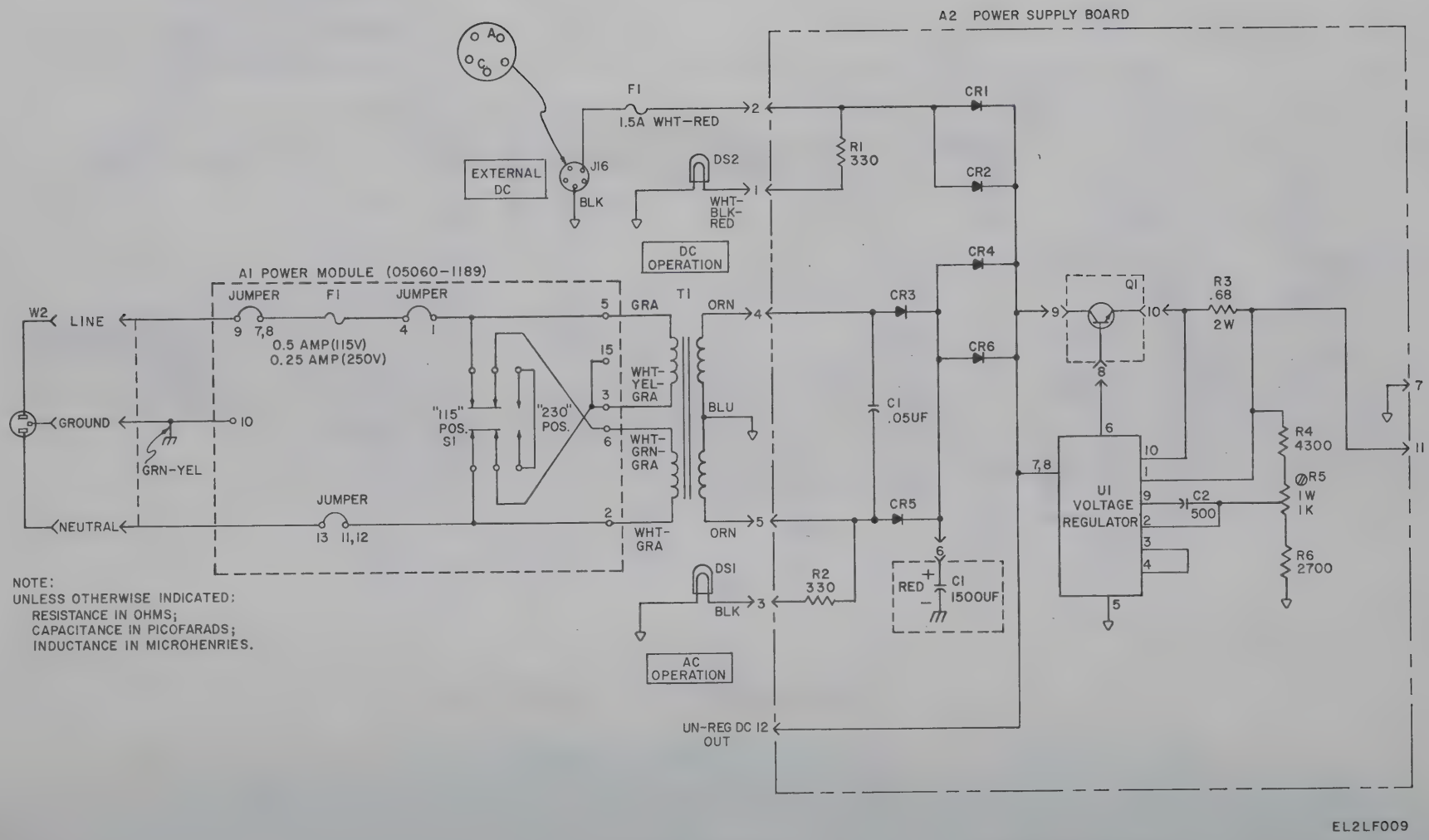


Figure 3-7. Power section 1A2A33A1 and 1A2A33A2, schematic diagram.

3-4. Power Supply Circuit Analysis

The input and output signal characteristics for +28 vdc power supply pS1, +200 vdc power supply PS2, and +5 vdc power supply PS3 are illustrated in figure 3-8.

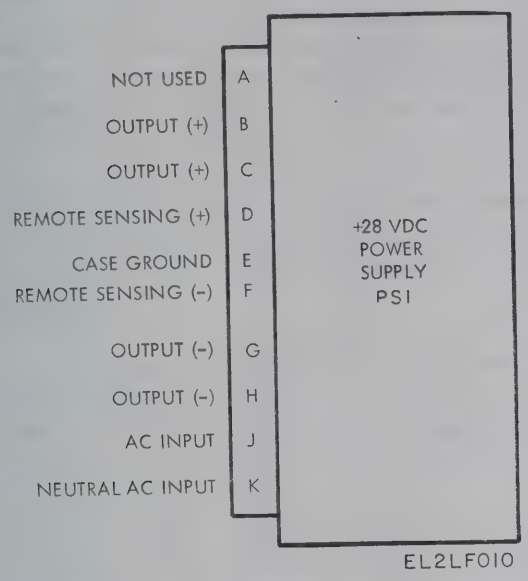


Figure 3-8. Plus 28 vdc power supply PS1, input/output signal characteristics.

3-5. Power Distribution Panel 1A2A4 Components

(fig. FO 3-2 and 3-9)

Power distribution panel 1A2A4 contains five power supplies which provide positive and negative regulated voltages for the AN/TSC-54. All power supplies operate the same way, except component values are changed to develop a lower output voltage. Only the two +28 vdc power supplies are discussed.

a. Positive 28 vdc power supply PS1 contains a 3-phase, 120/208 vac input transformer having a Y-connected primary and two secondary windings, two full-wave bridge rectifiers, and a regulation and sensing network. One secondary winding on transformer T101, a Y-connected stepdown winding, is connected to a full-wave bridge rectifier consisting of diodes CR101 through CR106. The full-wave bridge rectifier develops an output voltage across capacitor C101. Transistors Q101 and Q102 provide series regulation of the output voltage.

b. The other secondary winding on transformer T101 is connected to a full-wave bridge rectifier consisting of diodes CR1, CR2, CR3, and CR4. The full-wave bridge rectifier develops a voltage across capacitor C1, which provides bias for transistors Q1 through Q6. When the output voltage rises the potential on the base of transistor Q3 becomes more positive. Transistor Q3 conducts more heavily through resistor R7 driving the emitter of transistor Q2 more positive. Transistor Q2 conducts less through collector load resistor R5 and drives the base of transistor Q4 more positive. Transistor Q4 conducts less through resistor R13 decreasing the positive potential on the base of transistor Q6. Transistor Q6 conducts less through resistor R15 reducing the positive potential on the base of transistor Q7. Transistor Q7 conducts less through resistor R14 lowering the positive potential on the base of transistors Q101 and Q102. As transistors Q101 and Q102 conduct less, the voltage drop across them increases and returns the output voltage to the regulated value.

c. When the output voltage decreases, the potential on the base of transistor Q3 becomes less positive. Transistor Q3 now conducts less through resistor R7 driving the emitter of transistor Q2 less positive. Transistor Q2 conducts more heavily through collector load resistor R5 driving the base of transistor Q4 more negative. Transistor Q4 conducts more heavily through resistor R13 causing an increase in the positive potential on the base of transistor Q6. Transistor Q6 conducts more heavily through resistor R15 increasing the positive potential on the base of transistor Q7. Transistor Q7 conducts more heavily through resistor R14 increasing the positive potential on the base of series regulator transistors Q101 and Q102. As transistors Q101 and Q102 conduct more heavily, the voltage drop across them decreases and returns the output voltage to the regulated value.

d. Power distribution panel A4 contains 5 vdc Zener diode CR1 which receives +10 vdc from power supply PS3 through TB2-10. Zener diode CR1 supplies +5 vdc through J3-R to J10-A of antenna control 1A2A5. The +5 vdc is used by the scan generator logic circuits.

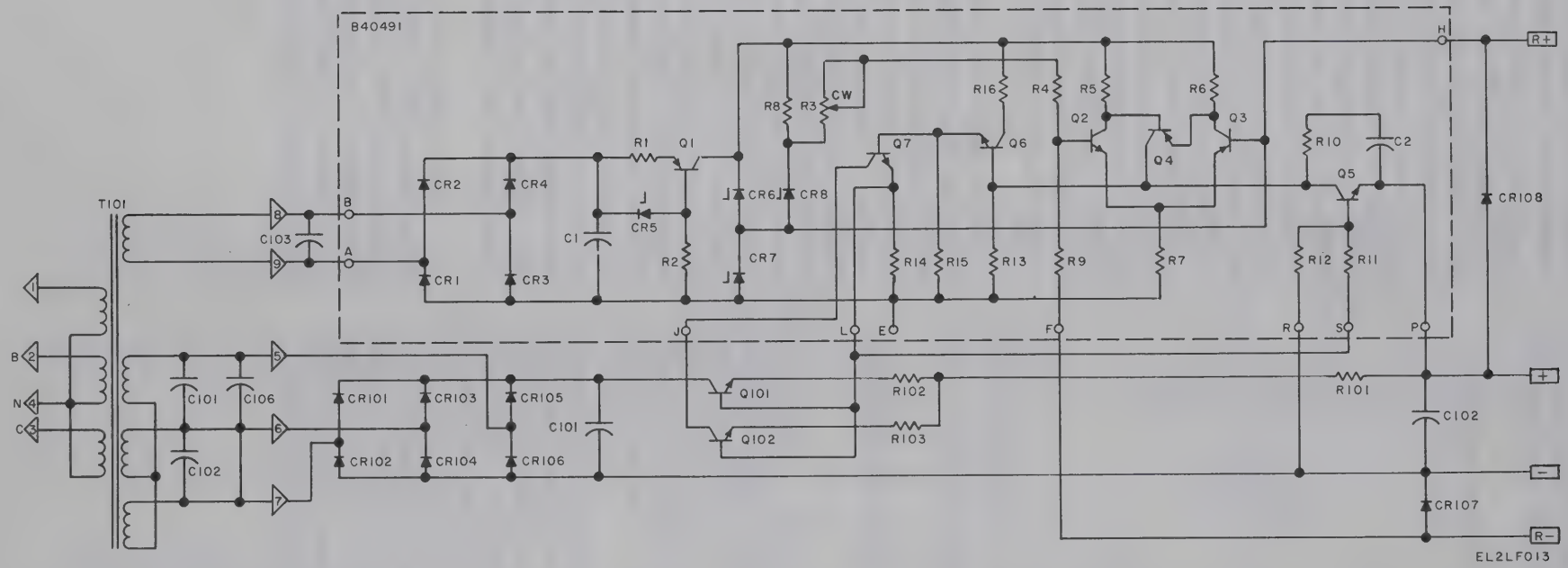


Figure 3-9. Typical +28 vdc/+10 vdc power supply, schematic diagram.

3-6. Plus 28 Vdc Regulated Power Supply PS5 Circuit Analysis

(fig. FO 3-3)

a. The positive 28 vdc power supply PS5 contains a 3-phase, 120/208 vac input transformer having a Y-connected primary and two secondary windings, two full-wave bridge rectifiers and a regulation and sensing network. One secondary winding on input transformer T101, a delta-connected step-down winding, is connected to a full-wave bridge rectifier consisting of diodes CR101 through CR106. The full-wave bridge rectifier develops an output voltage across capacitor C101. Transistor Q102 through Q106 provide series regulation of the output voltage.

b. The other secondary winding on transformer T101 is connected to a full-wave bridge rectifier consisting of diodes CR1, CR2, CR3 and CR4. The full-wave bridge rectifier develops a voltage across capacitor C1 which is used to provide bias for transistors S1 through Q4.

c. When the output voltage rises, the potential on the base of transistor Q3 becomes more positive. Transistor Q3 conducts more heavily through resistor R7 driving the emitter of transistor Q2 more positive. Transistor Q2 conducts less through collector load resistor R5 increasing the potential on the base of transistor Q4. Transistor Q4 conducts less through resistor R13 decreasing the positive potential on the base of transistor Q6. Transistor Q6 conducts less through resistor R15 decreasing the positive voltage on the base of transistor Q7. Transistor Q7 conducts less through resistor R14 decreasing the positive potential on the base of transistor Q101. Transistor Q101 conducts less through resistor R103 which decreases the positive potential on the base of transistors Q102 through Q106. As transistors Q102 through Q106 conduct less, the voltage drop across them increases and returns the output voltage to the regulated value.

d. When the output voltage decreases, the potential on the base of transistor Q3 decreases. Transistor Q3 now conducts less through resistor R7 and this reduces the positive voltage on the emitter of transistor Q2. Transistor Q2 conducts more heavily through collector load resistor R5 driving the base of transistor Q4 more negative. Transistor Q4 conducts more heavily through resistor R13 increasing the positive potential on the base of transistor Q6. Transistor Q6 conducts more heavily through resistor R15 increasing the positive potential on the base of transistor Q7. Transistor Q7 conducts more heavily through resistor R14 increasing the positive potential on the base of transistor Q101. Transistor Q101 conducts more heavily through resistor R103 increasing the positive potentials on the base of transistors Q102 through Q106. As transistors Q102 through Q106 conduct more heavily, the voltage drop across them decreases and returns the output to the regulated value.

3-7. Antenna Control Panel 1A2A5 Circuit Analysis

(fig. 3-10 through 3-14 and FO 3-4 through FO 3-8)

Antenna control panel 1A2A5 contains the circuitry (*a* through *d* below) used to control the positioning of the antenna.

a. Scan generator A20 (fig. FO 3-5) produces signals for synchronizing the tracking error signal with the modulation taking place in the ferrite scanner.

b. Upper module board A23 (fig. FO 3-7 and FO 3-8) is a hinged assembly mounted on the top of the chassis of the antenna control panel and contains electrical receptacles into which modules and cable connectors are plugged.

(1) The relay driver (fig. 3-11) is used to provide a low driving impedance to energize relays. In the static state, with all of the diode coupled inputs connected to a minimum of +5.0 vdc or open, and the "OR" input is open, current flows from the +10 vdc voltage source through resistor R1, and diodes CR3 and CR4 to the base of transistor Q1; a small amount of current also flows through resistor R3 to the -10.0 vdc source. The current in the base of transistor Q1 causes it to conduct into a saturated state. The voltage at the collector of transistor Q1 will be approximately +0.4 vdc. A small amount of current will flow through diode CR1 and resistor R4 to the -10.0 vdc source and the voltage drop across diode CR1 will be approximately 0.5 vdc (this causes the cathode of diode CR1 to be a -0.1 vdc). The -0.1 vdc level on the base of transistor Q2, reverse biases the transistor and holds it in the off state.

(2) If any of the inputs, including the "OR" input, are connected to ground, the current that was flowing into the base of transistor Q1 ((1) above) flows to ground through the grounded input and a small amount of current flows through diodes CR3 and CR4 and resistor R3 to the -10.0 vdc source (causing a voltage drop across diodes CR3 and CR4 of approximately 1.0 vdc). The anode of diode CR3 will be approximately +0.5 vdc or zero volt if the "OR" input is grounded, and the cathode of diode CR4 will be at -0.5 vdc or -1.0 vdc. The -0.5 or -1.0 vdc is also applied on the base of transistor Q1, which reverse biases the transistor holding it in the off state. The current that was flowing through transistor Q1 will now flow through diode CR1 into the base of transistor Q2 causing it to become saturated. Its collector will be at approximately +0.4 volts.

c. Servo operational amplifier A3 (fig. 3-12) consists of a dc amplifier, a voltage divider, and feedback capacitors. The voltage divider contains a potentiometer which provides adjustment of the bias, to obtain a zero voltage offset on the output. The dc amplifier has the capability of providing an inverted or noninverted output. This is controlled by the application of the input signal to either pin 2 or 3.

(1) Dc amplifier AR1 (fig. 3-13) contains dual field effect transistor Q5 as the input stage, to provide isolation and drift stabilization. Transistor Q6 acts as a common constant current source for transistor Q5. Transistor Q1 is an inverter which drives field effect transistor Q2. The output from source follower Q2 is fed into emitter follower Q3 which drives the common base amplifier stage Q4. The collector of transistor Q4 is the output.

(2) Dc bias and stabilization is obtained by feedback to the constant current source transistor Q6. Capacitors C1 and C2 provide frequency rolloff, so the circuit will not oscillate.

d. Gate expander A27 (fig. 3-14) consists of a 3-input diode gate, and a 2-input diode gate. These gates can be used in an AND or an OR configuration, and are also used to provide additional inputs to transistor logic gates.

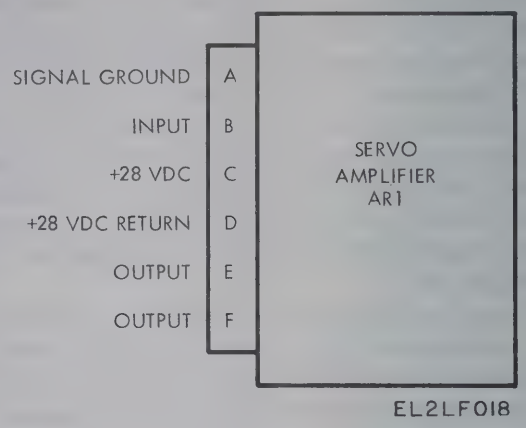


Figure 3-10. Servo amplifier AR1, input/output signal characteristics.

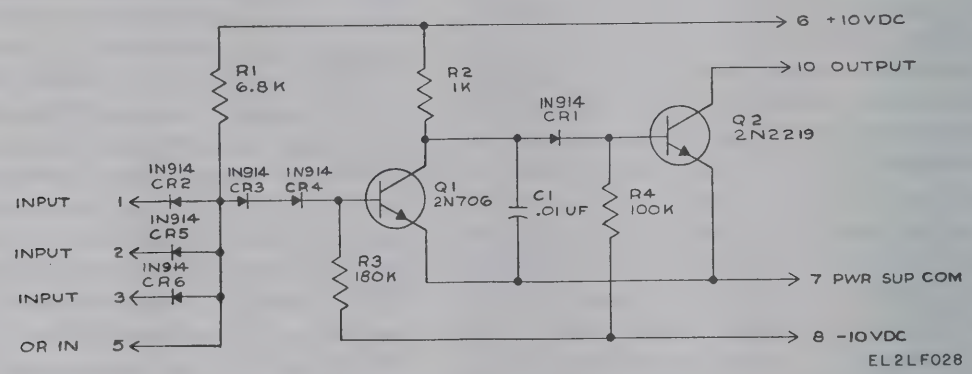


Figure 3-11. Relay driver, schematic diagram.

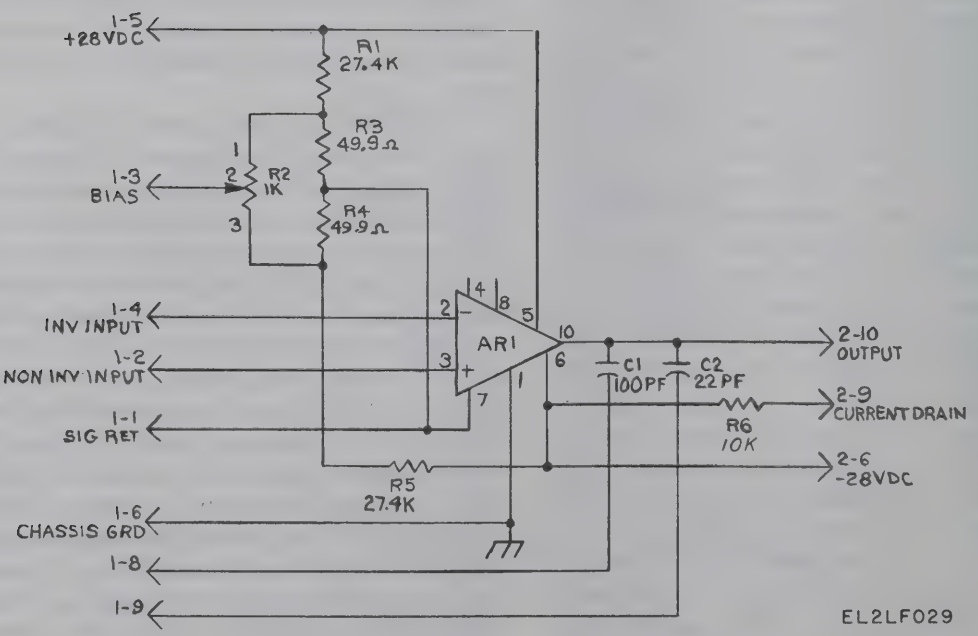


Figure 3-12. Servo operational amplifier A3, schematic diagram.

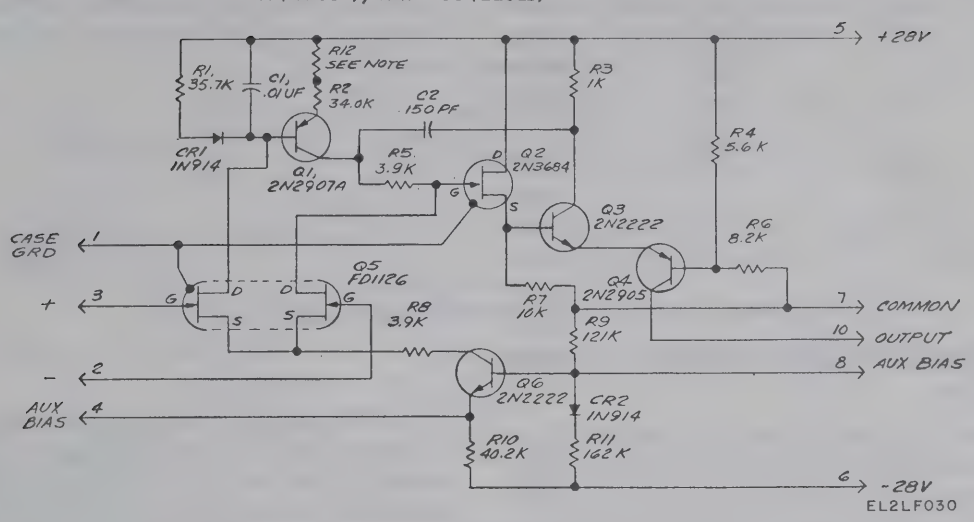


Figure 3-13. Dc amplifier AR1, schematic diagram.

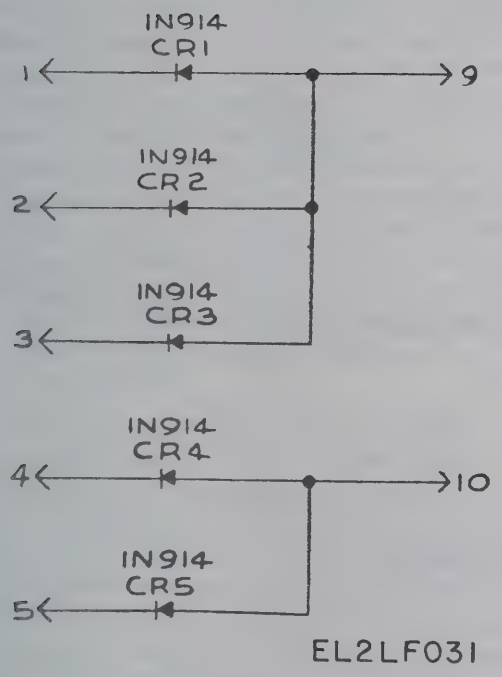


Figure 3-14. Gate expander 1A2A5A23A27, schematic diagram.

3-8. Dual NAND Gate A28 and NAND Gate A29 Circuit Analysis

(fig. 3-15 and 3-16)

a. In the static state of the 3-input NAND gate, with all three of the inputs connected to a voltage level of +5 vdc or more, or open, current flows from the +10 vdc voltage source at pin 6, through resistor R1 and diodes CR3 and CR4 to the base of transistor Q1. This current flow into the base of transistor Q1 causes Q1 to be in a saturated state, and its collector (pin 9) will be approximately -0.4 vdc above ground. A small amount of current also flows through resistor R3 to the -10 vdc source. When any one of the three inputs is connected to ground, the current that was flowing into the base of transistor Q1 will flow through the diode that is grounded.

b. A small amount of current will continue to flow through resistor R3 (*a* above), but the anode of diode CR3 is at a +0.5 vdc level, and the voltage drop across diodes CR3 and CR4 will be approximately 1.0 vdc. This causes the base of transistor Q1 to become back-biased and transistor Q1 will be in an off-state. When transistor Q1 is cut off, its collector (pin 9) will be at the +10 vdc level. The other NAND gate operates the same way, except that it has two inputs rather than three.

c. The NAND gate performs exactly the same as the dual NAND gate described in *a* and *b* above, except it has five inputs and an OR input (fig. 3-16). The OR input causes the circuit to perform the same as the other inputs, except it is either open or grounded.

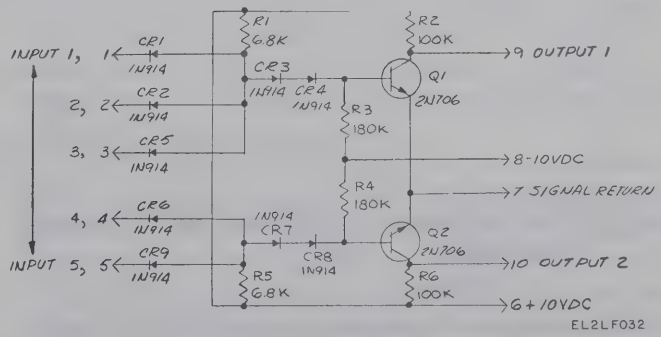


Figure 3-15. Dual NAND gate 1A2A5A23A28, schematic diagram.

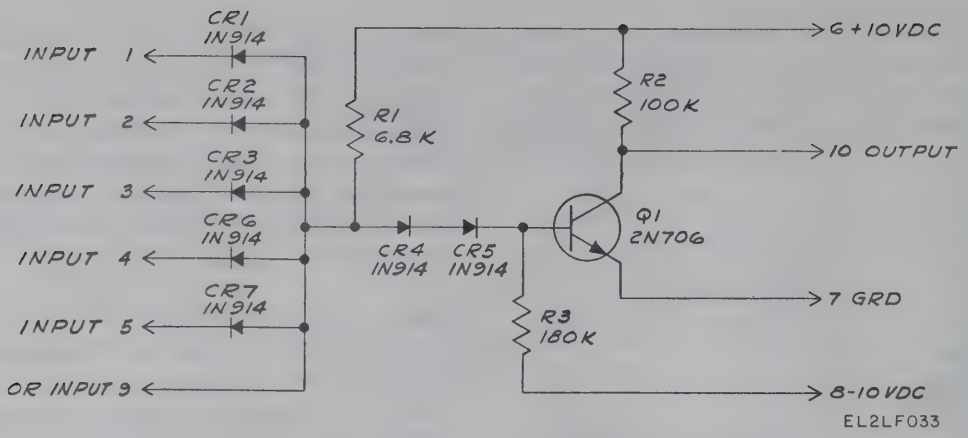


Figure 3-16. NAND gate 1A2A5A23A29, schematic diagram.

3-9. NAND Gate Driver A31 Circuit Analysis

(fig. 3-17)

a. In the static state with the diode coupled input connected to a minimum of +5.0 vdc or open, current flows from the +10 vdc source through R1, CR2 and CR3 into the base of Q1; and a small amount of current flows through resistor R4 to the -10 vdc voltage source. The current flowing into the base of transistor Q1 causes it to be in a saturated state. The voltage at the collector of transistor Q1 will be approximately +0.4 vdc. A small amount of current will also flow through diode CR4 and resistor R5 to the -10 vdc source and the voltage drop across diode CR4 will be approximately 0.5 vdc. This causes the cathode of diode CR4 to be at -0.1 vdc. The -0.1 vdc level on the base of transistor Q2, reverse biases the transistor holding it in the off-state, and current will not flow.

b. If the input is connected to ground, the current that was flowing into the base of transistor Q1 (*a* above) flows to ground through diode CR1 and a small amount of current also flows through diodes CR2 and CR3, and resistor R4 to the -10 vdc source. This causes a voltage drop across diodes CR2 and CR3 of approximately 1.0 vdc. The anode of diode CR2 will be approximately +0.5 vdc and the cathode of diode CR3 will be at -0.5 vdc. The -0.5 vdc is also on the base of transistor Q1, which reverse biases the transistor holding it in the off-state, and current will not flow through it. The current that was flowing through transistor Q1 will now flow through diode CR4 into the base of transistor Q2 causing it to become saturated. Its collector will be at approximately +0.4 vdc.

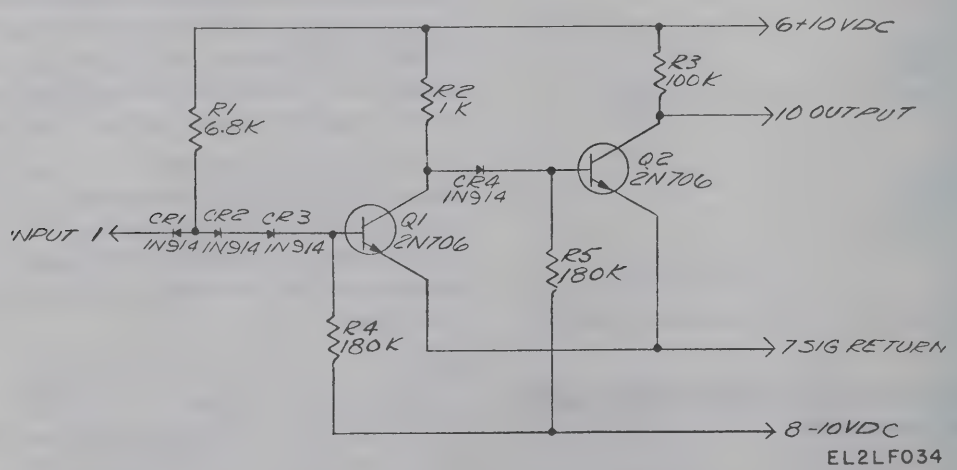


Figure 3-17. NAND gate driver 1A2A5A23A31, schematic diagram.

3-10. Operational Amplifier A61 Circuit Analysis

(fig. 3-18)

a. The inputs to operational amplifier A61 are to differential connected stages consisting of transistors Q4A and Q4B. The emitters of transistors Q4A and Q4B are connected to constant current source transistor Q5. The collector of transistor Q4B drives the base of transistor Q1, and the collector of transistor Q1 is connected to the collector of transistor Q4A. The two collectors are in phase with each other in order to achieve a very large voltage gain in this portion of the amplifier. The collectors

of transistors Q1 and Q4A drive into the base of transistor Q2.

b. The output from the emitter of transistor Q2 is applied to Zener diode CR2 and to the base of constant current source transistor Q5, through resistor R14. This produces an operating point feedback and prevents the amplifier from drifting. The output from the collector of transistor Q2 is applied to the base of transistor Q3, which is the output stage of the amplifier. The collector of transistor Q3 is connected to the output through a 330-ohm current limiting resistor.

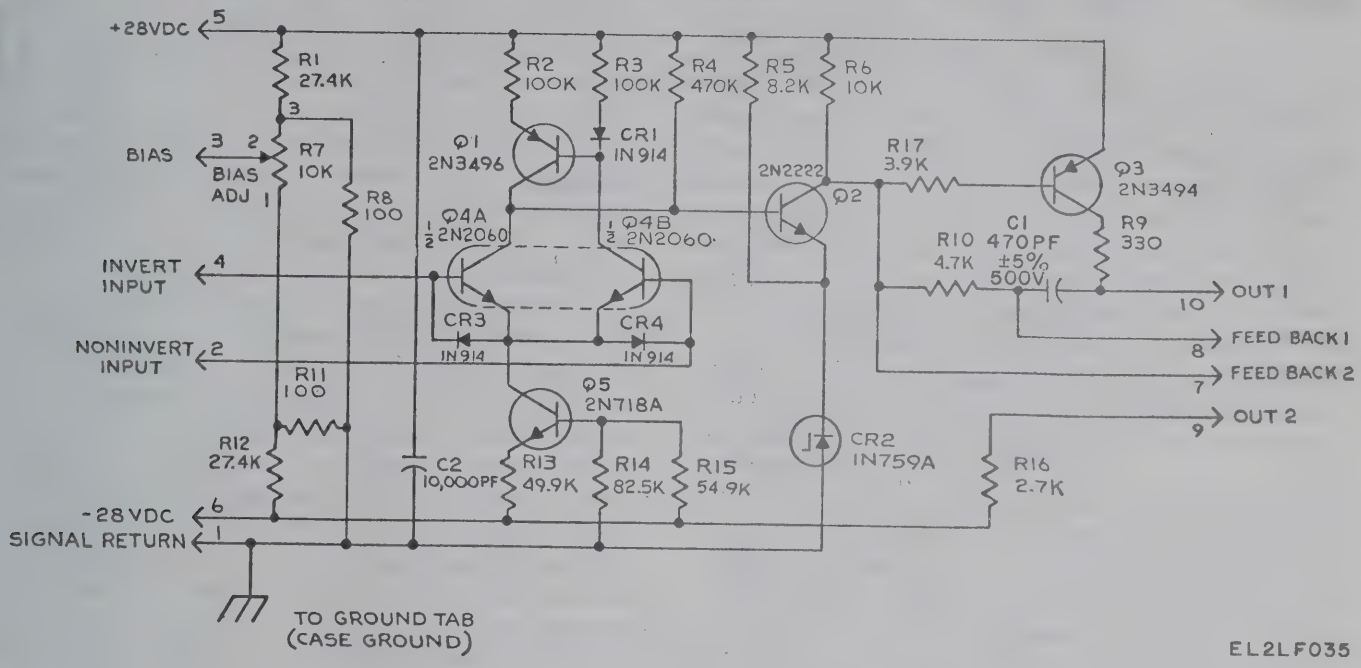


Figure 3-18. Operational amplifier 1A2A5A23A61, schematic diagram.

3-11. Level Shifter A63, Dual Low Level Switch A76 Circuit Analysis

(fig. 3-19)

a. When a high is present at the input of level shifter A63, diode CR2 is reverse-biased. Under this condition, current flows through the voltage divider consisting of resistors R4 and R1, and diodes CR3 and CR4. Transistor Q1 is forward-biased and current flows through collector load resistor R2. The decrease in voltage at the collector of transistor Q1 causes a decrease in voltage at the base of transistor Q2. Transistor Q2 is forward-biased, and is driven into saturation. The increased current flow through collector load resistor R5 causes the output voltage at pin 10 to be zero.

b. When a low is present at the input of level shifter A63, diode CR2 is forward-biased. Current flows through diode CR2 and resistor R1. This places a reverse bias on the base of transistor Q1 and transistor Q1 is cut off. Since no current is flowing through collector load resistor R2, the rise in voltage at the collector of transistor Q1 is applied through resistor R3 to the base of transistor Q2. This places a reverse bias on transistor Q2, and it is driven into cutoff. With no current flowing through collector load resistor R5, the output voltage at pin 10 drops to the negative potential at pin 6.

c. Dual low level switch A76 (fig. 3-20) contains two tetrode transistor Q1 and A2. Although the transistors are connected to a common power source at pin 6, and a common reference level at pins 1 and 8, they operate identically as individual switches. For purposes of this manual, only transistor Q1 is discussed.

(1) An input signal is applied to pin 2 and a trigger signal is applied to the anode of diode CR1. The trigger signal controls the gating action of the transistor. If the trigger signal represents a high, diode CR1 conducts and current flows through base bias resistor R2. Transistor Q1 is reverse-biased, and emitters E1 and E2 are virtually an open circuit. The input signal is coupled through resistor R1 to output pin 10.

(2) When a low level signal is present at pin 7, diode CR1 is reverse-biased, and the base of transistor Q1 rises to the negative potential at pin 6. This places a forward bias on transistor Q1, and emitters E1 and E2 are effectively shorted together. Pin 10 is placed at the reference level, and the input signal at pin 2 is dissipated across resistor R1.

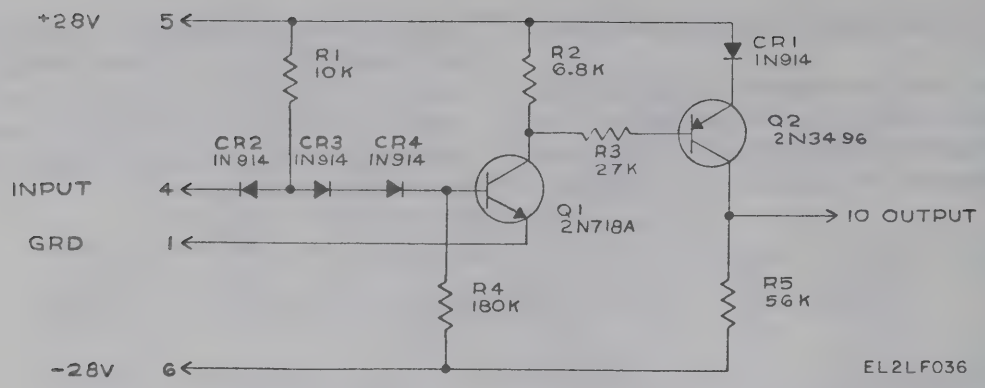


Figure 3-19. Level shifter 1A2A5A23A63, schematic diagram.

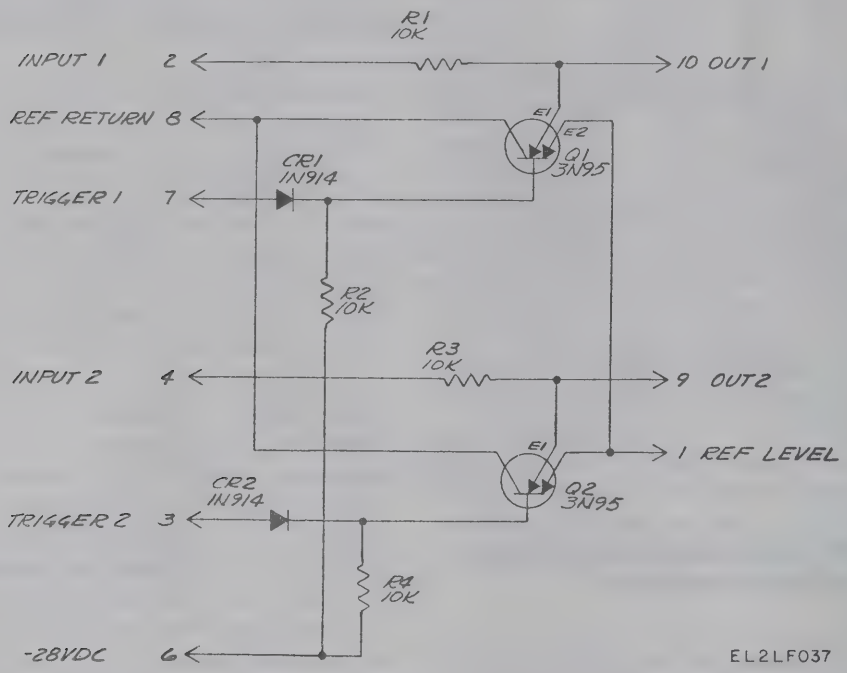


Figure 3-20. Dual low level switch 1A2A5A23A76, schematic diagram.

3-12. Lower Module Board 1A2A5A24 Circuit Analysis

(fig. 3-21 through 3-24 and FO 3-9)

Lower module board A24 is a hinged assembly mounted on the bottom of the chassis of antenna control panel 1A2A5 and contains electrical receptacles into which modules and cable connectors are plugged.

a. Shaping circuit A24A1 (fig. 3-21) provides two square-wave outputs 180° out-of-phase with each other. The circuit contains two dual transistors, Q1 and Q2, and two signal transistors, Q3 and Q4. Their function is described in (1) through (4) below.

(1) On the positive portion of the sinewave input, diode CR 3 conducts and limiting action occurs across resistor R1. Transistor Q1A becomes forward-biased and causes an increase in current flow-through emitter resistor R3 and collector load resistor R11. The decrease in voltage at the collector of transistor Q1A is directly coupled to amplifier Q2B. The increase in current flow-through emitter resistor R3, reverse biases transistor Q1B and causes an increase in the collector voltage of Q1B. This increase in voltage is directly coupled to the base of amplifier Q2A.

(2) Amplifier Q2A is now forward-biased and amplifier Q2B is reverse-biased. This results in an increase in voltage at the collector of amplifier Q2B and a decrease in voltage at the collector of amplifier Q2A. These outputs are directly coupled to the base of amplifiers Q3 and Q4. The increase in voltage at the base of amplifier Q3 causes an increase in reverse bias on amplifier Q3. The decrease in voltage at the base of amplifier Q4 causes an increase in forward bias on amplifier Q4. Under these conditions, current flow decreases through amplifier Q3, and increases through amplifier Q4.

The inverted output at pin 9 is taken across collector load resistor R5, and the noninverted output at pin 10 is taken across collector load resistor R6.

(3) During the negative portion of the sinewave input, diodes CR1 and CR2 conduct, and limiting occurs across resistor R1. Transistor Q1A becomes reverse-biased and causes a decrease in current flow through emitter resistor R3 and collector load resistor R11. The increase in voltage at the collector of transistor Q1A is directly coupled to amplifier Q2B. The decrease in current flow-through emitter resistor R3 forward biases transistor Q1B and causes a decrease in the collector voltage of Q1B. This decrease in voltage is directly coupled to the base of amplifier A2A.

(4) Amplifier Q2A is now reverse-biased and amplifier Q2B is forward biased. This results in an increase in voltage at the collector of amplifier Q2A and a decrease in voltage at the collector of amplifier Q2B. These outputs are directly coupled to the base of amplifiers Q3 and Q4. The decrease in voltage at the base of amplifier Q3 causes an increase in forward bias on Q3. The increase in voltage on the base of amplifier Q4 causes an increase in reverse bias on Q4. Under these conditions, current flow increases through amplifier Q3, and decreases through amplifier Q4. This action completes the cycle to convert the sinewave input to a square-wave output.

b. Line driver A24A44 (fig. 3-22) is a two-stage amplifier consisting of transistors Q1 and Q2 which, in the static state, are cutoff. The signal may be applied at either pin 2 or 4. Pin 4 provides a coupling capacitor C1 which blocks dc levels from the preceding circuit. Pin 2 is directly coupled to the base of amplifier Q1, and is normally used when the preceding circuit contains a coupling capacitor or is at a zero reference level.

(1) Amplifier Q1 is biased at cutoff by a voltage divider network consisting of resistor R4 and diode CR2. A positive input signal forward biases transistor Q1 and allows current to flow through collector load resistor R1. This causes a decrease in voltage at the collector of transistor Q1, which is directly coupled to the base of transistor Q2 through resistor R2.

(2) Transistor Q2 is a common emitter amplifier and its emitter is held at a constant reference level by breakdown diode CR1. The decrease in voltage on the base of amplifier Q2 increases the forward bias on the stage and allows it to conduct. Current flowing through collector load resistor R3 produces a positive signal in phase with the input signal.

c. Impedance amplifier A24A45 (fig. 3-23) is a single stage emitter follower. The output is taken across emitter resistor R3. Capacitor C1 provides degenerative feedback which improves the linearity and stabilization of the emitter follower.

d. Variable time delay A24A47 (fig. 3-24) consists of three transistor stages. During the static state, amplifier Q1 is forward-biased. Since amplifier Q1 is conducting, its collector voltage is low and there is no charge across capacitor C1. Therefore, the emitter voltage of unijunction transistor Q2 is low and it is cutoff. With no current flowing through unijunction transistor Q2 into the base of transistor Q3, Q3 will be cutoff.

(1) When a negative pulse is present at the input (pin 4), diode CR1 is forward-biased, and the current that was flowing into the base of transistor Q1 now flows through diode CR1 to ground. Transistor Q1 is now reverse-biased and it cuts off. The collector voltage of amplifier Q1 attempts to rise but is limited by the charging current of capacitor C1. Capacitor C1 starts to charge through potentiometer R1 and resistor R3. The time constant is determined by the setting of potentiometer R1.

(2) When capacitor C1 charges to a sufficient level to fire unijunction transistor Q2, current flows through base resistor R7 and a positive voltage is developed at the base of amplifier Q3. Transistor Q3 conducts through collector load resistor R5 causing the output voltage at pin 10 to decrease. The start of the output pulse was delayed from the start of the negative input pulse until capacitor C1 charged sufficiently to fire unijunction transistor Q2. At the end of the negative input signal, amplifier Q1 returns to the static state and starts to conduct. Capacitor C1 discharges through amplifier Q1 and unijunction transistor Q2 returns to cutoff, terminating the output pulse.

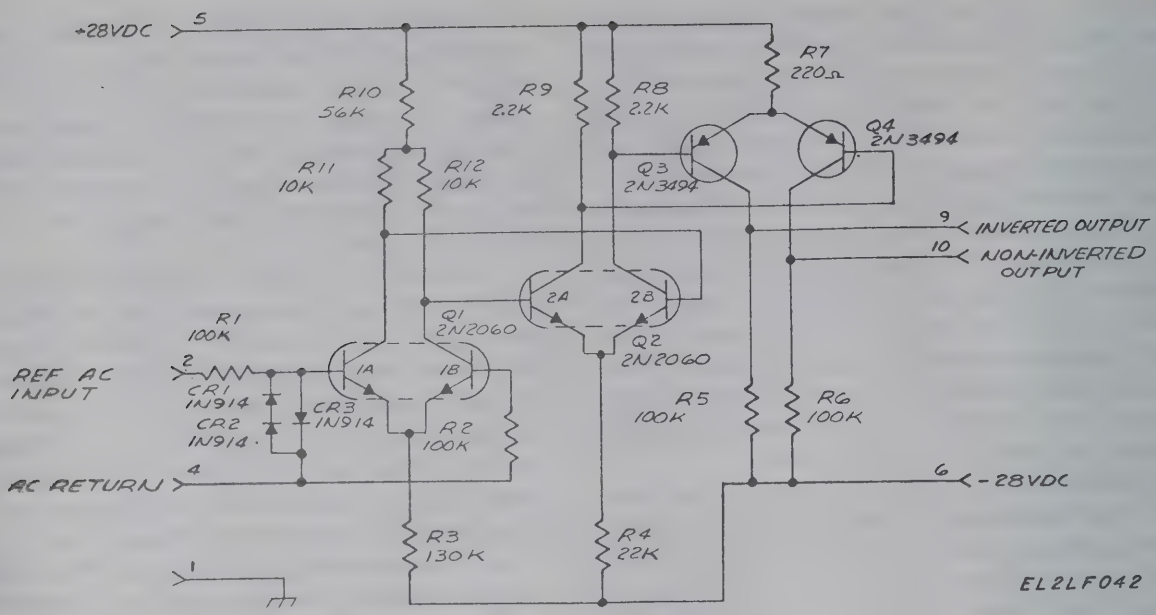


Figure 3-21. 70 MHz shaping circuit 1A2A5A24A1, schematic diagram.

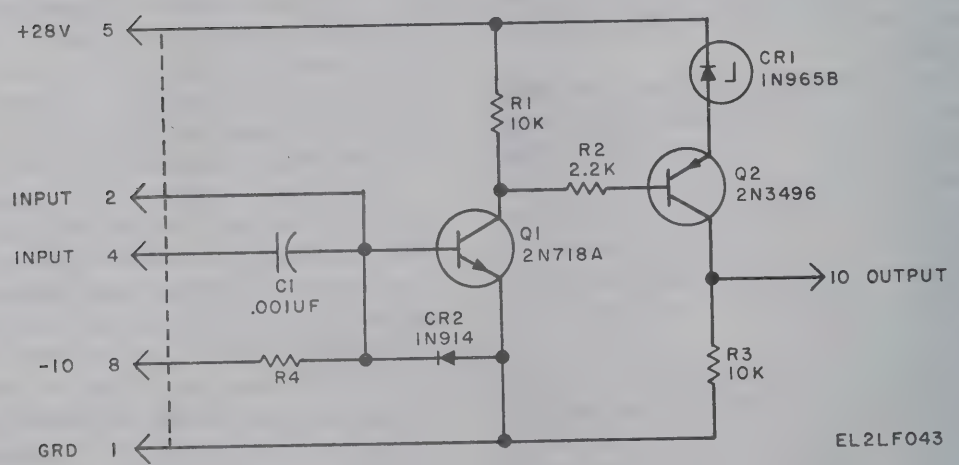


Figure 3-22. Line driver 1A2A5A24A44, schematic diagram.

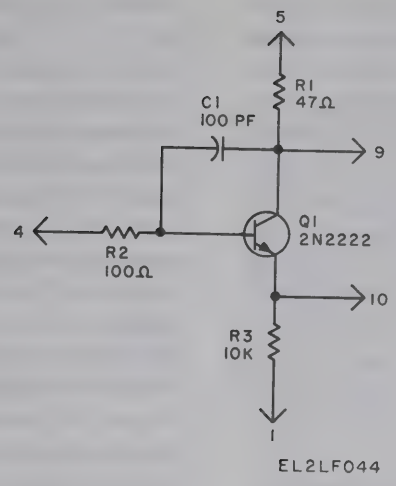


Figure 3-23. Impedance amplifier 1A2A5A24A45, schematic diagram.

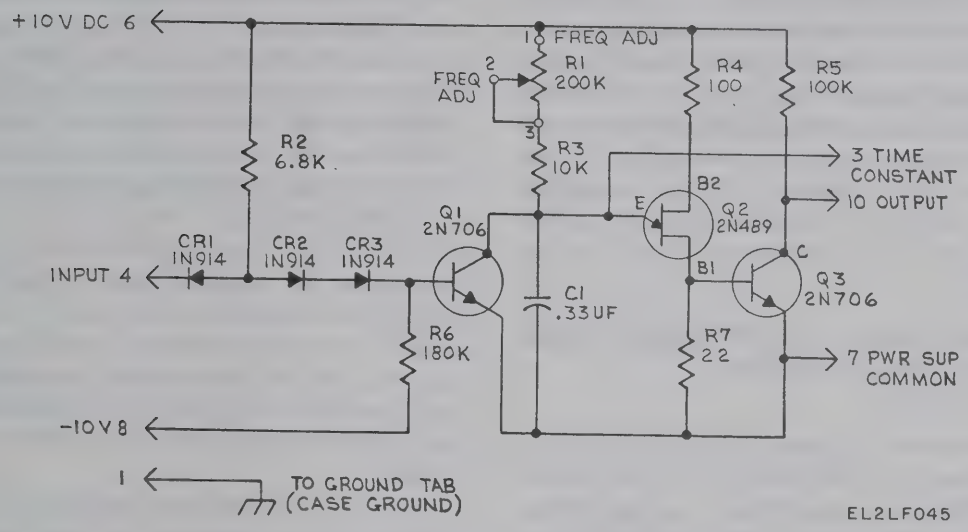


Figure 3-24. Variable time delay 1A2A5A24A47, schematic diagram.

3-13. Rf Power Monitor and Control 1A2A27 Circuit Analysis

(fig. FO 3-10 and FO 3-11)

a. With the exception of power meter A4, the rf power monitor and control (fig. FO 3-10) contains basic circuitry and requires no detailed circuit analysis. Refer to the functional analysis and controls and indicators for the basic operation of the panel.

b. Rf power meter A4 (fig. FO 3-11) provides a means of continously monitoring transmitter forward power output from 10 watts to 10 kw. The panel also provides an automatic high and low power audible alarm. The rf power meter on this panel allows the operator to set the transmitter power, at a given frequency, to within 0.2 db over the power range of 10 watts to 10 kw. Controls on this panel allow the operator to set the high and low power automatic alarm points to within 0.5 db of the power meter reading.

(1) The output from rf power head 2A3A10A22 is applied through coaxial switch 2A3A10S5 to J2 on rf power meter 1A2A27A4. The dc input signal from the power head is applied to modulator G1-A. The square-wave output signal of the modulator is stepped-up by input transformer T1 and applied to low-noise preamplifier Q1-AR2. The square-wave signal is amplified in this circuit and coupled to filter amplifier AR3, where much of the noise and other spurious signals are filtered out. The resulting sine-wave signal is then amplified and coupled to phase splitter Q2, Q3. This circuit provides the phase splitting action required to provide the demodulator input. The full-wave demodulator (G1-B), which is synchronously driven with the modulator, recovers the input dc signal at a greatly amplified level.

(2) The output of the demodulator is applied to integrating amplifier AR4, Q4. This circuit provides additional signal gain, and also reduces the

amplifier bandwidth to the degree required consistent with the selected resonse time (and noise level). The amplifier stage feedback capacitor determines the bandwidth of the dc amplifier and is controlled by the setting of the RESPONSE switch S2. When in the NORM position the response time of the power meter is less than 1 second and the noise is less than ±1 percent p-p of full scale on the most sensitive range. When in the FAST position the response time decreases to approximately 100 milliseconds, but the noise increasing particularly on the low ranges. The output of the integrating amplifier is coupled back to the modulator and input transformer circuit through the switch network. This feedback path provides a high degree of degeneration and, thus, gain stability, and at the same time provides a means of accurate control of the overall amplifier gain.

(3) The output of the integrating amplifier is also applied to the compensation network in the power head, where compensation is made for the sensitivity of the power head, and for its inefficiency at the frequency of the signal under measurement. The return from the power head compensation network is applied to inverting amplifier AR1, and the output of this circuit drives the front-panel meter M1 through a second range switch network.

3-14. Communications (IF) Patching Panel 1A3A22, Circuit Analysis.

(fig. FO 3-12)

The communications (if.) patching panel functions as an interconnection point for all signals to and from the AN/TSC-54 transmitting and receiving equipment. Figure FO 3-12 is a schematic diagram of the panel. Refer to the functional analysis for the basic operation of the panel.

3-15. Comm Demod 1A3A3 Circuit Analysis.

(fig. 3-25 through 3-45 and FO 3-13 through FO 3-21)

The comm demod of the AN/TSC-54 processes and detects the 70 MHz receive signal from the receiving circuits. It provides an audio output and antenna control signal. The detailed circuit analysis for the comm demod is given in *a* through *x* below.

a. The 70 MHz bandpass filter A1 (fig. 3-25) provides a 4-megahertz bandpass at 70 MHz. It is a 3-pole Butterworth configuration and has a vswr of less than 1.2 to 1 across the frequency band. Tuning is provided by variable capacitors C3, C6 and C8. Capacitors C1 and C10 are the variable elements of the impedance matching network used at the output and the input.

b. The 70 MHz to 21.4 MHz balanced mixer A2 as illustrated in figure 3-26, consists of two amplifier transmitters, Q1 and Q2, and a balanced mixer consisting of diodes CR1A and CR1B and transformer T1. The 48.6 MHz local oscillator signal is applied across resistor R1, which provides an input impedance match, and is coupled by capacitor C2 to the base of transistor Q1. Bias for transistor Q1 is developed by the voltage divider network composed of resistors R2 and R3 which are connected between -15 vdc and ground. Decoupling for the negative voltage supply is provided by inductors L6 and L7, and capacitors C8, C10, and C12. Capacitor C9 is a bypass for emitter resistor R11. The output from the collector of transistor Q1 is taken from tapped inductor L3 and is applied to the primary of transformer T1. The 70 MHz singal is applied through a resistive T attenuator and a Pi-type impedance matching filter to the center tape of the secondary winding of transformer T1. The two signals are mixed by diode matched pair CR1 and filtered by inductor L4 and capacitors C4 and C5. Resistor R6 provides the proper filter termination impedance. The 21.4 MHz intermediate frequency is coupled by capacitor C6 to the base of transistor Q2. The output signal is taken from the center tap of collector load inductor L5. Resistor R10 provides an output impedance match.

c. Demod 48.6 MHz vco A3 (fig. FO 3-14) consists of an oscillator and amplifiers and is discussed in (1), (2), and (3) below. Control of oscillator Q1 frequency is accomplished by use of varactor diode CR1. The control voltage is applied at pin 6 of jack J2. Any change in the value of varactor bias voltage causes a change in the capacitance of the diode and a corresponding change in the vco output frequency.

(1) The output from oscillator transistor Q1 is taken across resistor R1 and is coupled by capacitor C7 to the base of amplifier transistor Q2. Regenerative feedback is indictively coupled from the collector circuit of transistor Q2 by variable inductor L3 to inductor L2 in the gate circuit of transistor Q1. The output signal from transistor Q2 is applied across a divider network consisting of capacitors C8 through C10. One output from the divider is coupled by diode CR6 through resistor R17 to the inverting input at pin 2 of dc amplifier AR1.

(2) The noninverting input of dc amplifier AR1 is set to -0.8 vdc by the voltage divider consisting of resistors R20 and R21. The output of dc amplifier AR1 controls the gain of transistor Q2 through resistor R4. The combination of dc amplifier AR1, transistor Q2, and diode CR6 form an agc loop to hold the output of diode CR6 constant at -0.8 vdc. In this manner, the power output of the 48.6 MHz vco is held at a constant level over its frequency range. Resistor R18 and capacitor C15 form the feedback network around dc amplifier AR1. The RC network determines the agc time constant. Diode CR5 and

resistor R22 provide forward bias to diode CR6 to overcome any forward voltage drop.

(3) Transistor Q3 provides a constant current bias for output amplifier transistor Q4. The power output is taken from transformer T1 through the 3-way power divider consisting of resistors R12 through R15 at output jacks J3, J4 and J5. Offset bias is supplied to the afc and sweep circuit by Zener diode CR3 through Stabistor diode CR2 and resistor R29. Variations in ambient temperature cause corresponding changes in the voltage drop across stabistor diode CR2. The resulting changes in bias output cause necessary changes in vco voltage, and hence frequency, to cancel the effects of temperature variations on the vco frequency.

d. The 21.4 MHz if. preamplifier A4 is illustrated in figure FO 3-15, consists of five high-gain common-emitter transistor stages. Transformer coupling is used between all stages and at the amplifier output. In each case, the transformer primary inductance forms a part of the tuned collector circuit which is tuned by one of the variable capacitors C6, C10, C16, C24 or C33. The agc input voltage at pin 6 of jack J3 controls the collector current, and hence the gain of transistors Q2, A3 and Q4. Forward agc is used (that is, increasing collector current causes a decrease in gain) to provide a 50 dB range of amplifier gain.

e. The signal bandwidth select switch A5 (fig. 3-27) essentially consists of a matrix of diode switches. Normally, all the diodes are heavily reversed biased by the application of -28 vdc at pin 5 of jack J7. Selection of the 75 kHz bandwidth, for example, requires the application of a positive voltage at pin 4 of jack J7. The positive voltage forward biases diode CR1 into conduction and completes the rf signal path between jacks J1 and J2. Other bandwidths are selected in an identical manner by forward biasing the appropriate diodes.

f. The 75 kHz bandpass filter A6 (fig. 3-28) contains two crystals connected in a half-lattice configuration. The crystal network has a resonant frequency of 21.4 MHz. Bandwidth is controlled by series matching networks which determine the loaded circuit Q factor. Proper insertion loss (10 db) is determined by an internal resistive T attenuator. The 150 kHz bandpass filter operates in an identical manner except for the insertion of a 13 db loss.

NOTES:

1. UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS, ±5% TOLERANCE 1/4 WATT.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUB-ASSEMBLY DESIGNATION (S).

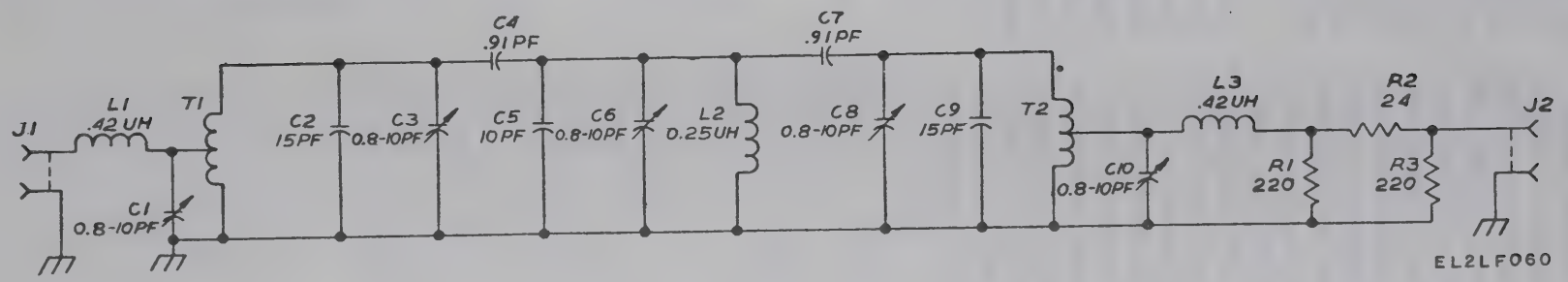


Figure 3-25. 70 MHz bandpass filter 1A3A3A1, schematic diagram.

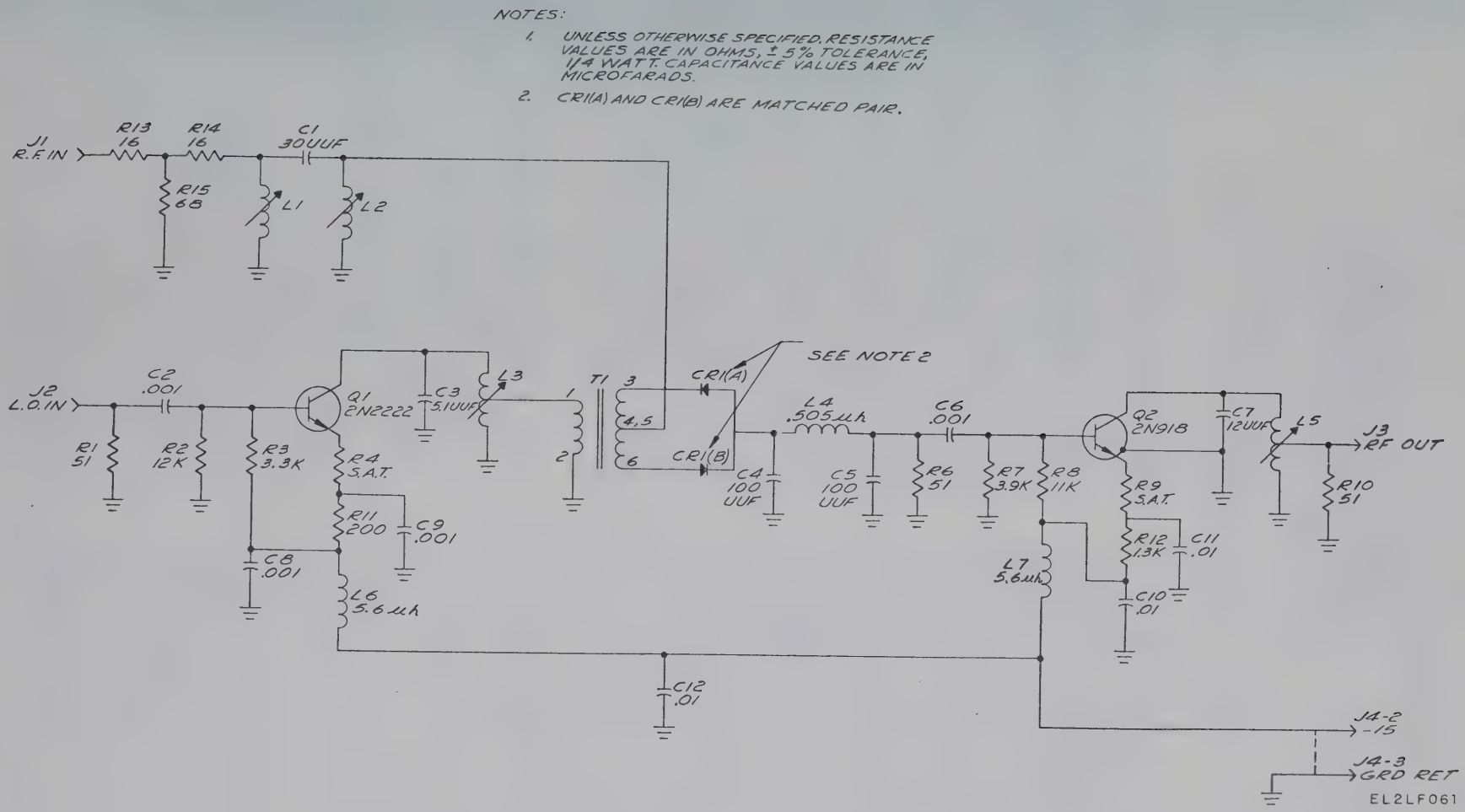


Figure 3-26. 70 MHz to 21.4 MHz balanced mixer 1A3A3A2, schematic diagram.

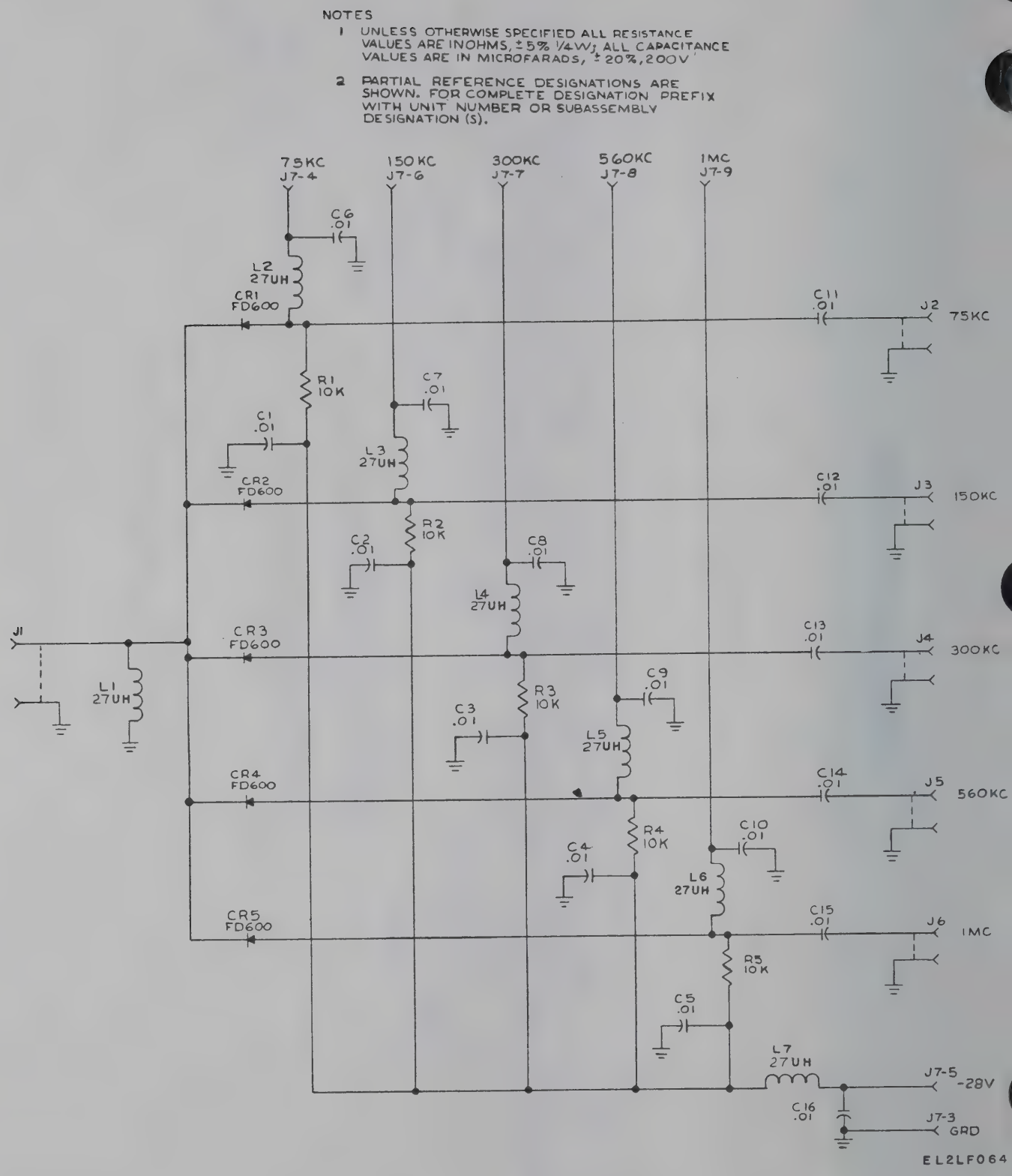


Figure 3-27. Signal bandwidth select switch 1A3A3A5, schematic diagram.

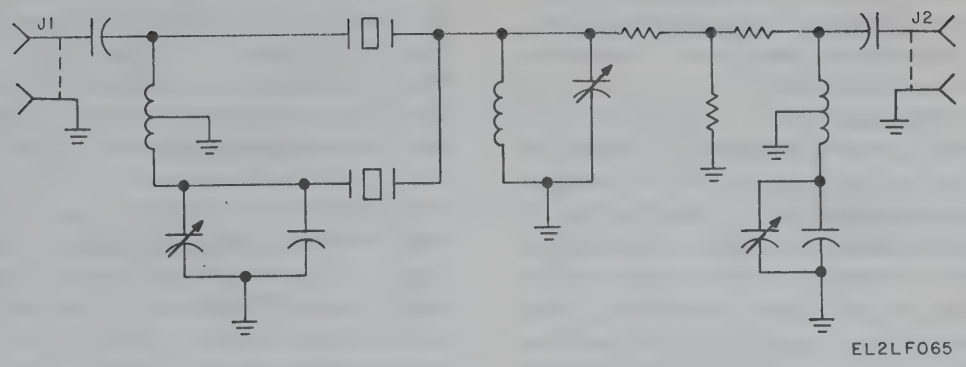


Figure 3-28. 75 kHz bandpass filter 1A3A3A6, schematic diagram.

g. The 300 kHz bandpass filter A8 (fig. 3-29) is a 3-section, linear-phase filter. Variable capacitors C2, C5, and C8 provide tuning. The pi attenuator consisting of resistors R1, R2 and R3 sets the insertion loss at 16 db. The 560 kHz (A9) and 1000 kHz (A10) bandpass filters operate identically except for an insertion loss of 19 dB and 21.5 dB, respectively and are illustrated in figures 3-30 and 3-31.

h. The 21.4 MHz post amplifier A12 illustrated in figure FO 3-16 consists of four identical transformer-coupled tuned stages and an envelope detector. The stages are tuned by variable capacitors C2, C10, C14 and C18. Detection is performed by diode CR1. The output is smoothed by the pi-section low-pass filter consisting of capacitors C24 and C25 and inductor L7 in the collector circuit of amplifier transistor Q5. Multiple outputs are taken from the secondary of transformer T5 through the 6-way power divider composed of resistors R27 through R33. The amplifier has an overall gain of 35 dB and a 1 dB bandwidth of 1.4 MHz.

i. 21.4 MHz am. phase detector A13 (fig. FO 3-17) consists of two buffer amplifiers and a phase/frequency discriminator bridge. The circuit compares the input signal to a reference signal and produces an output voltage which is proportional to the difference in phase between the signals. Since the amplifier stages are identical, only amplifiers Q1 and Q2 are discussed:

(1) A reference signal of 21.4 MHz is applied to connector J2. The reference signal is coupled by capacitor C3 to the base of amplifier transistor Q1. Dc bias is provided by the voltage divider consisting of resistors R9 and R10. The collector current is determined by resistor R11 which is bypassed by capacitor C6. Unbypassed resistor R4 controls the degeneration, and hence the gain of transistor Q1. The collector circuit contains a tuned resonant circuit consisting of inductor L1 and capacitor C1. Resistor R1 loads the tuned circuit and provides a wider bandpass. The operation of amplifier transistor Q2 is similar to that of amplifier transistor Q1. The output from transistor Q2 is coupled by transformer T1 to the input of transformer T2.

(2) The 21.4 MHz input signal at connector J1 is amplified by transistors Q3 and Q4 the same way as the reference signal. The output from transistor Q4 is coupled by transformer T3 to the input of transformer T4. Any difference in phase between the reference signal and the input signal causes an unbalance in the diode bridge and an output is produced at pin 7 of jack J3.

j. The 21.4 MHz vco illustrated in figure FO 3-18 provides an input to the 21.4 MHz am. phase detector (*i* above) and a 90 degree phase shifted reference signal to the 21.4 MHz loop phase detector. The circuit consists of a highly stable voltage-controlled oscillator, buffer stages, and am. agc loop for linear operation. A gain-controlled field effect transistor (FET) Q1, with a Hartley-type tank circuit, is used as the oscillator. The oscillator stage is followed by a common base amplifier Q2 and transistor Q3. The 21.4 MHz output is taken from power amplifier transistor Q5. Transistor Q4 provides a stable bias for amplifier transistor Q5. Operational amplifier AR2 compares the detected output at diode CR1 to a dc reference level established by the voltage divider composed of resistors R25 and R26. The operational amplifier adjusts the gain of transistor Q1 to provide a constant output power.

(1) The signal applied to pin 6 of jack J2 from the 21.4 MHz loop amplifier consists of two terms. A sinewave term which is caused by the carrier modulation, and a dc term which is generated in the vco and fed into the loop amplifier input to be summed with the modulation term. The dc term sets the free-running frequency of the vco to 21.4 MHz. This reference voltage is set by Zener diode CR4. Temperature compensation is provided by stabistor diode CR3 the forward-voltage drop of which changes with temperature. The forward-voltage drop changes in a direction that compensates for the change in resonant frequency of the tank circuit and thus maintains a nearly constant

oscillator frequency. The 21.4 MHz singal applied to the gate input is amplified by transistor Q1 and appears across the emitter-base circuit of common base amplifier transistor Q2.

(2) Bias for transistor Q2 is derived through the voltage divider network comprised of resistors R5, R6 and R7 connected to the positive voltage supply. The amplified signal in the collector circuit of transistor Q2 is developed across the distributed capacity of tuned inductor L2 and capacitor C5 which is resonant at the center frequency. This signal is coupled through capacitor C8 and across resistor R10 to the gage input of FET Q3. Positive potential for the drain of transistor Q3 is through resistors R16 and R11, and inductor L3 from the positive supply voltage. Negative bias for base stabilization of transistor Q4 is derived from the voltage divider consisting of resistors R14 and R13 connected across the positive supply.

(3) The output of the stabilized drain circuit of transistor Q3 is coupled through capacitor C9 to the base of grounded emitter transistor Q5. Bias for the base of transistor Q5 is developed by transistor Q4. The output signal appears across the primary winding of transformer T1 and is applied across the secondary winding to output jack J3.

k. The 21.4 MHz and 1.4 MHz loop amplifiers A21, illustrated in figure 3-32, provide outputs to the 1.4 MHz post amplifier and to the 21.4 MHz and 1.4 MHz voltage controlled oscillators, respectively. The input to the loop amplifiers, from their respective loop phase detectors, is passed through an active rc low-pass filter. Four selectable phase-lock loop bandwidths of 30 kHz, 50 kHz, 300 kHz, and 1500 kHz are available. The selection of the particular bandwidth filter depends upon the mode of operation as determined by matrix board A45 and the mode select switch. The circuit illustrated in figure 3-32 shows the relay switching configuration for selecting the desired loop bandwidth filter. With the relay contacts in the positions shown on the circuit diagram, the input signal applied at pin 6 of jack J1 is interconnected through the series connected relay contacts to pin 25 of jack J4. As shown on the functional diagram (fig. FO 2-2, sheet 9), a 50 kHz bandwidth filter is inserted between pins 7, 14, and 25 of jack J4. The loop filter provides the complex feedback impedance required between jack pins 7 and 14 and the series input resistor required between pin 25 and 7. A control bias from the 21.4 MHz vco is applied through pin 8 of jack J1 (fig. 3-32) and is summed with the input signal from the phase detector at pin 2 of operational amplifier AR1. Input pin 3 of amplifier AR1 is referenced to the signal return. Amplifier AR1 is used as a high gain operational amplifier and provides the vco correction voltage to the 21.4 MHz vco and also to the baseband amplifier. Emitter follower stage Q1 provides a low output impedance through current limiting resistor R4. Resistor R2 is the load resistor for amplifier AR1.

l. The agc amplifier A22 (fig. 3-33) receives the detected envelope signal from the 21.4 MHz post amplifier and provides the agc control reference voltage to the 21.4 MHz if. preamplifier. Outputs are also provided to local and remote signal strength meters. The circuit consists of cascaded operational amplifiers AR1 and AR2. The circuit theory of these two amplifiers is identical; therefore, only the details of feedback arrangements will be discussed here.

NOTE:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
2. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, ±5% TOLERANCE 1/4 WATT. CAPACITANCE VALUES ARE MICROMICRO FARADS.
3. WHEN PIN 9 ON MOTHER BOARD IS CONNECTED TO J2. THE WIRE FROM PIN 9 ON CHIP BOARD SM-D-5711169 TO MOTHER BOARD IS REMOVED.

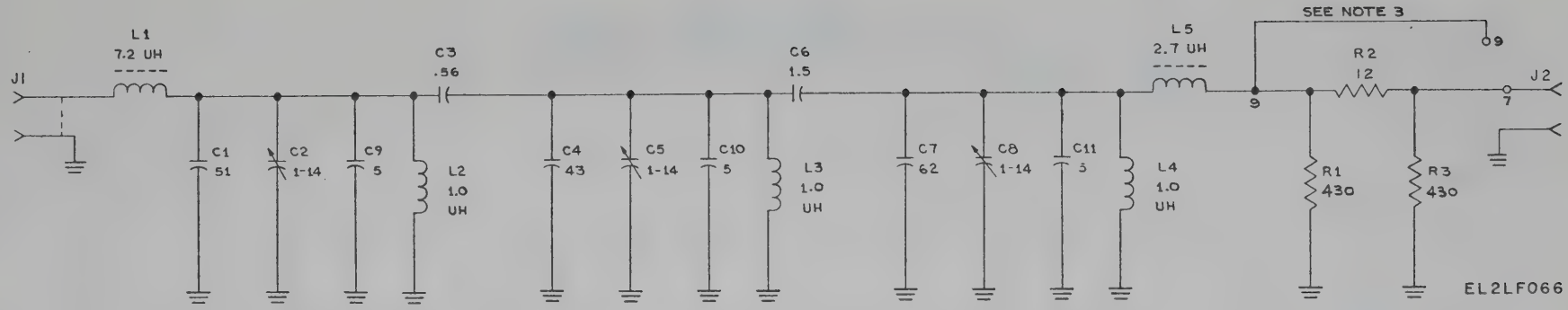


Figure 3-29. 300 kHz bandpass filter 1A3A3A8, schematic diagram.

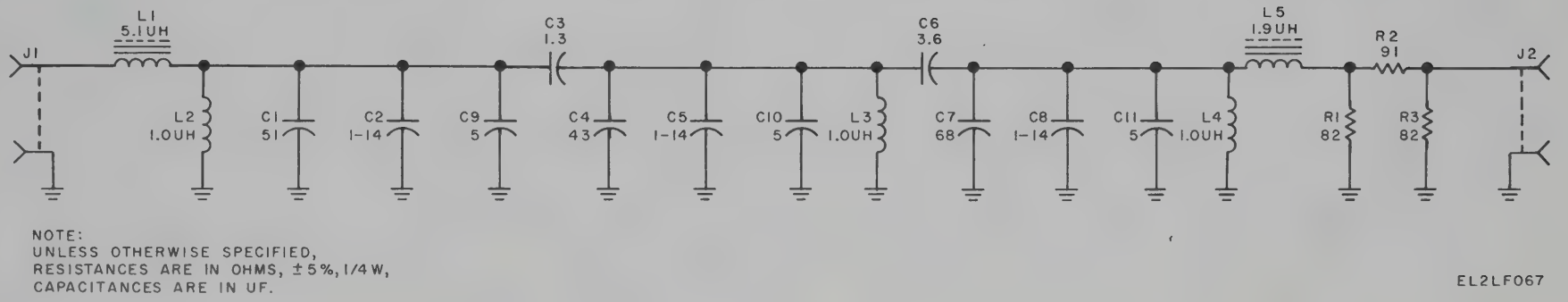


Figure 3-30. 560 kHz bandpass filter 1A3A3A9, schematic diagram.

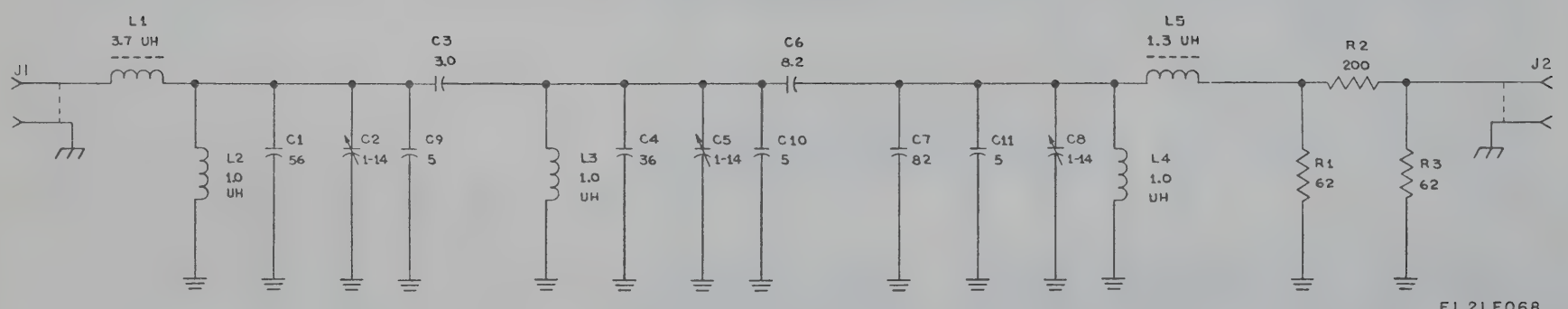


Figure 3-31. 1000 kHz bandpass filter 1A3A3A10, schematic diagram.

NOTES:

1. FOR 21.4 MHz LOOP, J5 IS FOR 300KHz LOOP FILTER, J4 IS FOR 50 KHz BW LOOP FILTER, J6 IS FOR 1500 KHz BW LOOP FILTER, AND J3 IS FOR 30 KHz BW LOOP FILTER.

2. FOR 1.4 MHz LOOP, J5 AND J6 ARE SPARES, J3 IS FOR 275 Hz BW LOOP FILTER, J4 IS FOR 550 Hz BW LOOP FILTER.

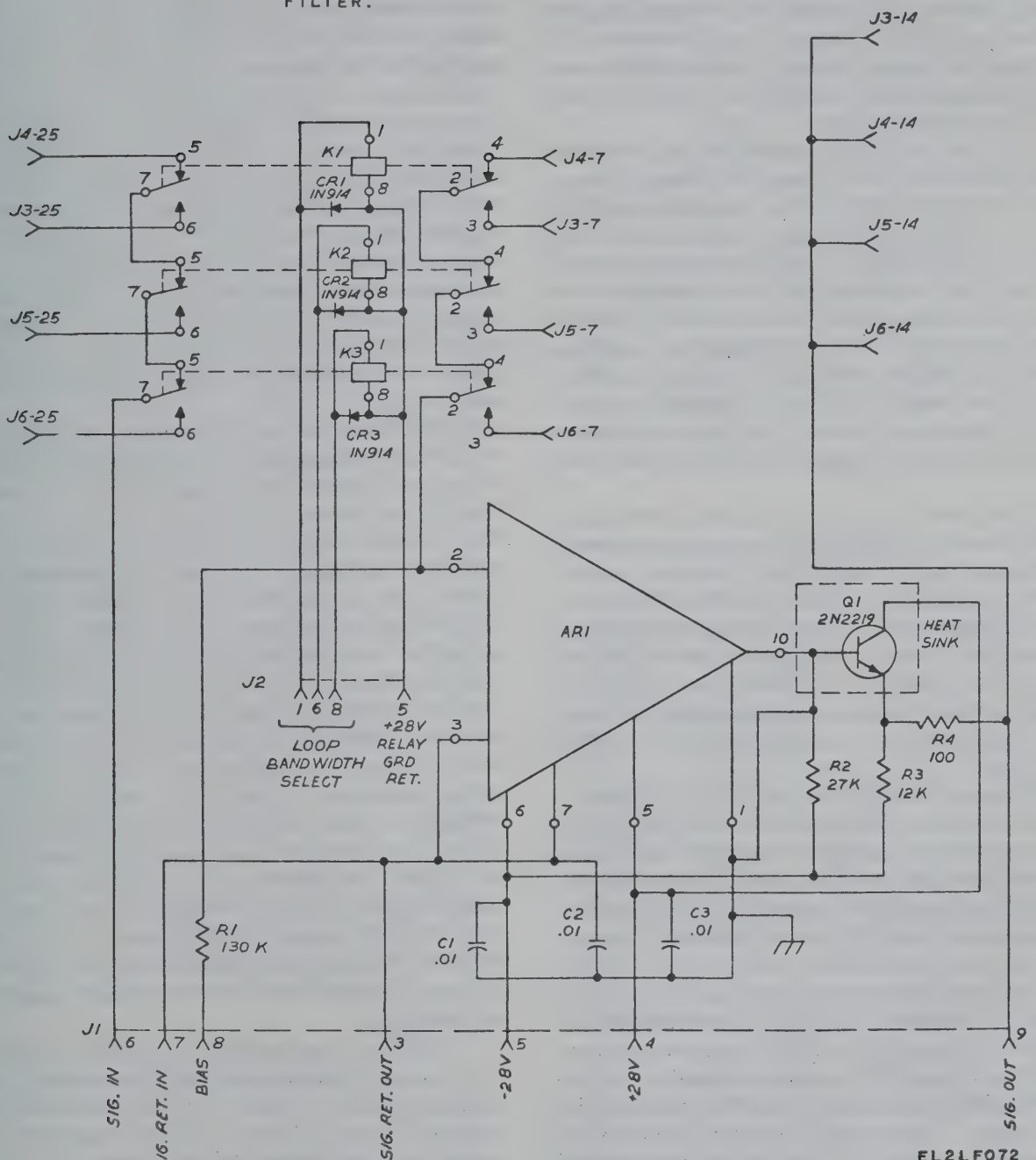


Figure 3-32. 21.4 MHz and 1.4 MHz loop amplifiers 1A3A3A21, schematic diagram.

(1) Amplifier AR1 is used in a high gain integrator configuration with the feedback network consisting of capacitor C1 and resistor R1 providing the required time constant. The agc input (the detected envelope from the 21.4 post amplifier) is applied through pin 6 of jack J1 across the integrating network consisting of resistor R18 and capacitor C13. A fixed reference voltage is applied to pin 3 of amplifier AR1 from the voltage divider network consisting of resistor R4, resistor R3, and potentiometer R5. The setting of potentiometer R5 determines the value of input voltage at which agc is initiated, and thus controls the output power level of if. preamplifier A4.

(2) The output of the amplifier is developed across resistor R27 and is applied through resistors R6, R19, and R20 to the respective signal strength circuits, and through series resistor R8 and potentiometer R9 to input 2 of amplifier AR2. Input pin 3 of this amplifier is connected to the common reference point. Potentiometer R9 and feedback resistor R12 control the gain of amplifier AR2, and potentiometer R10 controls the offset voltage. Thus resistor R10 is the zero adjustment control for the signal strength meters, while resistor B9 provides calibration of the full-scale reading.

(3) The output of the amplifier, developed across resistor R13, is applied through series resistor R17 to the base of transistor Q1 which is used in an emitter follower configuration. Diode CR4 holds the base of transistor Q1 from being driven excessively positive. Zener diode CR3 prevents the output level from going less negative than -9 vdc. As previously noted, the agc output is applied through pin 6 of jack J2 to control the gain of the 21.4 MHz preamplifier.

m. The demod signal detector A23 (fig. 3-34) provides an output to the phase lock and sweep stop circuit when an am. signal of sufficient amplitude is received from the envelope detector circuit of the 21.4 MHz post amplifier. Amplifier AR1, together with resistors R1 and R2 and capacitor C1, form a smoothing filter followed by amplifier AR2 which is used as a level detector. The level detector circuit drives operational amplifier AR3 and transistor Q1 which are arranged in a multivibrator configuration. Relays K1 and K2 are deenergized when the level of the detected signal is insufficient to fire the multivibrator. Under this condition, there is no signal detect indication through the deenergized contacts of relay K3 to the antenna control panel, and the OR output signal is not applied to the phase lock detect and stop sweep circuit. The circuitry and general operation of amplifiers AR1, AR2, and AR3 is identical; therefore only the feedback and time constant circuits involved in their operation as level detectors will be discussed here.

(1) The envelope detector signal is applied through resistor R1 to the input gate (pin 2) of the input FET stage of amplifier AR1. This is the inverting input of the dc amplifier. The noninverting input (pin 3) of the N-channel FET is referenced to ground potential. The feedback network consisting of capacitor C1 and resistor R2 controls the gain of amplifier AR1. The output of amplifier AR1 is applied through an integrator network, consisting of resistor R3 and capacitor C2, to the noninverting input (pin 3) of amplifier AR2. A reference bias is applied to the inverting input (pin 2) of amplifier AR2 from a voltage divider network connected across the positive supply voltage. The divider network consists of resistor R13, potentiometer R14, and resistors R15, R17, R11 and R12. Resistors R11 and R12 are connected in parallel across resistor R13 and a set portion of potentionmeter R14. Potentiometer R14 is set to provide two levels of voltage across resistors R11 and R12. Relay K3, which is controlled by the position of the receive mode select switch, provides for switching from a lower positive level of bias to a higher positive level.

(2) When the narrowband mode is selected, relay K3 is energized and the higher level of positive bias (+3.5 vdc) developed across resistors R11 and R12 is applied to the pin 2 of amplifier AR2. This higher bias level permits the multivibrator circuit to be fixed on a lower level detected signal input. Test point TP1 provides a monitoring point for the bias adjustment. The amplifier signal from amplifier AR2 is applied through resistor R6 to the noninverting input (pin 3) of amplifier AR3 which has its inverting input (pin 2) referenced to the negative potential on capacitor C3. Capacitor C3 charges from the ground potential through the break contacts of relay K1, resistor R7, and through resistor R18 towards the positive supply. When the level of the output voltage of the amplifier is sufficient to overcome the reference bias, applied through resistor R5 and diode CR1, the output of amplifier AR3 rises in a positive direction. The negative bias maintained by the conduction of diode CR2 is overcome and transistor Q1 is turned on.

(3) When transistor Q1 is turned on, the collector current through resistor R18 causes the OR output at pin 7 of jack J1 to go from +28 vdc to ground. Relays K1 and K4 are energized since there is a conducting dc path through transistor Q1. Relay K2 make contacts cause a logic gate to illuminate a signal detect lamp on the antenna control panel. Relay K1 make contacts connect the positive supply to resistor R7 which, with capacitor C3, forms a 4-second time constant. Capacitor C3 discharges through resistors R7 and R18 and, at the end of the time constant period, a positive volt-

age inhibits amplifier AR3 causing its output to go to ground. Transistor Q1 now becomes cut off, relays K1 and K2 return to the released position, and the OR output returns to the positive supply level (+28 vdc). Capacitor C3 starts charging from ground potential through the break contacts of relay K1 and resistor R7, and at the end of the time constant period, the multivibrator fires again. However, by this time the agc network has reduced the output of if. amplifier A12 to its quiescent level, and the signal detect circuit will not trigger again until another sudden rise in signal level is encountered.

n. The 21.4 MHz wideband discriminator A24 (fig. 3-35 and 3-36) receives an if. input from the 21.4 MHz post amplifier and provides a dc output voltage which is proportional to the frequency shift of the input signal frequency with respect to the 21.4 MHz center frequency. The output voltage is applied to the afc and sweep module. The wideband discriminator circuit diagram is shown on figure 3-35 and consists essentially of a transistor amplifier driving a Foster-Seely type discriminator circuit. The input and output signal characteristics of the narrowband discriminator are shown on figure 3-36.

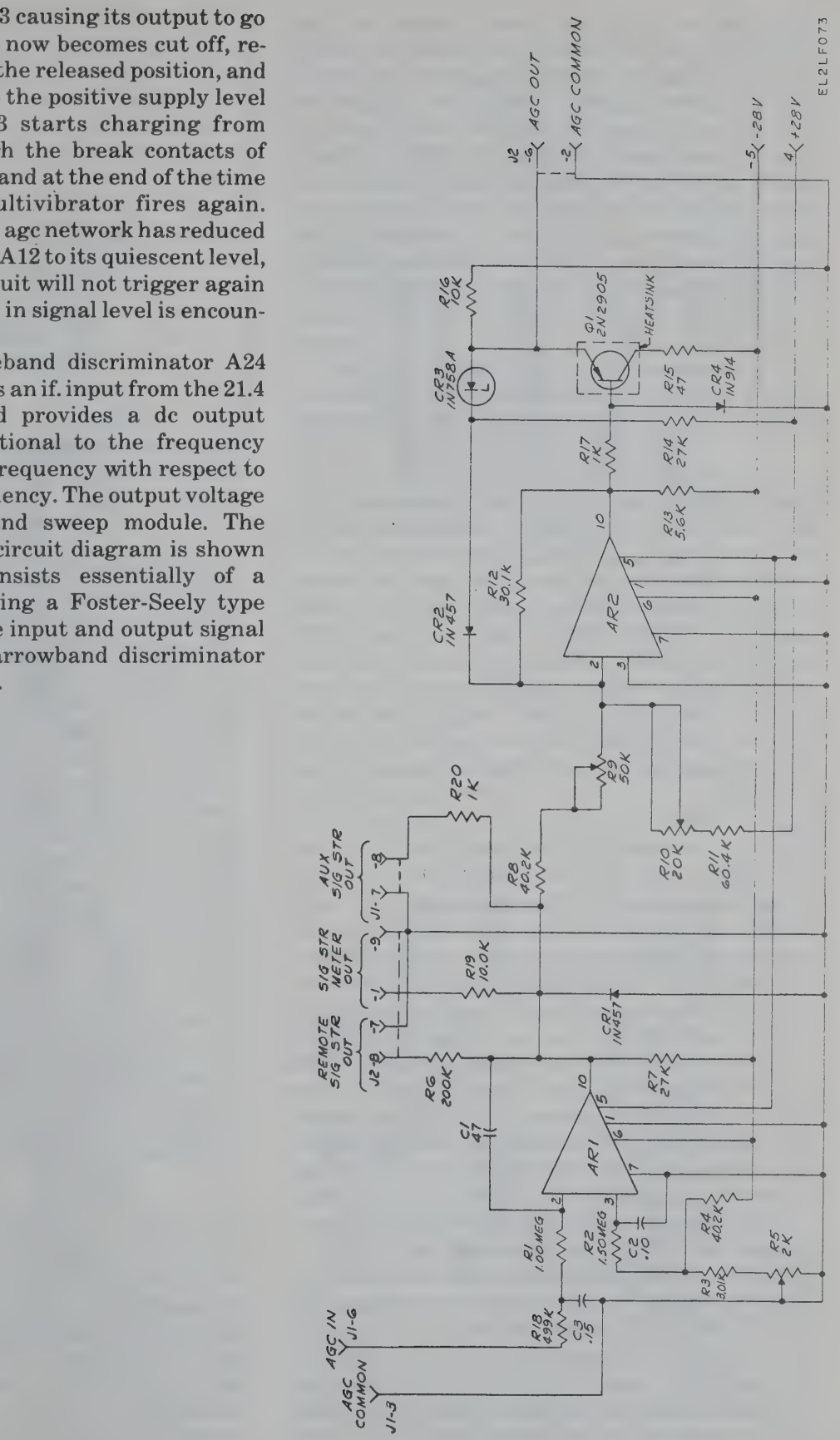


Figure 3-33. Agc amplifier 1A3A3A22, schematic diagram.

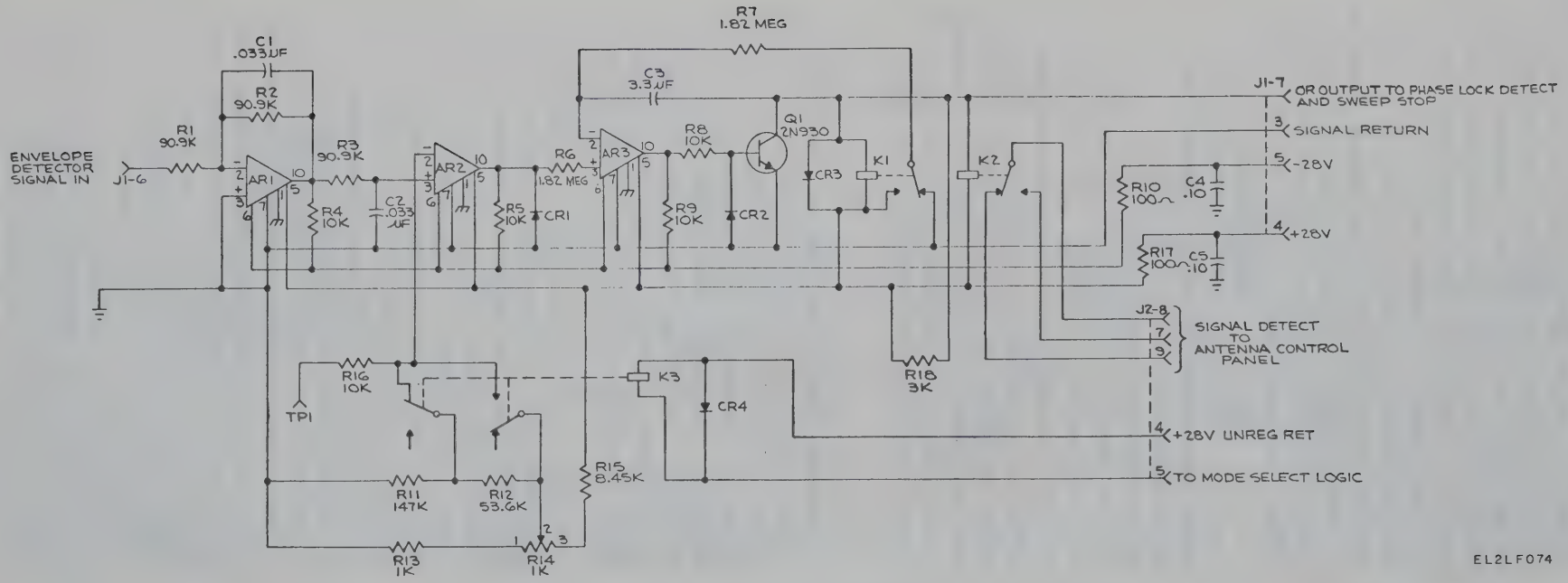


Figure 3-34. Demod signal detector A3A3A23, schematic diagram.

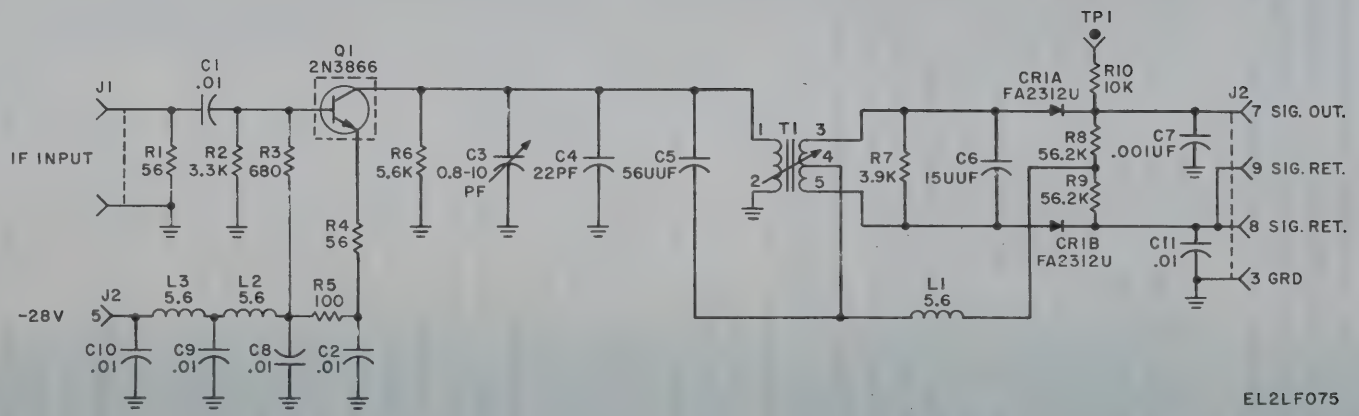


Figure 3-35. 21.4 MHz wideband discriminator 1A3A3A24, schematic diagram.

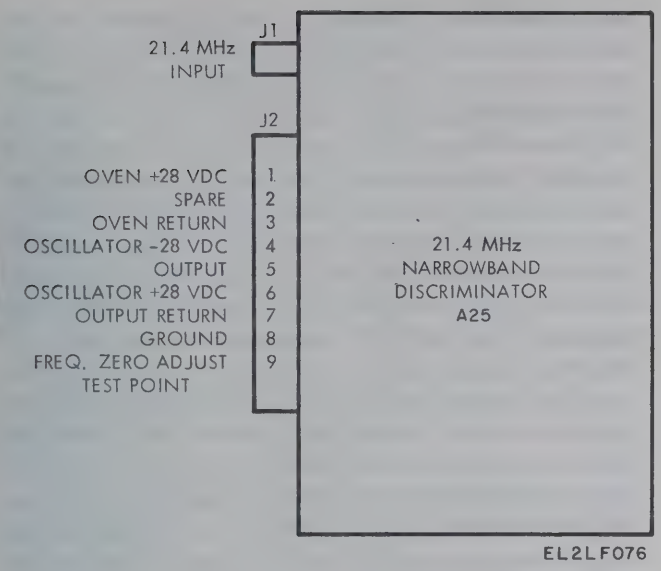


Figure 3-36. 21.4 MHz narrowband discriminator 1A3A3A25, input/output signal characteristics.

(1) The if. input is applied across resistor R1 and coupled by capacitor C1 to the base of transistor Q1. Bias operating potential for the base of transistor Q1 is derived through the voltage divider network, consisting of resistors R3 and R2, which is connected across the negative power supply. Inductors L2 and L3 and capacitors C8, C9, and C10 provide decoupling. Self-bias is developed across emitter resistor R5 which is signal bypassed by capacitor C2. Emitter resistor R4 is unbypassed to provide a slight amount of degenerative feedback. The collector of transistor Q1 is connected through load resistor R6 to the positive (ground) side of the power supply. Tuning capacitor C3 and tuned transformer T1 comprise a resonate circuit at the 21.4 center frequency. Each of the matched diodes (CR1A and CR1B) is connected in series with one half of the secondary winding of double tuned transformer T1 throught its respective load resistor and inductor L1. The primary voltage is developed through capacitor C5 and across inductor L1 between the center tap of the secondary winding and the junctions of load resistors R8 and R9.

(2) The output of diodes CR1A and CR1B are connected in phase opposition. When the input signal is at the center frequency and the phase discriminator is correctly aligned by adjustment of capacitor C3 and tuned transformer T1, the magnitude of the rf voltage applied to diode CR1A is the same as that applied to diode CR1B. This results in equal and opposite polarity voltage across resistors R8 and R9, so that the net voltage across the output is 0 volt. When the input signal frequency deviates above the center frequency, the rf voltage across diode CR1A increases while the rf voltage across diode CR1B decreases. This results in a net positive voltage across the output. Similarly, if the signal frequency deviates below the center frequency, a net negative going voltage appears at the output. The nominal voltage output range is ±4.0 vdc. The discriminator response is in the order of 450 ±200 kHz per volt. To achieve this wideband response and improve the damping of the diodes, resistor R7 is shunted across the secondary winding. A monitor point (TP1) is provided through isolating resistor R10. Capacitors C7 and C11 provide rf return paths to the primary of transformer T1 and isolate the dc output from ground reference.

(3) Operation of the 1.4 narrowband discriminator A26 is essentially identical and its input/output characteristics are shown in figure 3-37.

o. The phase lock detect and sweep stop circuit A27 illustrated in figure 3-38 provides an output of the afc and sweep circuit and controls a visual LOCK indicator on the antenna control panel. The circuit receives one input from the OR output of the demod signal detector and another input from either the 21.4 MHz or the 1.4 MHz am. phase detector (*n* above). The mode of operation (wideband or narrowband) determines which phase detector output signal is applied. The circuit consists of two operational amplifiers, two transistor relay drivers, and associated relays as outlined in (1), (2), and (3) below:

(1) The detector signal input is applied through pin 8 of jack J1 and resistor R2 to the inverted input (pin 2) of amplifier AR1. The noninverted input (pin 3) is referenced to ground potential. Resistor R1 and capacitor C1 form a low-pass smoothing filter. The output is developed across load resistor R4 and is applied to the noninverted input (pin 3) of amplifier AR2 through the low-pass filter consisting of resistor R3 and capacitor C2. The inverted input (pin 2) is maintained at a positive potential by a voltage divider connected across the negative power supply. The voltage divider consists of resistor R6, potentiometer R7, and resistor R8. Potentiometer R7 is adjusted for a correct level reference which can be monitored at test point TP1 through isolation resistor R11.

(2) When the signal level output of amplifier AR1 is sufficiently higher than the bias potential on capacitor C2, the output of amplifier AR2 is clamped at the -28 vdc level through resistor R5. Transistor Q1 is forward biased and conducts causing a number of actions to occur simultaneously. Relays K1 and K2, which are parallel-connected in series with Zener diode CR6 and the positive supply, are energized through conducting transistor Q1 which connects the relays to the negative (ground return) side of the +28 vdc supply. This action places +28 vdc through the make contacts of

relay K1 and pin 2 of jack J2 to illuminate a local LOCK indicator.

(3) At the same time, the make contacts of relay K2 close a LOCK indicator circuit to the antenna control panel through pins 1 and 3 of jack J3. Conduction of transistor Q1 places the cathode of diode CR4 at ground potential which turns on transistor Q2. A ground closure at diode CR3, from the signal detect module, will also turn on transistor Q2. Thus, diodes CR3 and CR4 and transistor Q2 form an OR gate which is enabled by a ground potential. This input is received either from the transistor Q1 circuit or from the demod signal detector control relay K3. When relay K3 is energized, one pair of make contacts grounds the input to the sweep amplifier in the afc and sweep circuit to stop the sweep search. Another pair of make contacts (connected to pins 4 and 5 of jack J3) completes a circuit in the afc and sweep module. The contact closure thus applies the correction voltage from the discriminator to close the afc loop. With the search sweep inhibited, the 48.6 MHz vco is controlled by the afc circuit of the afc and sweep module.

p. The X4 frequency multiplier furnishes two separate 20 MHz outputs, one to the 1.4 MHz narrowband discriminator and one to the 21.4 MHz to 1.4 MHz-balanced mixer. The input signal to the multiplier is a 5 MHz reference signal output of the 5 MHz distribution amplifier. The circuit (fig. FO 3-19) consists of two frequency doubler stages followed by a buffer amplifier output stage as outlined in (1) and (2) below:

(1) The 5 MHz input from the distribution amplifier is applied through jack J1 across input resistor R1. The signal voltage is coupled through capacitor C1 and across resistor R1 to the base of transistor Q1. Bias for amplifier transistor Q1 is determined by the voltage divider composed of resistors R2 and R3 connected between -15 vdc and ground. Resistor R5 controls the collector current and resistor R4 sets the gain of the stage. The collector circuit of transistor Q1 is tuned to resonate at 5 MHz by capacitors C4 and C5 and transformer T1. Resistor R6 is the collector load for transistor Q1. Diodes CR1 and CR2 conduct on alternate half cycles, and thus produce a waveform at the base of transistor Q2. The waveform is composed mainly of second harmonic energy since the diodes are matched.

(2) Transistor Q2 operates the same as transistor Q1 except that the collector circuit is turned to 10 MHz. Matched diode pair CR3 and CR4 produces a 20 MHz signal at the base of buffer amplifier transistor Q3. The transistor Q3 stage is a narrowband amplifier that is turned to 20 MHz by capacitors C12 and C13 and variable inductor L3. Capacitors C12 and C13 form an impedance matching network that reflects the output power divider circuit to the collector of transistor Q3 at the proper impedance level. The -15 vdc power supply is applied through the make contacts of relay K1 which is energized when narrowband operation is selected. The -15 vdc is supplied directly to pin 2 of jack J5 in the beacon demod where the multiplier is required continuously. The -15 vdc supply is filtered by the 4-section LC filter consisting of inductances L1 through L5 and capacitors C3, C8, C15, C16, and C17. The filtering prevents rf leakage into the power supply.

q. The afc and sweep circuit (fig. FO 3-20) functions as an afc circuit during phase lock condition and as a sweep generator during search condition. The circuit consists of four dc amplifiers and associated feedback gain control and stabilization circuits. Amplifier AR1 is used to amplify the error voltage input from the selected discriminator. Relays K1 and K2, controlled by the receive mode selector switch, select the particular discriminator output which is to be applied to the error amplifier. When energized, relay K1 connects the output of the 21.4 MHz wideband discriminator to the input of the error amplifier. Relay K2 similarly connects the output of the 1.4 MHz narrowband discriminator to the input of the error amplifier. As shown on figure FO 3-20 relays K1 and K2 are deenergized and the output of the 21.4 MHz narrowband (200 kHz) discriminator is applied as the input to the error amplifier through relay break contacts K1-2 and K2-2 and input resistor R2. This input is applied to the inverting input (pin 2) of the amplifier AR1. The amplifier's noninverting input (pin 3) is connected through resistor R4 to a ground potential reference. The circuit configuration and general operation of amplifiers AR1 through AR4 are identical; therefore, only the differences applicable to the afc and sweep are discussed.

(1) Resistors R1, R6, and R7 and the integrating network consisting of resistor R3 and capacitor C1 form part of the feedback loop. Relay break contacts K1-5 and K2-5 connect the junction point of resistors R6 and R7 to the inverting input pin of amplifier AR1 to provide the required gain. When relay K1 is energized, the point between resistors R7 and R8 is connected to the input of amplifier AR1, thus increasing the dc gain of the input network. When relay K2 is energized, resistor R1 is shorted out of the feedback loop. The gain of amplifier AR1 is adjusted, in each case, to compensate for the different kHz-per-volt sensitivities of the different discriminators, thus keeping the afc loop response correct for all discriminators. The output of error amplifier AR1 is applied through jack pin J1-7, the made contact of the sweep stop relay and jack pin J1-5 to the inverting input (pin 2) of amplifier AR2. The output of amplifier AR1 is

applied to the input of amplifier AR2 when the sweep stop relay is energized. In this mode, the network acts as an afc amplifier.

(2) Amplifier AR2, in conjunction with capacitors C2 and C3 and resistors R9 and R10, forms an integrating amplifier stage. The output of amplifier AR2 is applied through resistors R15 and R18 to amplifier AR3 which, together with resistors R17 and R23 and capacitor C4, forms the output filter/amplifier that drives the 48.6 MHz vco. The output of amplifier AR2 also is applied through resistor R22 to drive the tuning meter with a voltage that is proportional to the difference between the input frequency and the discriminator center frequency, thus providing a visual indication of the incoming signal frequency. An offset voltage is applied to the input of amplifier AR3 through resistor R21, which has the effect of setting the output voltage of amplifier AR3 to approximately −9 vdc. This level is the desired bias point for the varactor diodes in the 48.6 MHz vco. Also, the bias voltage changes with temperature due to the drop across Stabistor diode CR2 in the 48.6 MHz vco and this action tends to offset the effects of temperature on the vco center frequency. Resistor R18 forms one leg of a voltage divider; the other leg is resistor R26 in the 48.6 MHz vco.

(3) Due to variations in kHz-per-volt sensitivity of the 48.6 MHz vco, each of the modules contains a resistor that controls the gain of the afc and sweep amplifier. Thus, the afc loop response and sweep width is held within tight tolerances over a wide variation of kHz-per-volt slopes of the vco. During manual tuning control of the 48.6 MHz vco, a dc voltage is applied through resistor R20 to provide offset of the output voltage of amplifier AR3, and hence vary the 48.6 MHz vco frequency. The voltage on the manual tuning potentiometer is derived from the divider network consisting of resistors R25 through R28. When no signal is present, the sweep stop relay in the phase lock detect and sweep stop module is opened, and the output of amplifier AR1 is disconnected from the input of amplifier AR2. During search operation, amplifier AR2 is driven by the output of amplifier AR4 to produce a 50 kHz-per-volt sweep output to the 48.6 MHz vco. Under this operating condition, the output across potentiometer R13 and resistor R14 is applied through the integrating network consisting of resistors R36 and capacitor C8 across the clipper circuit of diodes CR7 and CR8.

(4) The rectangular waveform derived by the clipper action ((3) above) is applied to the noninverting input (pin 3) of amplifier AR4. The inverting input (pin 2) is held at a ground potential reference through resistor R37. Amplifier AR4 is alternately turned on and off by the input waveform voltage, and the resulting output at pin 10 is applied across bridge rectifier CR5 which consists of four matched diodes. Zener diode CR9 maintains a constant reference potential across the bridge rectifier. During positive excursions of the amplifier AR4 output, conduction through one side of the bridge sets the positive level of the driveinput to sweep generator AR2 through pin 1 of jack J3, the break contacts of the sweep stop relay, and pin 9 of jack J3. During negative excursions of amplifier AR4 output, conduction through the other side of the bridge sets the negative level of the drive input to the sweep generator. The adjustment of sweep width potentiometer R13 varies the amplitude of the voltage into amplifier AR4, thereby controlling the width of search sweep of the 48.6 MHz vco.

r. The balanced mixer is used to provide the 1.4 MHz if. in the demod and beacon demod. The input from the 21.4 MHz post amplifier and the 20 MHz signal from the X4 frequency multiplier are heterodyned in the mixer to produce the intermediate frequency. The circuit illustrated in figure 3-39 consists of a buffer amplifier stage, a balanced diode modulator, and a tuned output amplifier stage. This circuit functions in a manner similar to the 70 MHz to 21.4 MHz balanced mixer. The only differences in the circuits are the value of the components and the frequencies of the signals. The 1.4 MHz output of 21.4 MHz to 1.4 MHz balanced mixer 1A3A3A30 is applied to the 1.4 MHz if. bandwidth select circuit (*s* below).

s. The 1.4 MHz if. bandwidth select circuit A46 (fig. 3-40) applies the 1.4 MHz intermediate frequency from the balanced mixer to either the 10 kHz or the 4 kHz bandpass filter. The circuit consists of a resistive Pi attenuator network and a relay. The 1.4 MHz if. signal is applied through the attenuator network to the contacts of relay K1. When the relay is deenergized, the if. signal is applied to the 10 kHz bandpass filter. When the relay is energized by a 28 vdc signal from the matrix board at jack J3, the if. signal is routed to the 4 kHz bandpass filter. A 28 vdc return is applied to the relay coil at jack J5.

t. The 1.4 MHz post amplifier A34 provides multiple if. outputs to the 1.4 MHz discriminator and 1.4 MHz phase detectors and a detected output to the agc and am. amplifiers. The circuit (fig. 3-41) consists of three cascaded common emitter stages; transistors Q1, Q2 and Q3 that provide 30 db of gain.

(1) The −15 vdc power supply voltage is applied through individual decoupling networks consisting of inductors L5 through L8 and capacitors C13 through C17. Collector current for the three transistor stages is set by bypassed resistors R19, R20, and R21 in the emitter circuits. Emitter resistors R16, R17, and R18 provide degenerative feedback

to their respective stages and control the stage gain. The 1.4 MHz input signal from the if. bandwidth select circuit is applied through input jack J1 and across impedance matching resistor R1 through capacitor C6 to the base of transistor Q1. The output at the collector of transistor Q1 is coupled to the base of transistor Q2 through a tuned circuit consisting of variable inductor L2, resistor R4, and capacitors C3 and C7. These two capacitors provide impedance matching of transistor Q2. In the output transistor stage, a portion of the collector output is rectified by diode CR1 and filtered by inductor L1 and capacitor C1.

(2) The detected output across resistor R10 is applied through pin 6 of jack J6 to the inputs of the am. and agc amplifiers for development of tracking error and gain control signals, respectively. Undetected outputs from the collector circuit of transistor Q3 are resistively coupled to jacks J2 through J5. From jack J2, the signal is applied to the 1.4

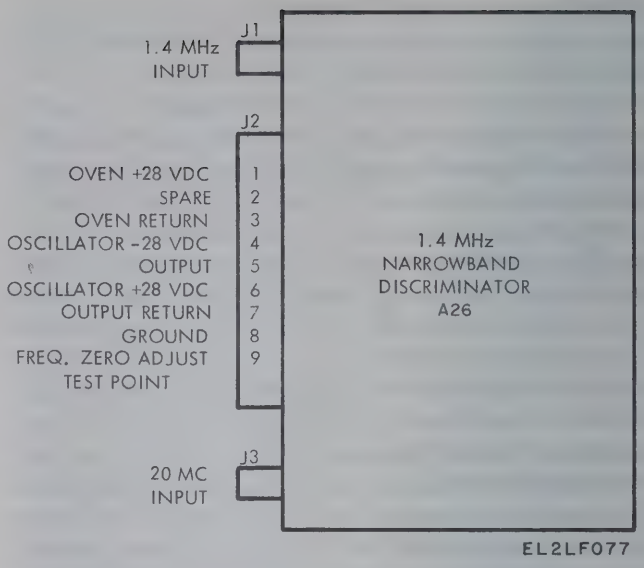


Figure 3-37. 1-4 MHz narrowband discriminator 1A3A3A26, input/output signal characteristics.

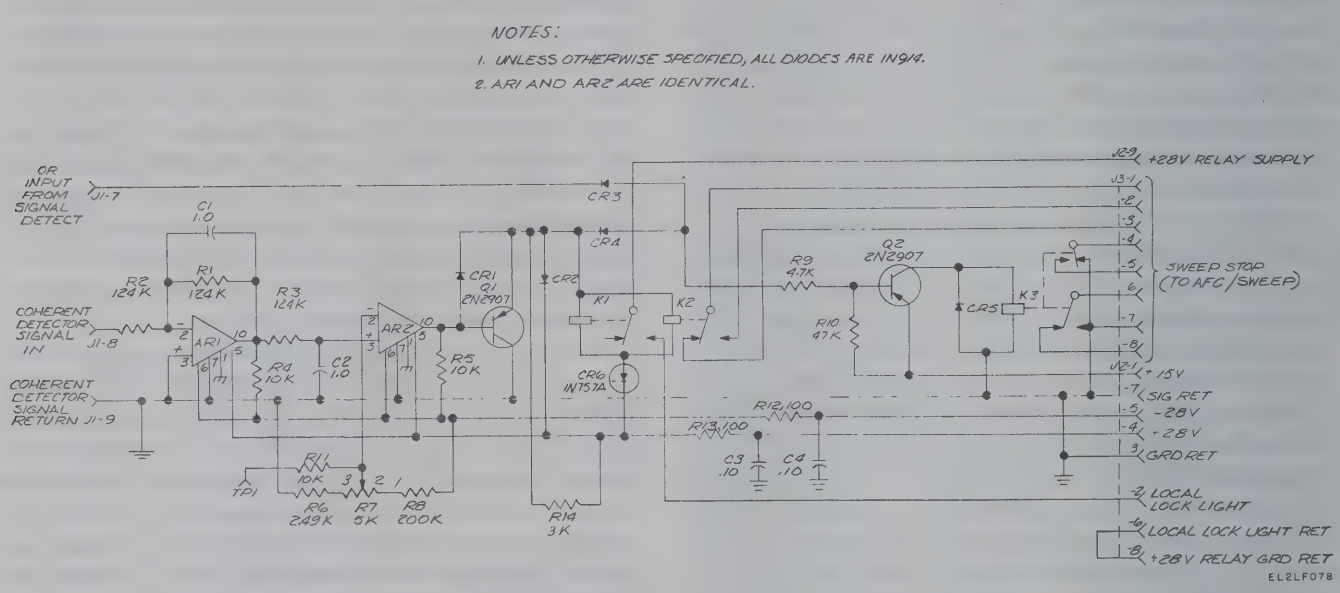


Figure 3-38. Phase lock and sweep stop circuit 1A3A3A27, schematic diagram.

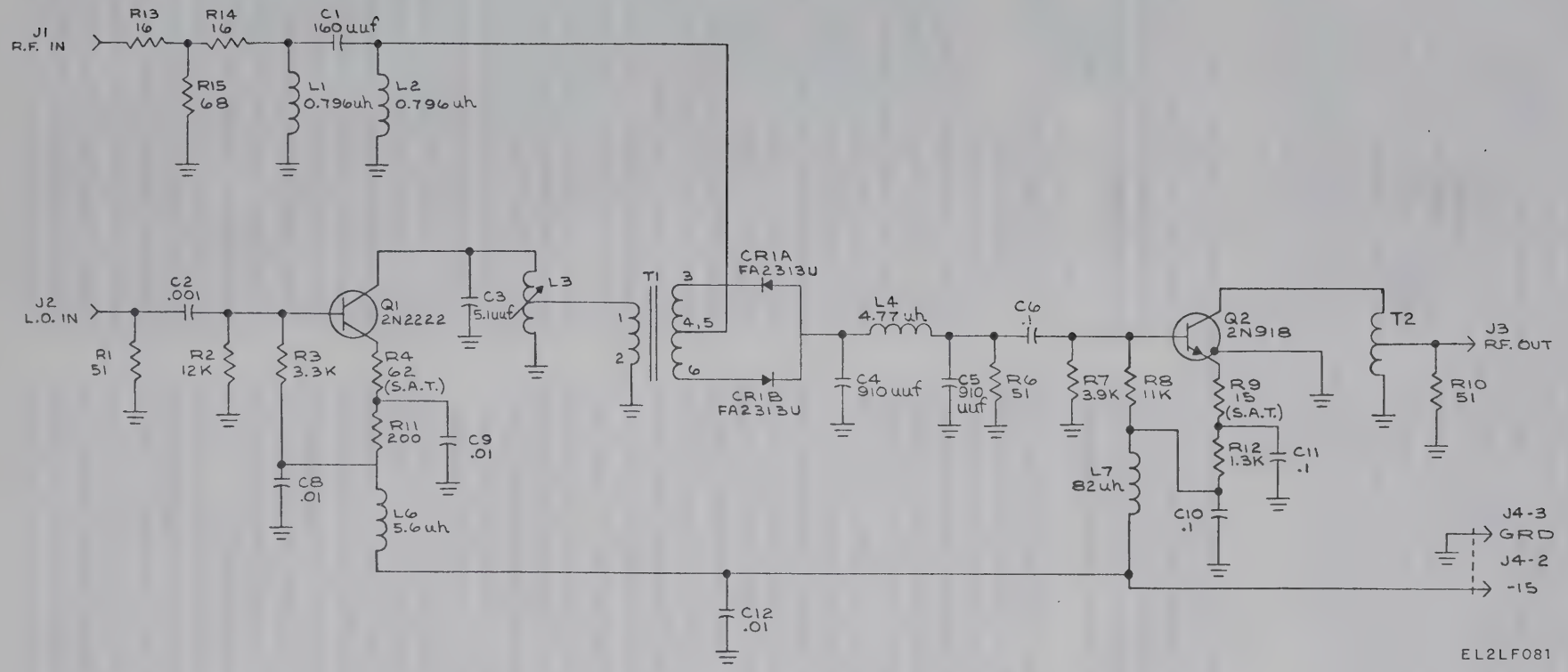


Figure 3-39. 21.4 MHz to 1.4 MHz balanced mixer 1A3A3A30, schematic diagram.

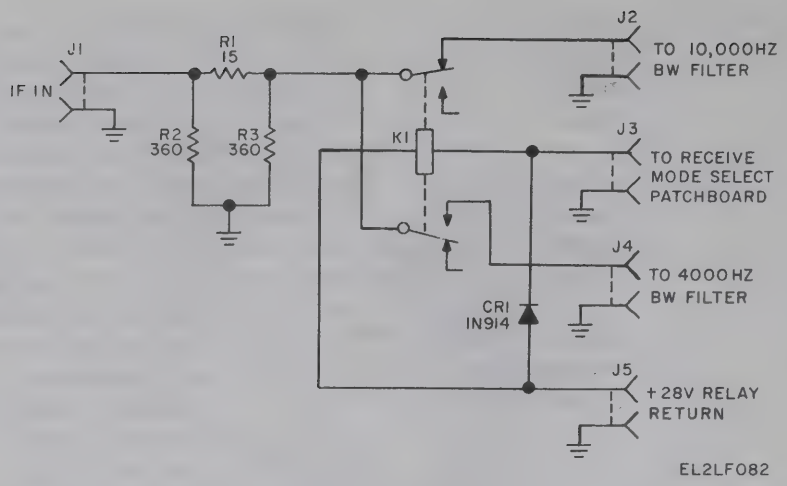


Figure 3-40. 1-4 MHz if. bandwidth select circuit 1A3A3A46, schematic diagram.

MHz narrowband discriminator; from jack J3 it is applied to the 1.4 MHz am. phase detector. Outputs from jacks J4 and J5 are applied to the 1.4 MHz loop phase detector and to the 50 ohm coax termination AT4, respectively.

u. The 1.4 MHz loop phase detector A36 (fig. 3-42) compares the phase of the 1.4 MHz if. signal, from the 1.4 MHz post amplifier, with the reference signal from the 90 degree differential phase shifter. The resultant demodulated audio output is applied to the 1.4 MHz loop amplifier and to the 0-30 db attenuator and baseband amplifier. The loop phase detector consists of two buffer amplifier circuits and a phase detector diode bridge output circuit. The 1.4 MHz reference signal from the phase shifter and the 1.4 MHz if. signal from the post amplifier are amplified in their respective 2-stage transistor circuits. The operation of each of the amplifier circuits is similar, therefore this discussion is limited to the reference amplifier circuit.

(1) The referenceinput is applied through jack J1 across input resistor R1. Capacitor C1 couples the input signal to the base of transistor Q1 which is a common emitter stage and functions as a buffer amplifier. Resistor R4 in the emitter circuit of transistor Q1 is unbypassed to provide degeneration and gain control Collector current is developed across bypassed emitter resistor R5. Inductors L2 and L3 and capacitors C6 and C7 form a negative supply decoupling network. The output from the tuned collector circuit is coupled through capacitor C3 to the base of emitter follower transistor Q2. The output of this stage is capacitance coupled to the primary winding of transformer T1.

(2) The if. input from the post amplifier is similarily amplified and applied to the primary winding of transformer T2. When a difference in either phase or frequency of the post amplifier signal with respect to the reference signal occurs, the difference in currents flowing through the differential rectifier bridge circuit appears as an audio output at pin 8 of jack J3. This output is proportional to the phase or frequency difference of the post amplifier with respect to the reference signal.

NOTE

The input and output signal characteristics of the 1.4 MHz VCXO A38 are shown in figure 3-43.

v. The 0-30 db attenuator and audio amplifier (fig FO 3-21) amplifies the demodulated if. signal (21.4 or 1.4 MHz) from the phase lock loop and supplies an output to the baseband subsystem at a selected level. The demodulated audio (21.4 or 1.4 MHz) signal from relay A48 is applied through pin 6 of jack J1 across input resistor R1. The circuit analysis of relay A48 is covered in chapter 2 and is illustrated in figure 3-46. The signal is applied to FET Q1 which stabilizes the current source circuit that drives emitter follower transistor Q2. The output of the emitter follower is applied to the variable attenuator circuit. The four BASEBAND ATTENUATION switches are shown in the down position on figure FO 3-21. In this condition, minimum attenuation is provided and the overall gain of the circuit is 32 ±2 db. The incoming signal can be attenuated up to 30 db (in 2-db increments) by setting different combinations of switches S1 (2-db) through S4 (16-db) to up position. The output of the attenuator circuit is applied to dc amplifier AR1 which functions as a dc amplifier. The output of amplifier AR1 is further amplified by common emitter transistor Q3 operating class A. The gain of amplifier Q3 (approximately 18 db) is determined by feedback resistor R25 and input resistor R20. The output of transistor Q3 drives transistors Q4 and Q5 that operate in a class B complementary emitter follower configuration. The output of the transistor Q4 and Q5 stage is taken across emitter resistors R26 and R28 through capacitor C8. This output drives transformer T1 through the 562-ohm impedance-matching resistor R27 to provide a balanced 600-ohm output to the baseband subsystem.

The output also drives the BASEBAND LEVEL meter on the front panel of the comm demod through calibrating resistors R30 and R31. Resistors R23 and R28 determine the dc bias points of transistors Q3 and Q4.

w. The am. amplifier contains two independent am. amplifier circuits A44 (fig. 3-44) that operate as conventional, low-frequency, low-gain operational amplifiers. The circuits receive the pseudo-monopulse am. tracking error signals through relay A48 from the envelope detectors and synchronous detectors, and supply these signals to the antenna control subsystem. A 1.4 MHz or 21.4 MHz demodulated envelope signal is applied to jack pin J1-6. The signal is coupled by capacitor C1 and resistor R1 to the input of dc amplifier AR1. The amplified output of amplifier AR1 is applied to the base of emitter follower transistor Q1. Feedback is applied through capacitor C3 and resistor R3 to establish the gain and frequency response of the stage. The output of the emitter follower is the synchronous detector signal, which is applied through pin 7 of jack J2 to the antenna control subsystem where it is used as a tracking error signal. The second amplifier circuit, containing amplifier AR2 and transistor Q2, functions in a similar manner and supplies the envelope detect tracking error signal to the antenna control subsystem.

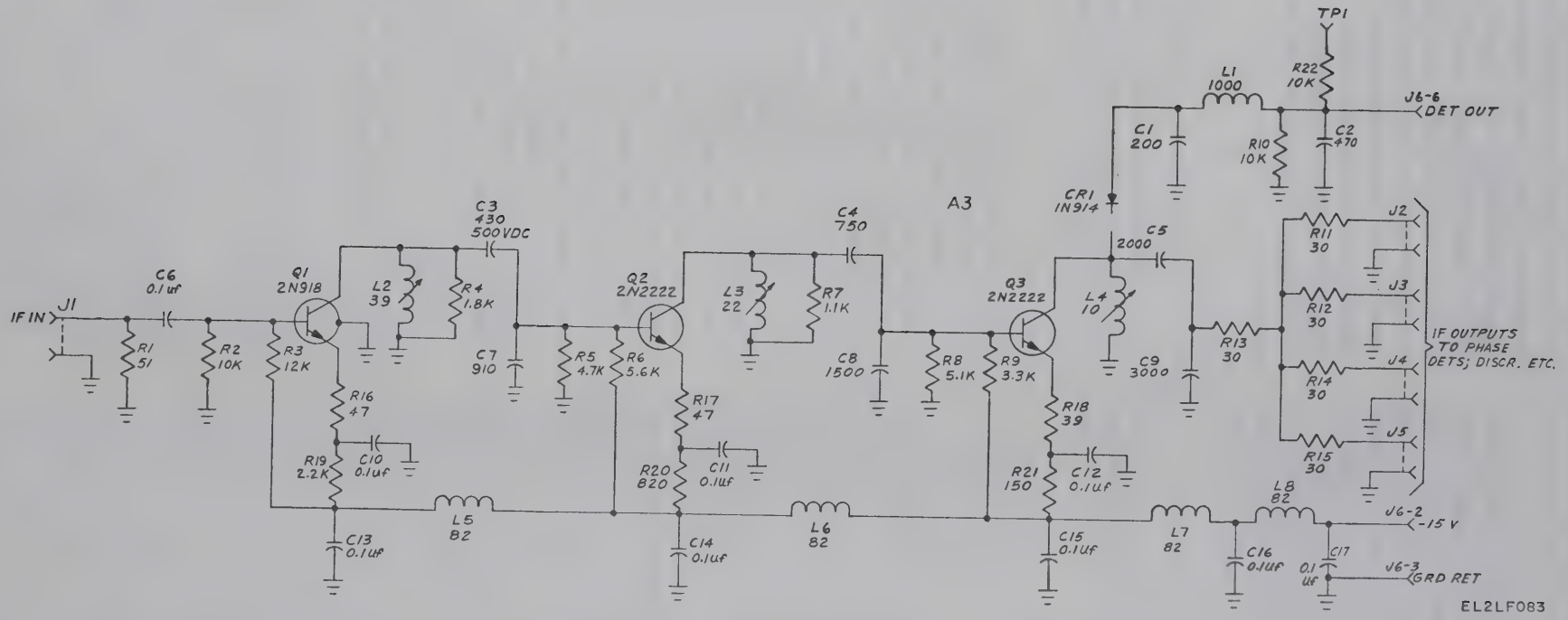


Figure 3-41. 1.4 MHz post amplifier 1A3A3A34 schematic diagram.

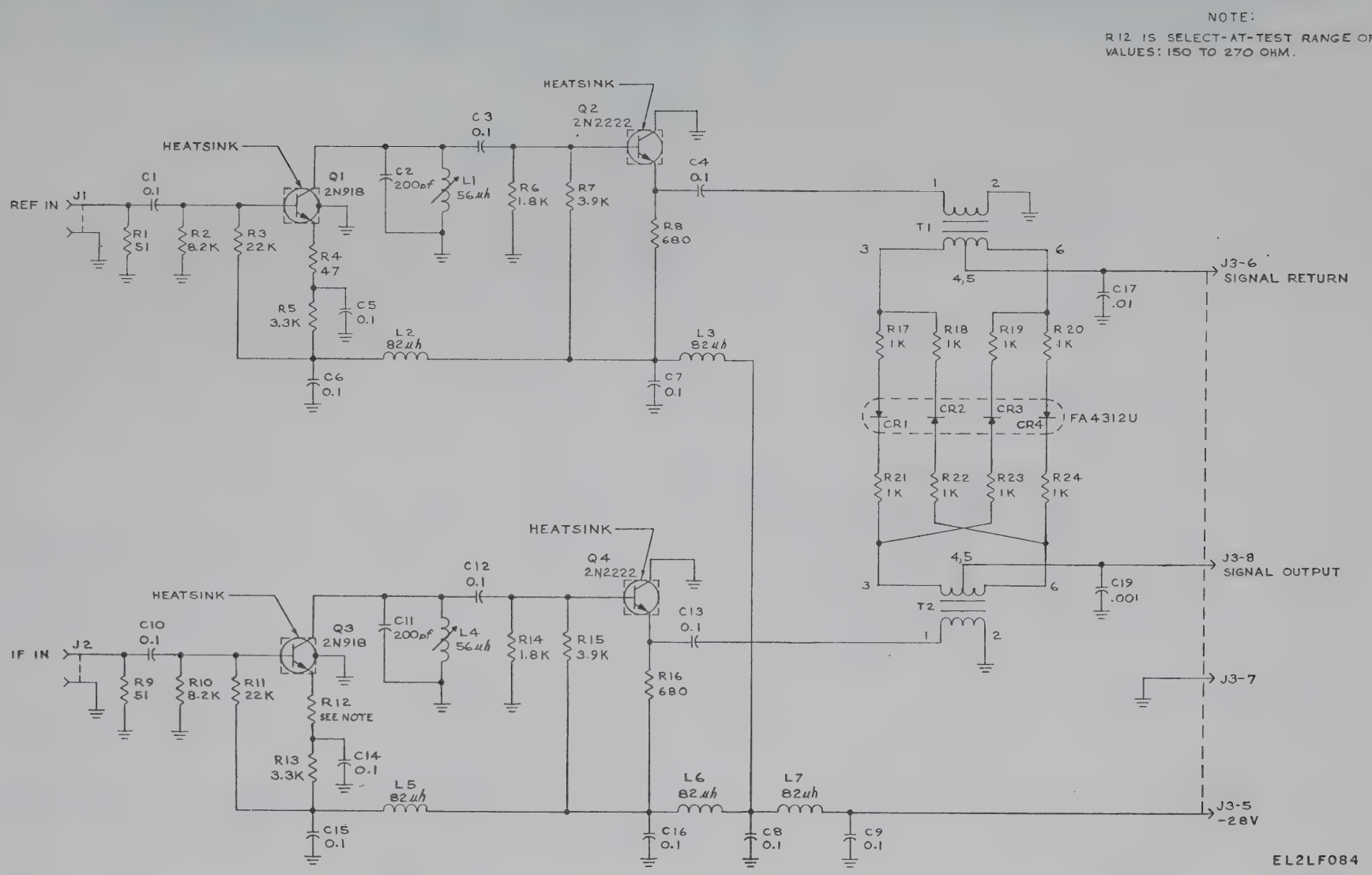


Figure 3-42. 1-4 MHz loop phase detector 1A3A3A36, schematic diagram.

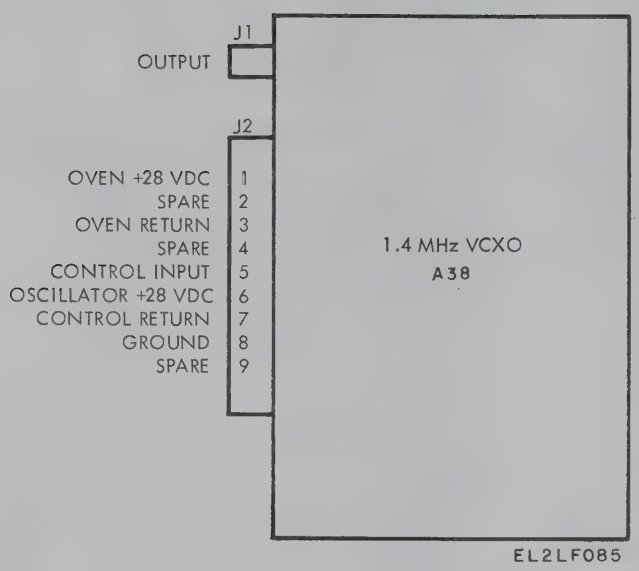


Figure 3-43. 1-4 MHz VCXO 1A3A3A38, input/output signal characteristics.

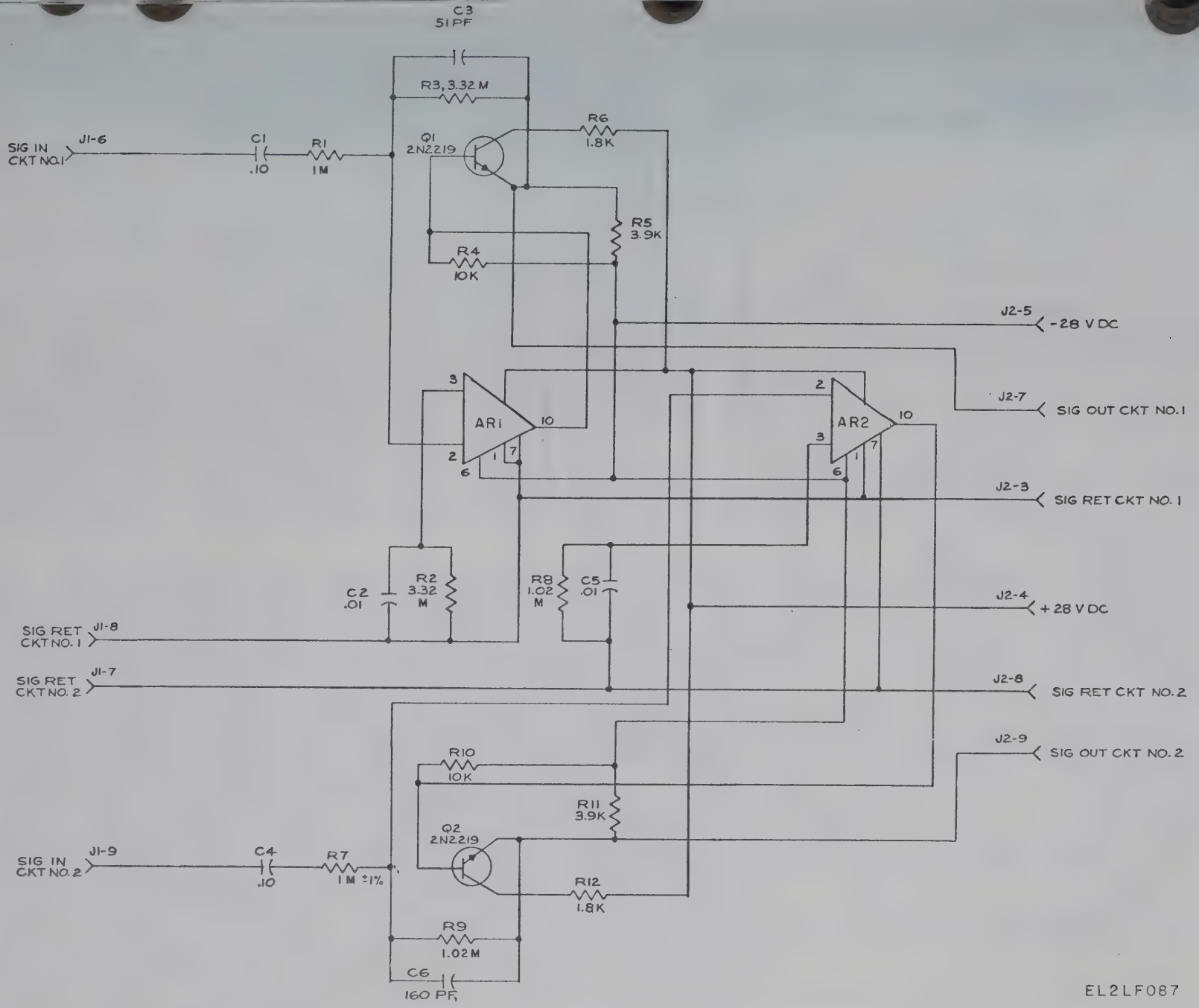


Figure 3-44. Am. amplifier 1A3A3A44, schematic diagram.

x. The power supply monitoring circuit A47 (fig. 3-45) monitors the ±15 vdc (PS2), −15 vdc (PS3), +28 vdc (PS1), and −28 vdc (PS4) power supplies. The monitoring circuit consists of four relays, each of which is equipped with an arc-suppression diode. When a power supply is operating properly, a voltage level is applied to the coil of the respective relay. With the relay energized, a 28 vdc unregulated level is applied through the normally open contacts to illuminate the respective power supply indicator.

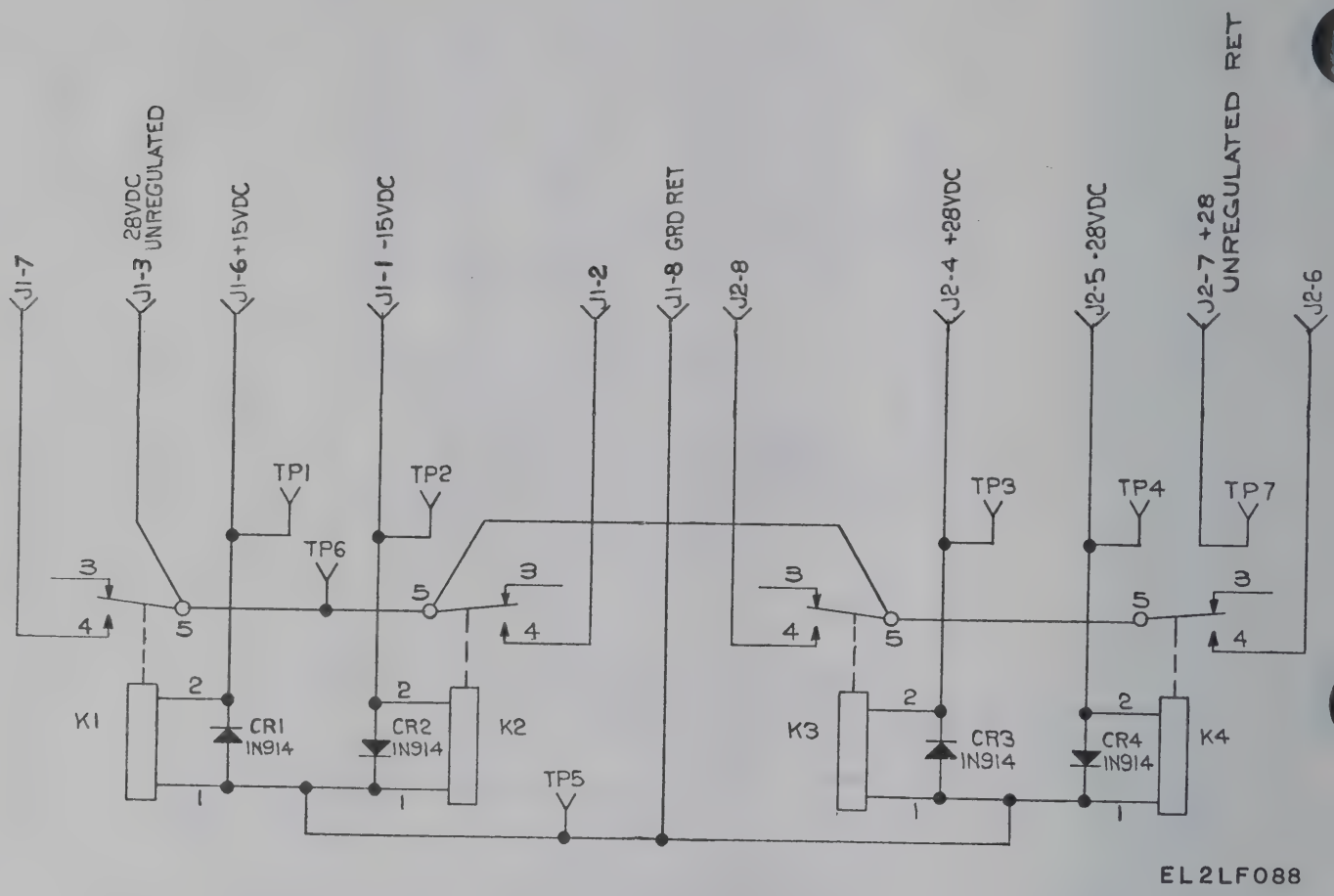


Figure 3-45. Power supply monitoring circuits 1A3A3A47, schematic diagram.

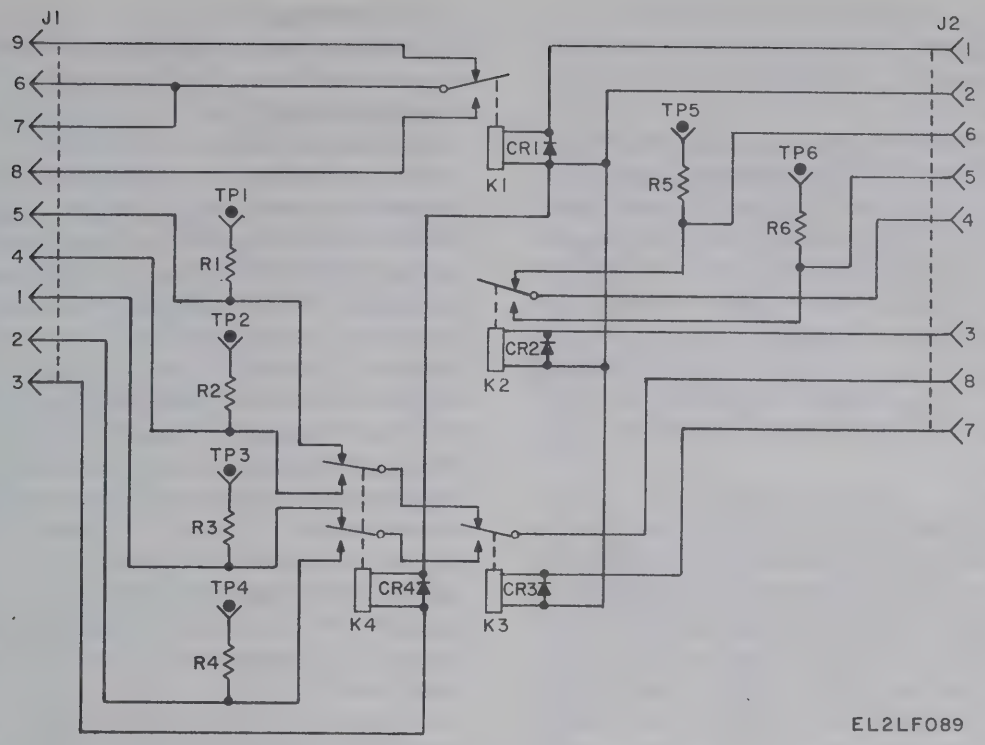


Figure 3-46. Relay A48, schematic diagram.

3-16. Beacon Demod 1A3A4 Circuit Analysis

(fig. 3-47 through 3-55 and FO 3-22 through FO 3-29)

The beacon demod of the AN/TSC-54 provides tracking error signals, a signal detect indication, and a signal strength indication to the antenna control circuits. The beacon demod also supplies an aural acquisition-aid signal to the baseband circuits and a satellite identification signal is available to drive an electronic counter. The beacon demod circuit analysis is presented in *a* through *q* below.

a. 50 kHz bandpass filter A6 (fig. 3-47) is a 3-section bandpass filter. Variable capacitors C2, C5 and C8 provide tuning.

b. The 1.4 MHz if. amplifier A13 receives the 1.4 MHz if. signal from the selected bandpass filter, and it provides three amplified 1.4 MHz if. outputs and a detected envelope output. The circuit diagram is shown on figure FO 3-23. The 1.4 MHz if. amplifier is comprised of five cascaded tuned amplifier stages which are tuned for maximum response at 1.4 MHz. The amplifier has a gain of 70 dB and a 1 dB bandwidth of ±20 kHz.

(1) The 1.4 MHz if. signal is applied through jack J1 and is coupled through capacitor C1 to the base of amplifier transistor Q1. Resistor R1 provides the proper input impedance match for the input signal. Resistors R2 and R3 form a voltage divider connected between -15 vdc and ground. This divider network provides the dc bias voltage (Vce) for transistor Q1. Inductor L1, capacitors C3 and C4, and resistors R6 form a parallel resonant tank circuit. Resistor R6 increases the bandwidth of the stage by lowering the Q factor of inductor L1. Collector current for transistor Q1 is controlled by emitter resistor R5 which is bypassed by capacitor C2. Emitter resistor R4 provides degeneration for, and controls the gain of, the transistor Q1 amplifier stage. The output of the transistor Q1 amplifier stage is taken from the junction of capacitors C3 and C4 to provide the proper impedance match to the input circuit of transistor Q2. The transistor Q2, Q3, Q4 and Q5 stages operate the same as transistor Q1. The signal at the collector of transistor Q5 is rectified by diode CR1, and the resulting dc voltage is filtered by the network comprised of capacitors C20 and C21, inductor L12, and resistor R30.

(2) The output at jack pin J5-6 is a negative dc voltage which represents the detected envelope. To provide the proper output impedance, the if. output is taken from the junction of capacitors C19 and C22 and is applied through a 3-way power divider, composed of resistors R26, R27, R28 and R29, to connectors J2, J3, and J4. Inductors L2, L4, L6, L8, L10, and L11 and capacitors C6, C7, C13, C17, C23, C24 and C25 form decoupling networks to prevent the if. signal from feeding into the dc power source.

c. Frequency multiplier A37 consists of three X2 multiplier circuits housed in the one unit. Each section receives 1.4 MHz input and provides 2.8

MHz output. Source and load impedances are 50 ohms, nominal. The unit requires +15 vdc for operating voltage. The frequency multiplier is a nonrepairable item.

d. The two 2.8 MHz loop phase detectors (A15 and A16) contain identical circuitry, but operate in different modes. The 2.8 MHz loop phase detector in the phase lock loop (A15) functions as a phase detector for the 2.8 MHz if. signal and a 2.8 MHz 90° phase reference signal. The other 2.8 MHz loop phase detector (A16) functions as an am. mixer/detector for the 2.8 MHz if. signal and a 2.8 MHz 0° phase reference signal. The circuit (fig. FO 3-24) consists of two nearly identical amplifiers and a phase detector.

(1) Operating voltage for the active components on the module is -28 vdc applied at J3-5 and filtered by pi filter L7, C8, and C9. Except for gain, the two amplifier boards are identical; therefore, only the amplifier in the reference leg will be discussed. A 2.8 MHz reference signal is applied at J1. Resistor R1 sets the input impedance at 50 ohms. Capacitor C1 couples the signal to the base of transistor Q1. Bias resistors R2 and R3 set the operating point of the transistor. The tank (C2 and L1) in the collector circuit of Q1 is resonant at 2.8 MHz. The gain of Q1 is approximately 10 db higher than that of Q3. Capacitor C3 couples the 2.8 MHz reference signal to the base circuit of emitter follower Q2. Resistor R17 prevents oscillations. The signal is then coupled from the emitter of Q2 to the primary of T1 on the phase detector board.

(2) The phase detector board operates in either of two modes depending upon the phase relationship between the if. signal and the reference signal. Consider first 2.8 MHz loop phase detector A15 in the phase lock loop. The reference signal is displaced 90° from the if. signal and the phase detector board functions in the phase detector mode. As long as this phase relationship is maintained, the output of the phase detector board is zero and the two signals are phase locked. If the if. starts to change frequency, the phase relationship between the two signals changes. A dc error voltage is produced that is proportional to the phase difference between the two signals. This error voltage causes the frequency of the reference signal to shift slightly, tracking the phase of the if. signal.

(3) Consider next 2.8 MHz loop phase detector A16, which functions as an am. mixer detector. The phase detector board on module A16 receives a 0° phase reference signal and the if. signal. The output is a coherent dc voltage of approximately +1 volt. Any modulation that is present on the if. signal, causes the dc voltage to vary at an audio rate and produce an envelope signal which contains the 25 Hz tracking signal.

e. Module A17 (fig. 3-48) is a 90 degree differential phase shifter which provides reference signals for 2.8 MHz loop phase detectors A15 and A16. The 2.8 MHz input at J1 is from frequency multiplier A37. The output at J2 lags the input by 45 degrees, while the output at J3 leads the input by 45 degrees.

f. The 2.8 MHz loop amplifier A20 (fig. 3-49) receives the error voltage from the phase detector, amplifies the error voltage, and applies a control voltage to the 1.4 MHz vcxo to correct the vcxo frequency. The loop amplifier is comprised of three resistors, one capacitor, and an operational amplifier. The reference terminal of operational amplifier AR1 is grounded through resistor R1 which is bypassed by capacitor C1. The signal input is applied to terminal 2 of amplifier AR1, and the output at terminal 10 of amplifier AR1 is applied to output pin 7 of jack J1. Resistor R2 is the load resistor connected to -28 vdc and terminal 10 of amplifier AR1. Resistor R2 is the load resistor connected to -28 vdc and terminal 10 of amplifier AR1. Resistor R3 isolates test point TP1 from the output signal line.

g. The signal detect circuit A22 (fig. FO 3-25) receives the detected envelope signal from the 1.4 MHz if. amplifier, and provides a 4-second signal detect signal to the antenna control circuits and to the phase lock detect and sweep stop. The signal detect is comprised of two operational amplifiers, a monostable multivibrator, and associated circuit components. Operational amplifier AR1 is used as a smoothing filter and amplifier AR2 is used as a level detector. The output of the level detector drives the monostable multivibrator circuit which is comprised of operational amplifier AR3 and transistor Q1.

(1) In the quiescent condition, transistor Q1 is cut off, relays K1 and K2 are deenergized, and the signal detect indication is not produced. Operational amplifiers AR1, AR2, and AR3 are identical and have been discussed previously; therefore, only the external components pertaining to their operation in the signal detect circuit are discussed here. The detected envelope signal is applied through resistor R1 to the inverting input (pin 2) of amplifier AR1. The noninverting input (pin 3) is grounded. Capacitor C1 and resistor R1 form a feedback network which controls the gain of amplifier AR1. The output of amplifier AR1 is integrated by resistor R3 and capacitor C2 and is applied to the noninverting input (pin 3) of amplifier AR2. The reference bias is applied to the inverting input (pin 2) of amplifier AR2. The reference bias is obtained from a bias network comprised of resistors R10 through R16 connected across +28 vdc and ground and relays K3 and K4. Relays K3 and K4 are controlled by the mode select switch on the front panel of the beacon demodulator.

(2) When the normal mode of operation is selected, relay K3 is energized and the reference bias for amplifier AR2 is taken from the wiper arm of potentiometer R14. This is the maximum reference bias obtainable from the bias network. When the last ditch communication mode of operation is selected, relay K4 is energized and the reference bias for amplifier AR2 is taken from the junction of resistors R11 and R12. When the last ditch beacon mode is selected, relays K3 and K4 are both deenergized and the voltage at the junction of resistors R10 and R11 is applied as the reference bias to amplifier AR2. The bias voltages at the junction of resistors R11 and R12 and the junction of resistors R10 and R11 are progressively lower than the bias voltage from potentiometer R14. These lower voltages allow the level detector output to trigger the monostable multivibrator for lower input signal levels. When the input signal at pin 6 of jack J1 is of sufficient level, the output of operational amplifier AR1 causes the output of operational amplifier AR2 to go maximum positive. The output of amplifier AR2 is clamped to a ground reference by diode CR1. The positive output of amplifier AR2 is applied through resistor R6 to the noninverting input (pin 3) of operational amplifier AR3, which is part of the monostable multivibrator. The positive output of amplifier AR3 turns on transistor Q1. The base of transistor Q1 is clamped to ground by diode CR2.

(3) When transistor Q1 conducts, a ground return path is provided for relays K1 and K2 and capacitor C3 is charged to the positive supply voltage through resistor R7 and the contacts of relay K1. This produces a positive voltage at the inverting pin of amplifier AR3 and ensures that the output of amplifier AR3 is initially negative and that transistor Q1 is cut off. After capacitor C3 has charged, the voltage at the inverting input (pin 2) of amplifier AR3 returns to 0 volt. When transistor Q1 conducts by the application of a positive output of amplifier AR3, capacitor C3 discharges through resistor R7, the closed contacts of energized relay K1, the positive supply, and transistor Q1. This develops a negative voltage across resistor R7 which is applied to the inverting input of amplifier AR3. This negative voltage is present for the time constant period of capacitor C3 and resistor R7 and holds the output of amplifier AR3 positive for approximately 4 seconds.

(4) After 4 seconds, the inverting input returns to 0 volt and the output of amplifier AR3 goes negative. This negative voltage is applied through resistor R8 to the base of transistor Q1, cutting off Q1. The negative voltage at the base of transistor Q1 forward biases diode CR2 and the forward resistance of the diode holds the base slightly negative. For the 4-second period that transistor Q1 is conducting, the output at jack pin J1-7 is 0 volt; and when transistor Q1 is cut off, the output returns to +28 vdc. When relay K2 is energized, the closed contacts of relay K2 connect pins 7 and 9 of jack J2. This circuit closure is applied to the antenna control circuits for 4 seconds as a signal detect indication.

h. The 1.28 MHz/120 kHz mixer A25 receives a 1.28 MHz satellite identification signal from the 50 kHz bandwidth filter and a 1.4 MHz signal from the 1.4 MHz vcxo, and produces a 120 kHz output. The mixer circuit, as illustrated in figure 3-50, is comprised of a 1.4 MHz buffer amplifier, a balanced diode mixer, and a 120 kHz output amplifier.

(1) The 14. MHz signal is coupled through capacitor C2 to the base of buffer amplifier transistor Q1. The signal is amplified and the output is taken from tapped load transformer T3 and is applied to the primary winding of balanced mixer transformer T1. Resistor R1 provides the proper impedance match for the input signal. Resistors R2 and R3 provide the dc bias voltage for transistor Q1. Collector current is controlled by emitter resistor R11 which is bypassed by capacitor C9. Emitter resistor R4 provides degeneration to stabilize the gain of transistor Q1. The 1.28 MHz signal is first applied through a resistive T attenuator network comprised of resistors R13, R14 and R15, and then through a pi impedance matching filter comprised of inductors L1 and L2 and capacitor C1 to the center tap of the transformer T1 secondary winding. The 1.28 MHz and 1.4 MHz singnals are heterodyned in the balanced mixer comprised of diode CR1A, CR1B and transformer T1. The difference frequency of 120 kHz is selected by the pi filter comprised of capacitors C4 and C5 and inductor L4. The output of the filter is developed across load resistor R6. The 120 kHz signal at resistor R6 is coupled through capacitor C6 to the base of buffer amplifier transistor Q2.

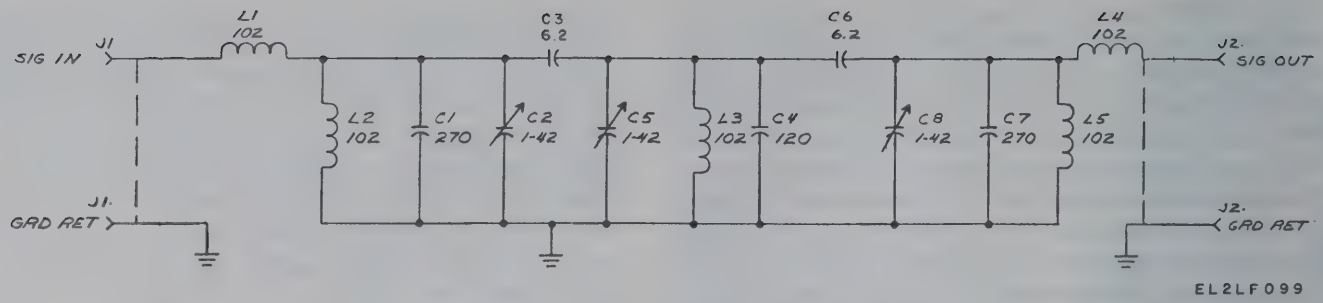


Figure 3-47. 50 kHz bandwidth filter 1A3A4A6, schematic diagram.

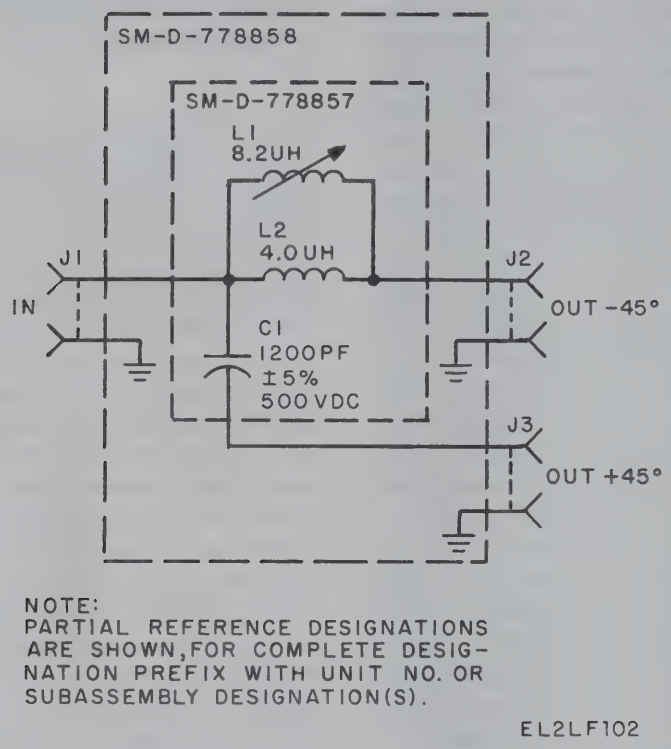


Figure 3-48. 90 degree differential phase shifter 1A3A4A17, schematic diagram.

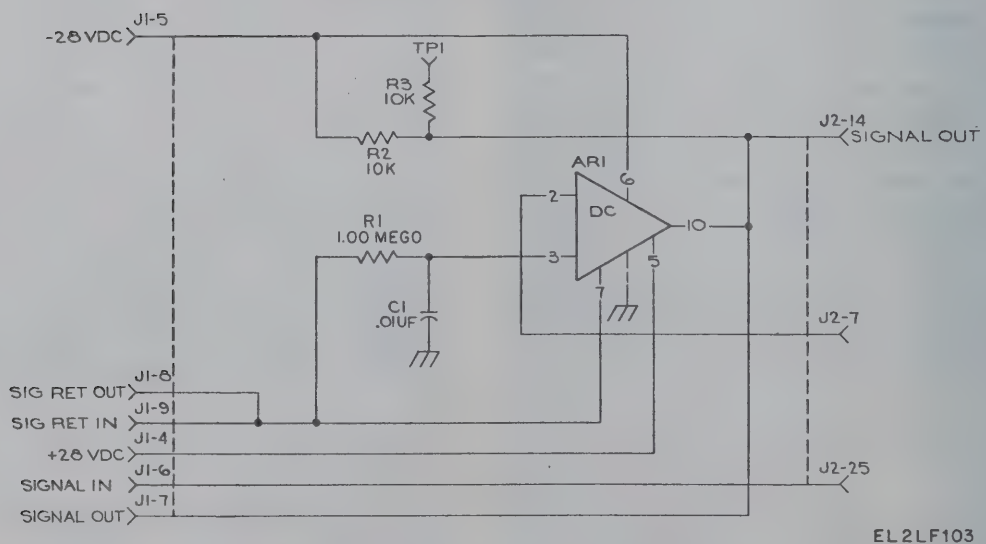


Figure 3-49. 2.8 MHz loop amplifier 1A3A4A20, schematic diagram.

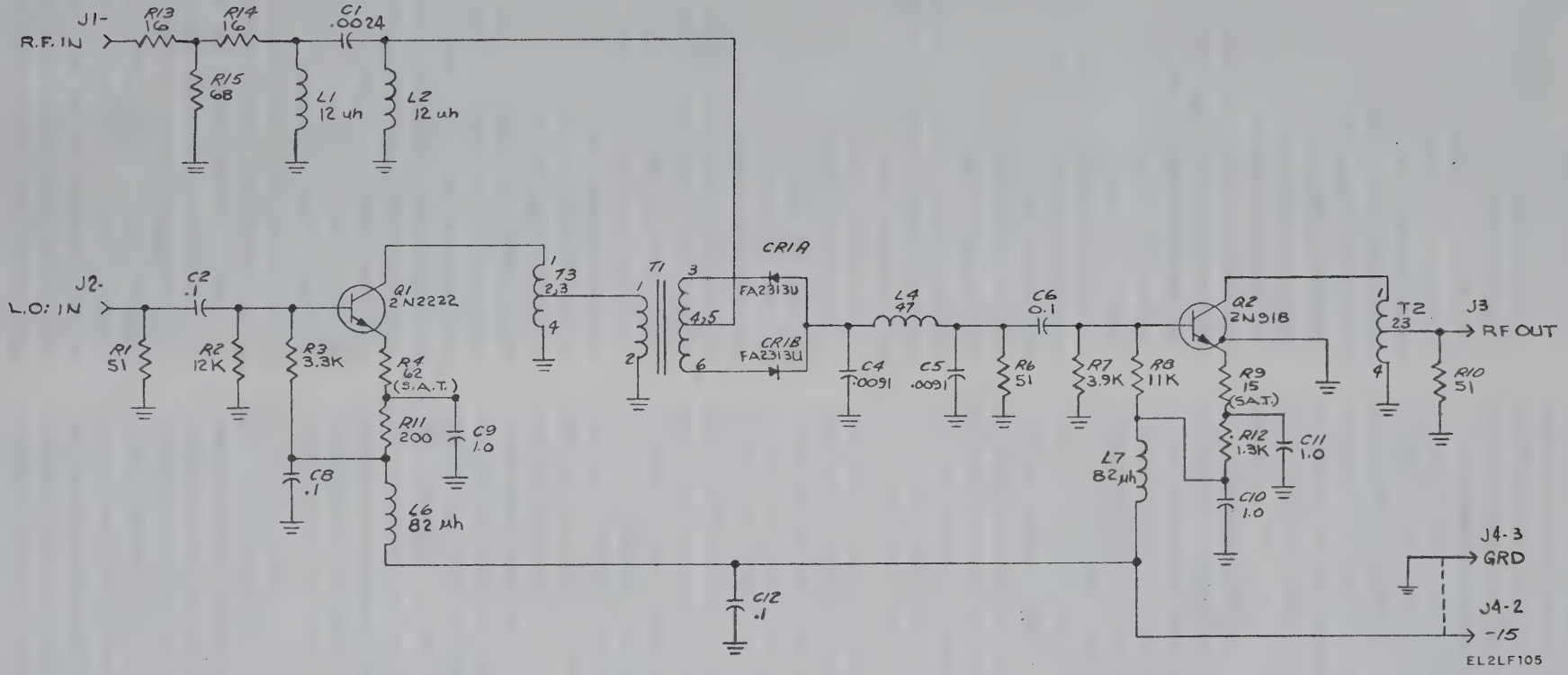


Figure 3-50. 1.28 MHz/120 kHz balanced mixer 1A3A4A25, schematic diagram.

(2) The operation of transistor Q2 is the same as that of transistor Q1. The output is taken from a tap on transformer T2 and is applied to output jack J3. Resistor R10 provides the proper output impedance. Capacitors C8, C10 and C12 and inductors L6 and L7 form decoupling networks to prevent the rf from feeding into the dc power source.

i. The 120 kHz filter/amplifier A27 (fig. FO 3-26) receives the 120 kHz signal from the 1.28 MHz/120 kHz mixer and provides a filtered and amplified 120 kHz output. A 3 dB bandwidth of 32 kHz centered at 120 kHz is provided so that all satellite identification frequencies between 110 kHz and 120 kHz may be passed.

(1) The 120 kHz input is applied to a bandpass filter comprised of variable inductors L1 and L2 and capacitors C1, C2 and C3. Inductors L1 and L2 are tuned to provide the proper response curve. The output of the filter is coupled through capacitor C4 to the base of tuned amplifier transistor Q1. The dc bias (Vce) for transistor Q1 is provided by resistors R1 and R2 which are connected between -15 vdc and ground. Collector current for transistor Q1 is controlled by emitter resistors R3 and R4. Resistor R4 is bypassed by capacitor C5. Emitter resistor R3 provides degeneration to stabilize the amplifier gain. The collector load is a parallel resonant tank circuit which is comprised of variable inductor L3, resistor R5, and capacitors C7 and C8. Inductor L3 is tuned for a maximum response at 120 kHz. Resistor R5 controls the response of the tank circuit by lowering the Q factor of inductor L3. To provide the proper output impedance from the tank circuit, the signal is taken from the junction of capacitors C7 and C8 and is applied through series peaking variable inductor L5 to the base of amplifier transistor Q2.

(2) The operation of transistor Q2 is the same as the operation of transistor Q1. The output of the transistor Q1 amplifier stage is applied through an impedance matching network comprised of capacitors C14 and C15 and inductor L8 to the 2-way power divider consisting of resistors R12, R13, and R14. The power divider outputs are applied to output jacks J3 and J4. Inductors L4 and L7, and capacitors C6, C10 and C12 form decoupling networks that prevent the rf from feeding into the dc supply.

j. The 120 kHz loop phase detector A28 (fig. FO 3-27) receives three 120 kHz signals; two are phase 0° and one is phase 90°. The 120 kHz phase 0° input at jack J2 is compared with the 120 kHz phase 90° input at pins 6 and 7 of jack J3. If the two signals are not 90 degrees apart, an error voltage is produced at jack pin 9. This error voltage is used to correct the 480 kHz vco frequency. The 120 kHz phase 0° input at jack J2 is also compared with the 120 kHz phase 0° input at pins 8 and 9 of jack J3. When these two signals are in phase, a dc voltage is developed at jack pin 7 that is used to generate a sweep stop voltage.

(1) The 120 kHz phase 0° signal is amplified by common emitter amplifier transistor Q2. Resistor R3 provides the proper input impedance. Collector current is controlled by emitter resistor R6 which is bypassed by capacitor C6. Degeneration for gain stabilization is provided by emitter resistor R4. The output of transistor Q2 is applied through emitter follower transistor Q1 for impedance matching. The output of transistor Q1 is coupled through capacitors C5 and C7 to the primary windings of transformers T1 and T2, respectively. The secondary winding of transformer T1 is center tapped to ground. Zener diodes CR1 and CR2 are connected across the secondary windings of transformer T1 to prevent the voltage from exceeding 7.5 vdc.

(2) The signal appearing across transformer T1 secondary winding 3 and 4 is applied to terminal 8 of chopper G1. The signal appearing across transformer T1 secondary winding 5 and 6 is of the opposite polarity from the 3 and 4 winding and is applied to terminal 8 of chopper G2. The 120 kHz phase 90° signal is applied across terminals 4 and 5 of choppers G1 and G2. The terminal 2 outputs of the choppers are pulsed dc voltages. The output of G1 is of opposite polarity to the output of G2. When the two 120 kHz input signals have a phase difference of 90 degrees, the two outputs are opposite in polarity and equal in amplitude; therefore, they cancel each other. Under this condition, the output at jack pin J1-9 is 0 volts. When one of the 120 kHz input signals varies in phase, the combination of the two outputs will be either negative or positive depending upon the direction of phase error.

(3) The error voltage is filtered by the filter network comprised of inductors L1 and L2, capacitors C1, C2 and C3, and resistor R1 to provide a steady dc. The filtered dc signal is applied to jack pin J1-9 as an error voltage. The operation of choppers G3 and G4 is similar to choppers G1 and G2, except that both input signals are 120 kHz phase 0°. When these two signals are in phase, the outputs at chopper terminal G3-2 and G4-2 are both positive; therefore, they add to produce a positive dc level. This positive voltage is filtered by resistor R7 and capacitor C9 and is applied to jack pin J1-7.

k. the ID sweep, loop filter, and acquisition circuits A29 receive two dc inputs from the loop phase detector and provide a vco control voltage output, a counter enable output, and a phase lock signal output when the ID loop is phase-locked. The circuit is illustrated in figure FO 3-28. When the loop is not locked, the unit provides a ramp sweep voltage which is used to sweep the 480 kHz vco. The dc input error voltage is applied through pin 4 of jack

J1 to an input filter comprised of capacitor C1 and resistors R1 and R3. The filter eliminates fast changing components of the input voltage. The filter output is applied to the inverting input (pin 2) of operational amplifier AR1. The non-inverting input (pin 3) is referenced to ground through resistor R6. The output of operational amplifier AR1 is developed across load resistor R7 and applied through resistor R4 to the inverting input (pin 2) of operational amplifier AR2. The noninverting input (pin 3) is referenced to ground through resistor R9. The amplified error output of amplifier AR2 is applied to jack pin J2-8 as a vco control voltage. Resistor R2 and capacitor C3 form a feedback network which controls the response of amplifier AR2.

(1) During the time that the input at pin 6 of jack pin J1 is amplified by amplifiers AR1 and AR2, the sweep circuit associated with operational amplifier AR3 is disabled by the output of the level detector circuit comprised of operational amplifier AR4, transistors of Q2 and Q1, and their associated circuit components. At this time, the input at jack pin J1-7 is a positive dc voltage that is filtered by resistor R26 and capacitor C6. The filtered dc voltage is applied to the noninverting input (pin 3) of amplifier AR4. Amplifier AR4 is used as a level detector. When the positive voltage input to amplifier AR4 reaches a preset level, the output of amplifier AR4 is clamped to a maximum positive voltage. The detector reference level at pin 2 is established by a voltage divider comprised of resistor R24 and potentiometer R30. The voltage at the wiper arm of potentiometer R30 is applied through resistor R29 to pin 2 of amplifier AR4. Resistor R29 and the set portion of potentiometer R30 are bypassed by capacitor C8.

(2) The positive output of amplifier AR4 is applied through resistor R27 to the base of transistor Q2 and also through isolation diode CR8 and resistor R28 to the base of transistor Q3. This positive voltage turns on transistor Q2 and the collector goes negative. The emitter of transistor Q2 is referenced to −7.5 vdc by a voltage divider comprised of breakdown diode CR11, capacitor C4, and resistor R22. Diode CR7 prevents the base emitter breakdown voltage from being exceeded. Capacitor C5 provides collector-to-base feedback to stabilize the switching function. The negative voltage at the collector of transistor Q2 is applied through dropping resistor R20 to the base of transistor Q1, turning on transistor Q1. This places a ground at the junction of resistors R10 and R15. The ground is applied through resistors R10 and R5 to pin 2 of operational amplifier AR1. This prevents the output of operational amplifier AR3 from being applied to amplifier AR1 and thus prevents the amplifier AR3 and AR1 circuits from oscillating.

(3) The positive voltage at the base of transistor Q3 turns on transistor Q3 and energizes collector load relay K1. Diode CR10 prevents the base emitter breakdown voltage from being exceeded, and capacitor C7 provides collector to base feedback to stabilize the switching function. Diode CR9 suppresses switching transients across the armature of relay K1. When relay K1 energizes, ground is removed from jack pin J2-8, enabling an external counter and jack pins J2-4 and J2-6 are shorted together to provide a phase lock indication. When the input at jack pin J1-7 decreases below the detection level, the output of amplifier AR4 goes negative. This negative voltage turns off transistors Q2 and Q3. With transistor Q3 turned off, relay K1 is deenergized, and the counter enable and phase lock signals are not provided at the output. When transistor Q2 is turned off, the positive collector voltage is applied through diode CR6 to transistor Q1, turning off transistor Q1.

(4) Assuming at this time that the output of amplifier AR3 is negative, a negative voltage will develop across resistor R16, which is part of a voltage divider comprised of resistors R17, R11, R14 and R16. This negative voltage is applied through resistors R15, R10, and R15 to pin 2 of amplifier AR1 causing the output to start going positive and the integrating capacitor starts charging. The positive-going ramp voltage at the output of amplifier AR1 is applied across potentiometer R13 and resistor R19. The set voltage at the wiper of potentiometer R13 is applied through dropping resistor R12 to noninverting input (pin 3) of operational amplifier AR3. Diodes CR4 and CR5 limit the amplitude of the negative and positive voltages at pin 3 to the drop across the forward resistance of the diodes. The positive voltage at pin 3 causes the output of amplifier AR3 to go positive. This output is clipped at +10 vdc by quad diode CR13 and breakdown diode CR3. The positive voltage developed across diode CR3 is applied through forward biased diodes CR2 and CR1 and resistor R5 to pin 2 of amplifier AR1. This causes the ramp voltage at the output of amplifier AR1 to go negative which in turn causes pin 3 of amplifier AR3 to go negative.

(5) The resulting negative output of amplifier AR3 is clipped at −10 vdc by quad diode CR13 and breakdown diode CR3. The negative voltage is developed across resistors R14 and R16. A negative voltage developed at the junction of resistors R14 and R16 is applied through resistors R15, R10 and R5 to pin 2 of amplifier AR1 causing the output of amplifier AR1 to start going positive. This action completes one cycle of operation. The difference in amplitude of the negative and positive square wave inputs to pin 2 of amplifier AR1 results in a 15-second duration positive-going ramp voltage

and a 1.5-second duration negative-going ramp voltage at the output of amplifier AR1. This function continues until the input at pin becomes sufficient to cause the output of amplifier AR4 and transistor Q2 to turn on transistor Q1. The sweep output of amplifier AR1 is amplifier and inverted by amplifier AR2, and the output is a negative-going ramp voltage which varies from +7.5 vdc to −7.5 vdc in 15 seconds and returns to +7.5 vdc in 1.5 seconds.

l. The 4-to-1 countdown and quadrature circuit A30 (fig. FO 3-29) receives the 480 +40 kHz output of the 480 kHz vco and provides two 120 ±10 kHz outputs. These outputs are 90 degrees apart and at the satellite identification frequency. The two outputs are used by the ID loop phase detector. A third output provided by the unit is used by an electronic counter to display satellite id.

(1) The 480 ±40 kHz intput at jack J1 is coupled through capacitor C1 and dropping resistor R3 to pins 7 and 9 of integrated circuit device A1. Resistors R5 and R6 form a voltage divider connected between −15 vdc and ground. The divider provides a negative reference level for pins 7 and 9. The integrated circuit device is a flip-flop circuit which divides the input frequency by a factor of 2 and provides a 240 kHz phase 180° output at pin 5 and a 240 kHz phase 0° output at pin 4. The output at pin 5 is applied to pins 7 and 9 of integrated circuit device A2, while the output at pin 4 is applied to pins 7 and 9 of integrated circuit device A4. Integrated circuit devices A2 and A4 contain flip-flop circuits which divide the 240 kHz input frequency by a factor of 2 and provide a 120 kHz output at pin 5. Due to the countdown process, the two kHz signals have a phase relationship of 90 degrees.

(2) The output circuits associated with integrated circuit devices A2 and A4 are almost identical; therefore, the circuit associated with integrated circuit device A2 is covered in detail and only the differences in the integrated circuit device A4 output circuits are covered. The 120 kHz phase 90° output of integrated circuit device A2 is applied through resistor R7 to the base of emitter follower transistor Q2. Transistor Q2 contains two npn transistor elements. The first element is connected as an emitter follower and the second element is connected as a common base amplifier. The signal developed across emitter resistor R9 is directly coupled to the emitter of the common base amplifier. Base emitter bias is applied through base resistor R10 from pin 1 of integrated circuit device A3. The amplifier signal is taken from the junction of collector resistors R1 and R4 and is directly coupled to the base of amplifier transistor Q1. Diode CR1 prevents the reversed emitter base breakdown voltage from being exceeded. The signal at the collector of transistor Q1 is applied as feedback through capacitor C5 and resistor R8 to the base of transistor Q2 to provide gain stabilization. The output of transistor Q1 is directly coupled to the base of transistors Q3 and Q4 which are connected as a complementary symmetry circuit.

(3) This circuit has the advantages of a push-pull circuit without the requirement for a center tapped output transformer. The base emitter forward bias for transistors Q3 and Q4 is obtained from the forward resistance voltage drop across diodes CR2 and CR5. The diodes are forward biased by the negative voltage from resistor R11 which is also the collector resistor for transistor Q1. The output at the emitter emitter of transistors Q3 and Q4 is coupled through capacitor C6 to output transformer T1 which provides 120 kHz phase 90° isolated output signal. The 120 kHz phase 90° signal at the emitter of transistors Q3 and Q4 is also coupled through capacitors C9 and C10 and resistor R18 to pin 6 of integrated circuit device A4. A negative dc reference is applied to pin 6 by the voltage divider comprised of resistors R13 and R17. The 120 kHz phase 90° signal sets the flip-flop in integrated circuit device A4 to be sure that the 120 kHz output at pin 5 has the proper phase of 0 degrees. Resistors R2 and R12 are collector resistors, and capacitors C4 and C8 are bypass capacitors.

(4) The output of 120 kHz phase 0° circuit is taken from the emitter of transistors Q7 and Q8 and coupled through capacitor C15 and transformer T2 to provide a 120 kHz phase 0° isolated output. The signal is also coupled from the emitter of transistors Q7 and Q8 by capacitor C13 and resistor R22 to jack J3 to provide the satellite identification output signal to the electronic counter. Bias voltages for the unit are provided by integrated circuit device A3, transistor Q3, and associated circuit components. Resistor R14, diode CR4 and 5.1 volt breakdown diode CR3 provide the dc forward bias for the base of transistor Q5. Collector resistor R15, transistor Q5, and integrated circuit device A3 form a voltage divider connected between −15 vdc and ground. The −5.2 vdc is developed across integrated circuit device A3. This voltage is applied to pin 2 of integrated circuit devices A1, A2 and A4. Approximately −1 vdc is developed at pin 1 of integrated circuit device A3. This voltage is applied to resistors R10 and R23. Integrated circuit device A3 is bypassed by capacitor C7.

m. Integrated circuit devices A1 and A2 are used in the 4-to-1 countdown and quadrature unit to provide a 2-to-1 countdown function. The input and output signals are shown in figure 3-51. The npn transistors used in the circuit have their collectors returned to ground at pin 3 while the emitters are returned to −5.2 vdc at pin 2. The circuit of the unit is basically a bistable multivibrator (flip-flop). The

inputs and outputs of the flip-flop are buffered by emitter followers. Set and reset circuits are provided to control the initial flip-flop state.

(1) The flip-flop is comprised of transistors Q6 through Q11, collector load resistors R1 and R2, base biasing resistors R4, R6, R10 and R11, and emitter resistors R3 and R5. Parallel connected transistors Q1 and Q2, emitter resistor R9, and coupling capacitor C1 form one input emitter follower stage. The second input emitter follower stage is comprised of parallel connected transistors Q15 and Q16, emitter resistor R12, and coupling capacitor C2. The output emitter followers are transistor Q3 and emitter resistor R7, and transistor Q14 and emitter resistor R8. The set circuit is comprised of transistors Q5 and Q4 and resistor R13, while the reset circuit is comprised of transistors Q12 and Q13 and resistor R14. The input frequency to be counted down is applied to pins 7 and 9. The input emitter followers conduct when power is applied and pass only the negative half-cycles of the input frequency.

(2) Initially assuming that the transistors Q6 and Q7 portions of the multivibrator are turned on and the transistors Q10 and Q11 portions are turned off, the following action occurs:

(*a*) The negative half-cycle of the input signal at the base of transistor Q1 reverse biases the base emitter junction and a negative pulse is developed across the emitter resistor R9. This negative pulse is coupled through capacitor C1 to the base of saturated transistor Q6, cutting off Q6. This causes the transistor Q6 collector to go positive which causes transistor Q8 to conduct through resistor R4. This develops a positive voltage across resistor R4 which turns on transistor Q10 causing the collector of Q10 to go negative. The negative collector voltage cuts off transistor Q9 which causes the base of transistor Q7 to go negative, driving the transistor Q6-Q7 side of the multivibrator further into cutoff. As the negative pulse is developed at the emitter of transistor Q1, a negative pulse is also developed across resistor R12, due to the input at the base of transistor Q15. This negative pulse is coupled through capacitor C2 to the base of transistor Q11, but this pulse has no effect because Q11 is already cut off.

(*b*) The multivibrator is now in the state where the transistor Q6-Q7 side is cut off and the transistor Q10-Q11 side is turned on. On the negative half cycle of the input frequency, the negative output of the transistor Q1-Q2 emitter follower will not affect the multivibrator because the transistor Q6-Q7 side is cut off. However, the negative output from the transistor Q15-Q16 emitter follower will cut off transistor Q11 and cause the multivibrator to change state. In this manner, the multivibrator completes one flip-flop action for every two cycles of the input frequency. The bases of output emitter follower transistors Q3 and Q14 are connected to the collectors of transistor pairs Q6-Q7 and Q10-Q11, respectively. The output at the emitter (pin 4) of transistor Q3 is the complement of the output at the emitter (pin 5) of transistor Q14.

(3) A negative intput through pin 6 to the base of transistor Q5 causes the Q5 collector to go positive. This positive pulse is applied through emitter follower transistor Q4 to the base of transistor Q6 turning on Q6. This sets the multivibrator in a state with transistor Q6 and Q7 turned on and transistors Q10 and Q11 turned off. A negative input through pin 1 to the base of transistor Q12 causes the Q12 collector to go positive. This positive pulse is applied through emitter follower transistor Q13 to the base of transistor Q11, turning on Q11. This resets the multivibrator in the state with transistor Q10 and Q11 turned on and transistor Q6 and Q7 turned off.

n. The integrated circuit device (fig. 3-52) is essentially a voltage divider. Diodes D1 and D2 provide temperature compensation and, along with resistors R1 and R2, provide the dc bias for transistor Q1. The applied voltage is connected to pins 2 and 3. Pin 2 is the negative terminal and pin 3 is the positive terminal. Resistor R3 is the emitter resistor. The output is taken from the emitter of transistor Q1 and applied to pin 1.

o. The 480 kHz vco A31 is used in the beacon demod to provide a frequency which is phase locked to the incoming satellite identification frequency. The circuit is shown in figure 3-53. The output frequency is controlled over a limited range by a dc corrective voltage that is applied to jack pin J1-8. This correction voltage is derived by dividing the output frequency by a factor of 4 and comparing the phase of the resulting frequency with the satellite identification frequency (110 kHz to 130 kHz). Any detected phase difference produces a dc error voltage. This error voltage is used to correct the frequency of the 480 kHz vco. The frequency of the oscillations is controlled by varying the amount of charge and discharge of capacitor C2. Capacitor C2 changes through forward biased transistors Q1 and Q2 and discharges through transistor Q3.

(1) Transistor Q1 is forward biased by a voltage divider comprised of resistors R1 and R2 and Zener diodes CR2 and CR3. The voltage divider is connected between +28 vdc and −28 vdc. The two Zener diodes maintain a combined voltage drop of 17 volts. The dc correction voltage is applied through diode CR1 to the junction of resistor R1 and diode CR2. Diode CR1 is forward biased by the negative voltage appearing at the junction of diode CR2 and resistor R1. The voltage drop across resistor R2 determines the base to emitter forward bias

of transistor Q1; therefore, by applying a dc correction voltage to the voltage divider, conduction of transistor Q1 is varied accordingly. This determines the amount of charge developed across capacitor C2. Emitter resistor R3 is connected to +28 vdc.

(2) Transistor Q2 is forward biased by a voltage divider comprised of resistors R4 and R7, diode CR4, and bypass capacitor C1 connected between ground and +28 vdc. Diode CR4 provides temperature compensation. Resistor R6 and potentiometer R5 form the transistor Q2 emitter resistance. Potentiometer R5 is used for setting the emitter voltage to provide the center frequency reference voltage for capacitor C2. When power is applied, capacitor C2 starts developing a positive charge through transistors Q1 and Q2. This positive voltage is applied to the gate of FET Q4-A, and thus increases current flow through common source resistor R15 and drain resistor R10. The drain of FET Q4-A and the source of FET Q5 are maintained at +15 vdc by Zener diode CR7. The positive voltage across source resistor R15 reduces conduction through FET Q4-B and drain resistor R11, and the drain goes positive. This positive signal is applied to the gate of FET Q5.

(3) The gate of FET Q4-B is biased by a voltage divider network comprised of resistors R12 and R16 connected between ground and +28 vdc. The positive signal at the gate of FET Q5 increases the conduction through drain resistors R14 and R13. Resistor R14 is bypassed by capacitor C3. The junction of resistors R13 and R14 goes negative, and this negative signal is amplified by transistor Q6 and coupled through capacitor C5 to the base of complementary connected amplifier transistor Q7. Diode CR14 provides bias stabilization for transistor Q6. Zener diode CR12, resistor R18, and bypass capacitor C4 provide a +5.1 vdc emitter bias. Resistor R17 and 16 volt Zener diode CR13 provide the negative collector voltage. Diodes CR8, CR9, and CR10 and resistor R20 provide a −30 vdc forward bias for transistor Q8. Diode CR11 provides the +1 vdc forward bias for transistor Q7.

(4) The base of transistor Q7 is prevented from being driven more positive than +5 vdc by clamping diode CR6. The positive voltage at the base of transistor Q7 increases conduction through transistor Q7 and collector resistor R19. The collector of transistor Q7 is bypassed by capacitor C6. Transistor Q8 is cut off by the positive voltage across resistor R20 resulting from the increased conduction through diode CR11. The emitter of transistor Q7 goes positive and this voltage is fed through forward biased diode CR5 to the base of transistor Q3, turning on Q3 and allowing capacitor C2 to discharge through transistor Q3 producing a negative going voltage at the gate of FET Q4A. This negative signal is processed by FET Q4A, Q4B, and Q5, and amplifier transistor Q6, producing a negative voltage at the base of transistor Q7. This negative voltage reverse biases transistor Q7 and diode CR11. This allows the base of transistor Q8 to go negative turning on transistor Q8 and producing a negative voltage at the emitter of transistor Q8. The negative voltage is applied through diode CR5 to the base of transistor Q3, cutting off Q3 and allowing capacitor C2 to start charging to the positive level established by transistors Q1 and Q2. The oscillating function continues at a rate of 480 kHz ± the corrected frequency produced by the dc correction voltage applied to jack pin J1-8. Resistor R21 is the collector load for transistor Q8, and capacitor C7 is the collector bypass capacitor.

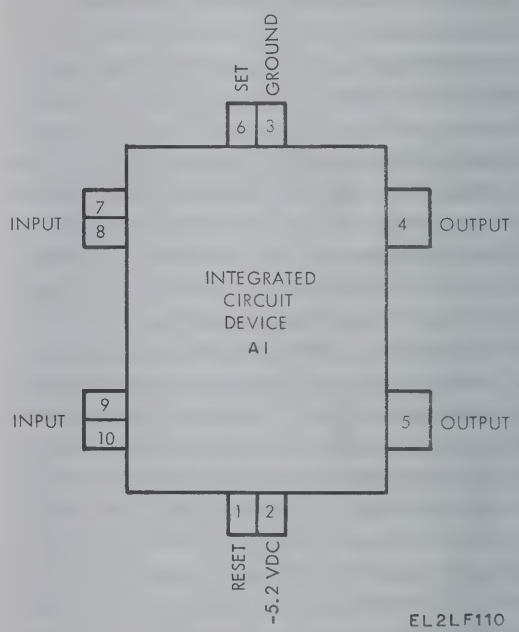


Figure 3-51. Integrated circuit device A1 and A2, input and output characteristics.

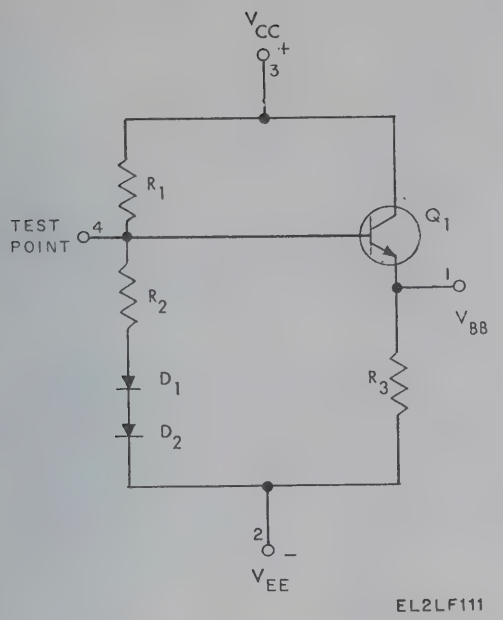


Figure 3-52. Integrated circuit device, schematic diagram.

p. The audio amplifier A32 (fig. 3-54) is used in the beacon demod to amplify and translate the detected satellite identification frequency into an aural acquisition-aid signal to the baseband equipment. The audio amplifier is comprised of resistors R1 thruogh R4, capacitors C1 and C2, and operational amplifier AR1. The input signal is coupled through capacitor C1 and resistor R1 to pin 2 of operational amplifier AR1. The output at pin 10 of amplifier AR1 is developed across load resistor R3 and is applied as feedback through capacitor C2 and resistor R2 to pin 2 of amplifier AR1. This feedback, together with resistor R1 and capacitor C1, establishes the frequency response of amplifier AR1. The response of amplifier AR1 is maximum at 1 kHz. The output of amplifier AR1 is applied through dropping resistor R4 to jack pin J1-9.

q. The afc and sweep amplifier circuit A34 (fig. 3-55) controls the frequency of the 48.6 MHz vco in the beacon demod. The afc function is performed during the phase lock condition, and the sweep function is performed during the signal absent condition. The circuit consists of four dc operational amplifiers (AR1 through AR4) and their associated circuit components as discussed in (1) through (7) below:

(1) During a phase lock condition, the discriminator output is applied through resistor R1 to the inverting input (pin 2) of operational amplifier AR1. The noninverting input (pin 3) of amplifier AR1 is referenced to ground through resistor R2. Resistors R7, R8, R9, and R4 and capacitor C1 form a feedback network which controls the gain of amplifier AR1. Relay K1 selects two different amounts of feedback. When relay K1 is deenergized, the feedback is applied through relay contacts 5 and 4 and the feedback network comprised of resistor R4 and capacitor C1 to the inverting input of amplifier AR1. When relay K1 is energized, resistor R7 is placed in parallel with resistor R8 and the feedback voltage is taken from the junction of resistors R8 and R9.

(2) The output of amplifier AR1 is applied through a frequency compensation network comprised of capacitor C2 and resistors R14 and R15 to the inverting input (pin 2) of operational amplifier AR2. Noninverting input (pin 3) of amplifier AR2 is referenced to ground through resistor R16. Capacitor C3 is the integrating capacitor connected across amplifier AR2. The output reference level is supplied by a voltage divider comprised of resistors R20 and R31 and potentiometer R30 which is connected between –28 vdc and ground. The output of amplifier AR2 is applied through resistor R37 to jack pin J2-3 to provide a tuning indication. The output is also applied through resistor R11, contacts 1 and 2 of deenergized relay K1, and resistor R27 to the noninverting input (pin 3) of amplifier AR3. Inverting input (pin 2) is provided with a temperature compensation input that is applied through jack pin J2-8 and resistor R28 to amplifier pin 2. The reference input at jack pin J2-8 is filtered by capacitor C7.

(3) The output of amplifier AR3 is applied as feedback through resistor R24 and R36 and capacitor C8 to pin 2. Resistor R29 is the output load resistor. The output of amplifier AR3 is applied to jack pin J2-1 as the vco control voltage. When the vco is controlled manually, resistor R27 is connected to ground through jack pin J2-5. Resistors R32 and R33 form a voltage divider connected between +28 vdc and ground. The voltage divider supplies a positive voltage to the externally located manual potentiometer. Resistors R34 and R35 form a voltage divider connected between –28 vdc and ground. This voltage divider supplies a negative voltage to the externally located manual potentiometer. The fine and course manual control inputs at jack pins J1-6 and J1-7 are filtered by capacitors C5 and C6, respectively, and are applied through resistors R25 and R26 to pin 3 of amplifier AR3. The output of operational amplifier AR4 is inhibited by a ground applied through jack pin J1-2 to diode CR7 and resistor R5.

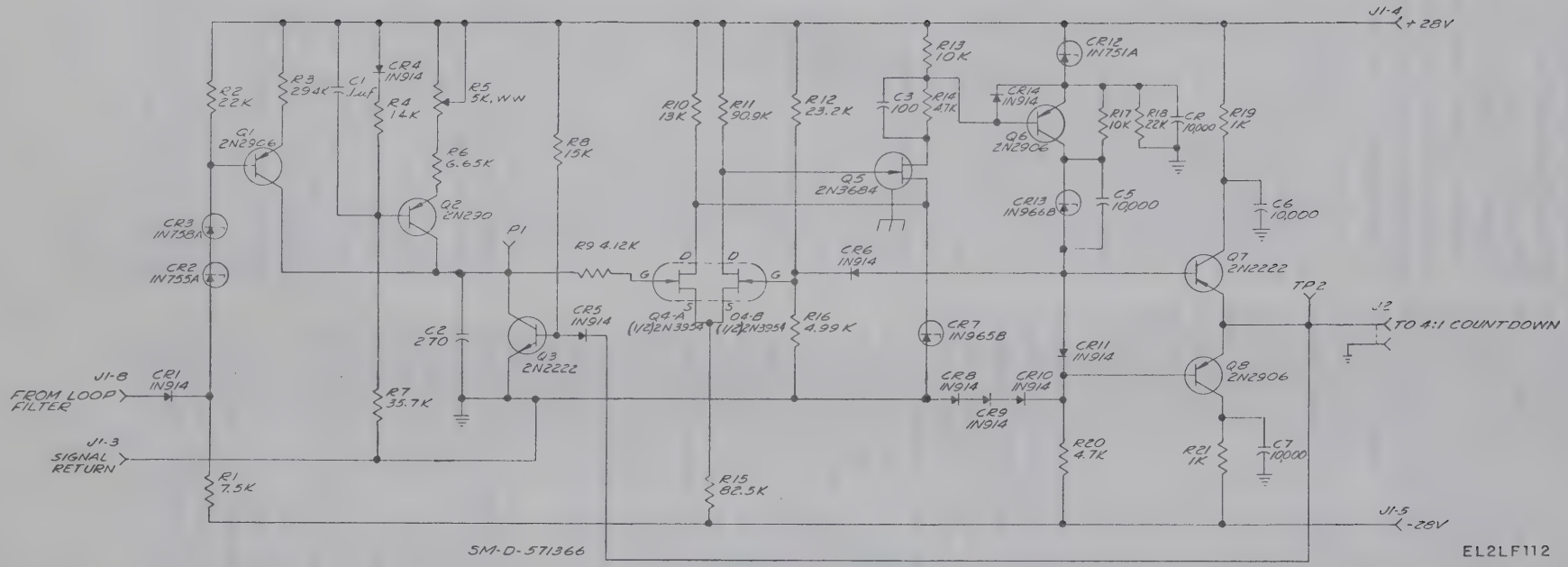


Figure 3-53. 480 kHz vco 1A3A4A31, schematic diagram.

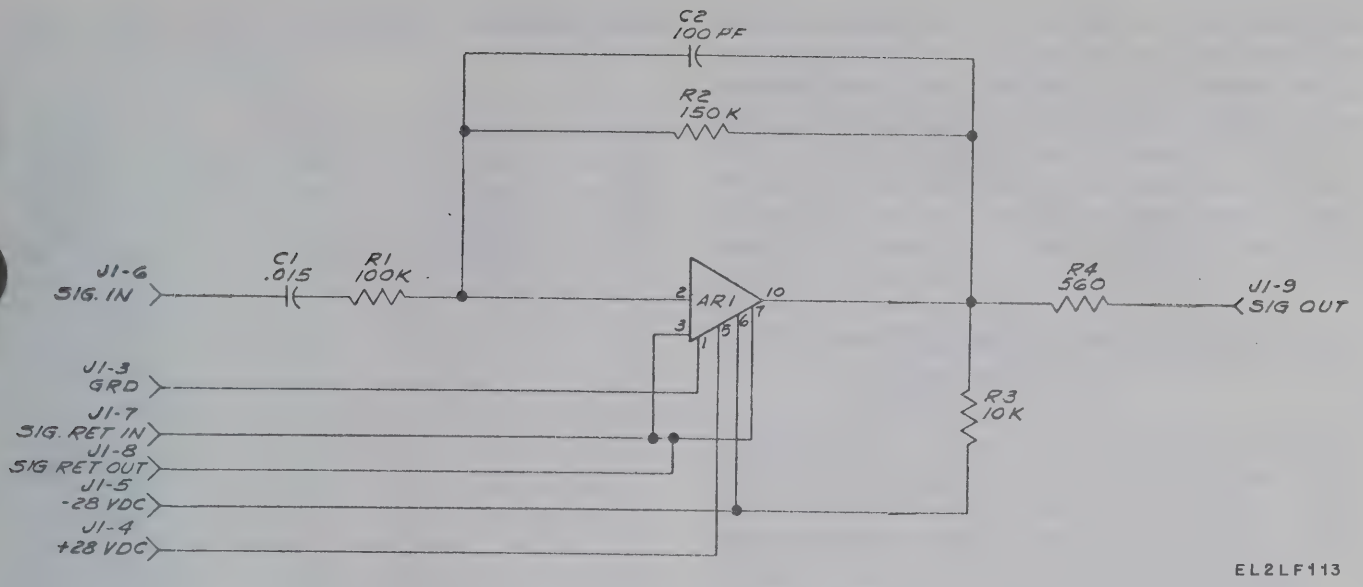


Figure 3-54. Audio amplifier 1A3A4A32, schematic diagram.

(4) During a signal absent condition, the ground is removed from diode CR7 and the output of amplifier AR4 is applied through jack pin J1-1, a set of contacts of the sweep stop relay, and jack pin J1-2 to diode CR7. The signal at the wiper arm of potentiometer R30 is applied through resistor R23 and capacitor C4 to noninverting input (pin 3) of amplifier AR4. This input is clipped at the forward resistance voltage drop across diodes CR8 and CR9. Inverting input (pin 2) is referenced to ground through resistor R22. Resistor R19 is the output load resistor. A negative input to amplifier AR4 causes the output at pin 10 to go negative. This negative voltage forward biases diode CR4. The negative voltage is limited to −12 vdc by quad diode CR3 and breakdown diode CR5. From diode CR4, the negative voltage is applied through jack pin J1-1, an external set of relay contacts, and jack pin J1-2 to diode CR7 and resistor R5. The negative voltage forward biases diodes CR6 and CR2 and reverse biases diode CR7. This voltage is developed across resistor R6 to establish the negative voltage level.

(5) The negative voltage level is applied through diode CR6 and resistor R17 to inverting input (pin 2) of amplifier AR2. This causes the output of amplifier AR2 to go positive, and integrating capacitor C3 starts charging. The action produces a positive-going ramp voltage that is applied from the wiper arm of potentiometer R30 to pin 3 of amplifier AR4 causing the output of AR4 to go positive. This positive voltage reverse biases diode CR4. The positive voltage is applied through resistor R10, clipped to +12 vdc by quad diode CR3 and breakdown diode CR5, and is applied through the external relay to diode CR7 and resistor R5. This positive voltage reverse biases diodes CR2 and CR6. The positive voltage is passed by diode CR7 and is applied through resistor R18 to inverting input (pin 2) of amplifier AR2. The output of amplifier AR2 swings negative and starts discharging integrating capacitor C3.

(6) The output polarity reversal terminates the positive-going ramp and starts producing a negative-going voltage which is applied from the wiper arm of potentiometer R30 to noninverting (pin 3) of amplifier AR4. The output of amplifier AR4 now goes negative, is clipped, and is gated through diode CR6 to the inverting input (pin 2) of amplifier AR2. The negative-going output of amplifier AR2 reverses and causes capacitor C3 to start charging. This action initiates the positive-going ramp voltage at the output of AR2. Recurring oscillations thus produce the sawtooth waveform at the output of AR2 until a ground is applied to jack pin J1-2. Each positive-going portion of the sawtooth waveform has a duration of 0.86 seconds and each negative-going portion has a duration of 0.14 seconds.

(7) The difference in duration is produced by the difference in amplitude between the positive and negative square waves applied to amplifier AR2. The output of amplifier AR2 is applied through resistor R11, relay K1, and resistor R27 to noninverting input (pin 3) of amplifier AR3. The sawtooth output of amplifier AR3 is applied to jack pin J2-1 and is used to sweep a vco. The amplitude of the sawtooth, and therefore the sweep width, is reduced by energizing relay K1. This places resistor R12 in series with resistor R11.

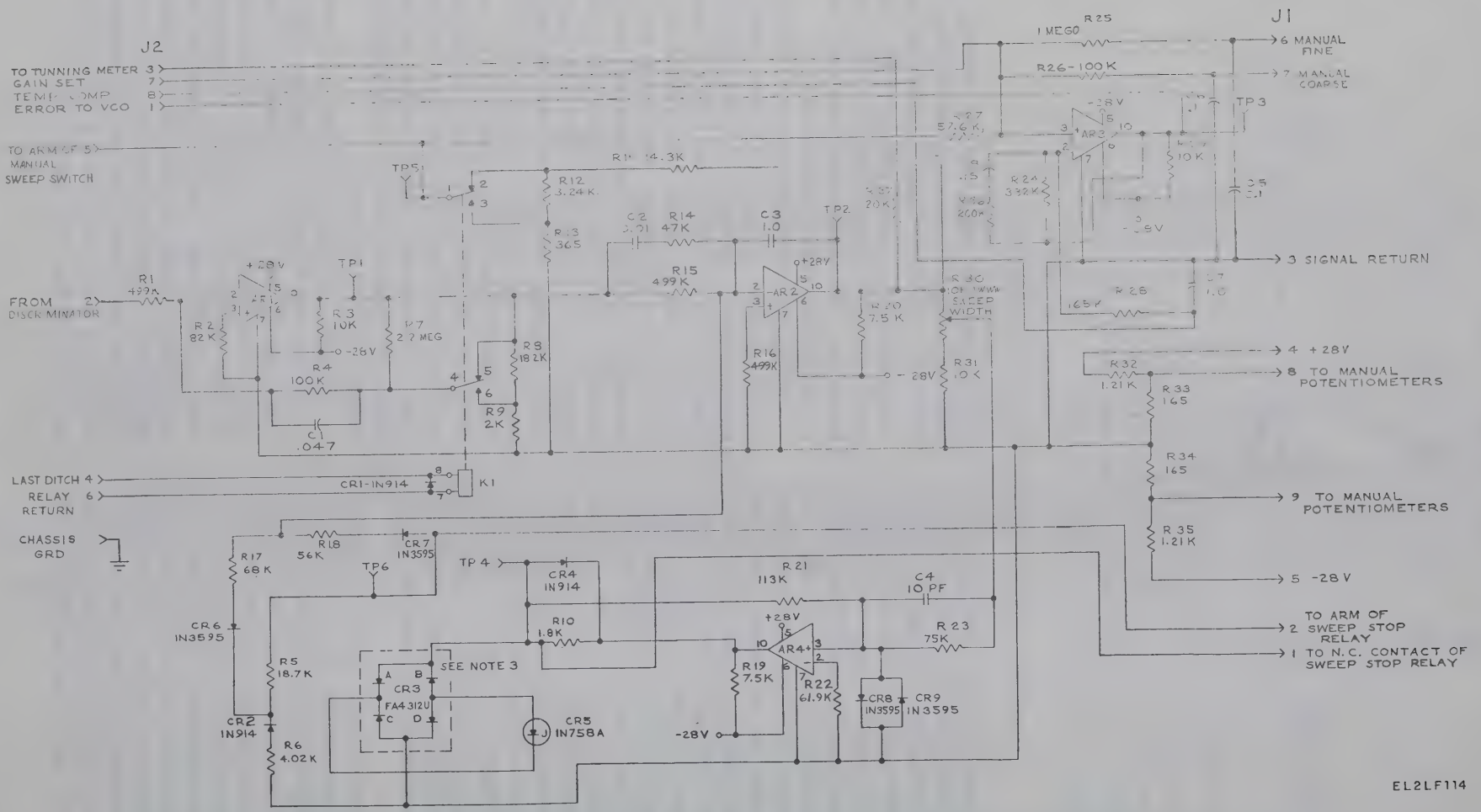


Figure 3-55. Afc and sweep amplifier circuit 1A3A4A34, schematic diagram.

3-17. Test Translator Control 1A2A26, Circuit Analysis

(fig. FO 3-30)

a. The test translator control panel provides the operator with the means of loop testing the receiver circuits. The panel controls application of a simulated receive signal at various points in the receive signal path. Unregulated +28 vdc, applied to the panel at J1-AA, is routed to switch/indicator A1 through A4 and switch S2 through S8. An external control relay for the test translator oscillator is energized when INJECTION SIGNAL-ON/OFF switch/indicator A4 is in the ON position, routing +28 vdc to J1-FF. Note that the opposite (lower) set of contracts of A4 routes +28 vdc to J1-R in the OFF position. J1-4 ties to a waveguide switch which, when activated, terminates the transmit signal. When A4 is ON, contacts C2 and NO2 are closed, applying the +28 vdc to the indicator portions of A4.

b. ATTENUATION switch S3, through S7, controls the application of fixed attenuators in the patch of the test translator oscillator signal. This feature allows manually controlled variations in the test signal power level in 1 db steps over a 31 db range for loop testing under simulated weak, intermediate and optimum signal conditions. Any combination of switches may be utilized to obtain the desired attenuation. A closed switch routes +28 vdc to coaxial switches which connect the appropriate attenuator in the signal path.

c. INJECTION point switch S2 determines the point along the signal path that the test translator signal is inserted. The position of S2 routes +28 vdc to the appropriate pin on a coaxial switch which connects the test signal at its input port to the proper output port. MIXER CURRENT meter M1 is used to selectively monitor the forward or reverse current of the waveguide crystal mixer. This is accomplished by setting selector switch S1 to the appropriate position (FWD or RVS). TEST TRANSLATOR/PILOT GENERATOR switch S8 is not used at this time.

d. Two-segment, back-lighted switch/indicators A1, A2, and A3 control the status of waveguide switches to select which combination of parametric amplifier (LNA1 or LNA2) and TWT (TWT 1 or TWT 2) will be on-line. In addition to selecting the on-line components, the switch/indicators connect the off-line parametric amplifier and TWT into the GAIN MONITOR circuit so that the off-line components may be checked by injecting the test translator signal to the off-line components and monitoring GAIN MONITOR meter M2 on the control panel. Since there are four possible combinations of off-line components, each combination has an individual meter calibration resistor. All three switch/indicators are identical. The top set of contacts applies control voltage to the appropriate waveguide switch. A return path through the waveguide switch causes one of the segment lamps to light indicating the switch position selected. The detected test translator signal, applied at J1-A, is routed through the lower set of contacts of switch/indicator. The lower set of contacts routes the detected test translator signal to the appropriate meter calibration resistor to the meter.

3-18. Comm Demod Power Supplies 1A3A9 Circuit Analysis

(fig. FO 3-31)

This assembly consists of eight power supply modules and associated circuit breakers. These modules supply the regulated voltages for the comm demod circuits. A 115 vac single-phase input signal is applied through jack J1, terminals 1 and 2 of terminal board TB1, and the respective circuit breakers CB1 through CB4 and CB5 through CB8 to the input transformers of the power supplies. Input/output signal characteristics for power supplies PS1 through PS8 are shown in figure 3-22.

3-19. Beacon Demod and Baseband Power Supplies 1A3A10

(fig. FO 3-32)

This assembly consists of nine power supply modules and associated circuit breakers. These modules supply regulated voltages for the beacon demod circuits. A 115 vac single-phase input signal is applied through jack J2, terminals 1 and 2 of terminal board TB1, and the respective circuit breakers CB2 through CB4 and CB5 through CB7, to the input transformers of the power supplies. Input/output signal characteristics for power supplies PS1 through PS9 are shown in figure 3-8.

3-20. Teletypewriter Patch Panel 1A3A25, Circuit Analysis

(fig. FO 3-33)

a. The teletypewriter patch panel provides access to teletypewriter loops and allows cross patching when other than normal system routing is required. The patch cord jacks are arranged in LINE, EQUIP, MON and MISC designated horizontal rows and are numbered J1A through J26A, J1B through J26B, J27 through J52 and J53 through J77 and S1, respectively.

b. Each EQUIP and LINE jack provides a normal-through connection so that when a patch cord is inserted, the normal-through connection is broken and the signal input is available for patching to other circuits. LINE and EQUIP jacks not used in the normal-through circuits provide for patch cord access to their associated lines or equipments. Each MON jack is a monitoring point for the circuit jack immediately above it. It pro-

vides a convenient point for patching the monitor equipment into the signal circuits without interrupting normal operation. The MISC jacks provide access points for associated test equipment and test signals.

c. Line isolator unit 1A3A26 (fig. FO 2-8, sheet 2) provides +6 vdc from J3-N and −6 vdc from J3-J to teletypewriter patch panel 1A3A25 terminals J107-P and J107E, respectively. The desired voltage level is selected by switch S1 to provide either a steady mark or a steady space test signal which is patched to the circuit under test from +6V OUTPUT jack J77. Edge voltmeter M2 (fig. FO 2-1, sheet 2) is connected to ±6V METER jack J76 (fig. FO 2-1, sheet 3) which is patched to the monitor jack of the TTY channel of interest.

3-21. Baseband Patch Panel 1A3A12, Circuit Analysis

(fig. 3-56)

a. The baseband patch panel provides access to the various teletypewriter, voice and wideband loops. Provisions are made to allow cross patching when other than normal system routing is required.

b. The patch cord jacks on the baseband patch panel are arranged in LINE, EQUIP and MON designated rows and generally have similar functions. Each EQUIP and LINE jack provides a normal-through connection so that when a patch cord is inserted, the normal-through connection is broken and the audio or signal input is available for patching to other circuits. LINE and EQUIP jacks that are not used in the normal-through provide for patch cord access to their associated lines or equipment. Each MON jack is a monitoring point for the circuit jack immediately above it. It provides a convenient point for patching the monitoring equipment into the signal circuits without interrupting normal operation. Unmarked jacks are spares that are used for expansion of equipment facilities.

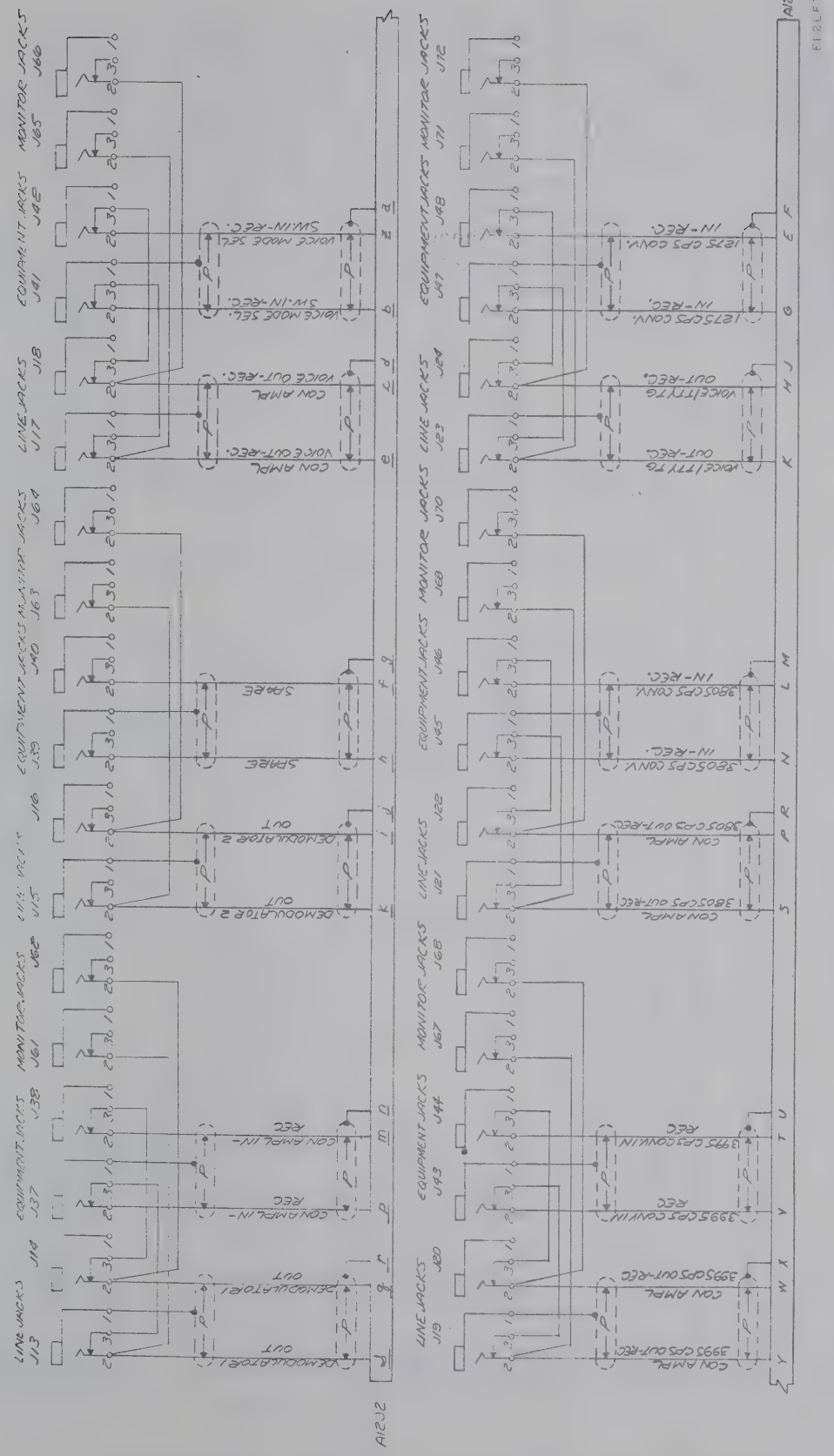


Figure 3-56. ① *Baseband patch panel 1A3A12, wiring diagram (sheet 1 of 9).*

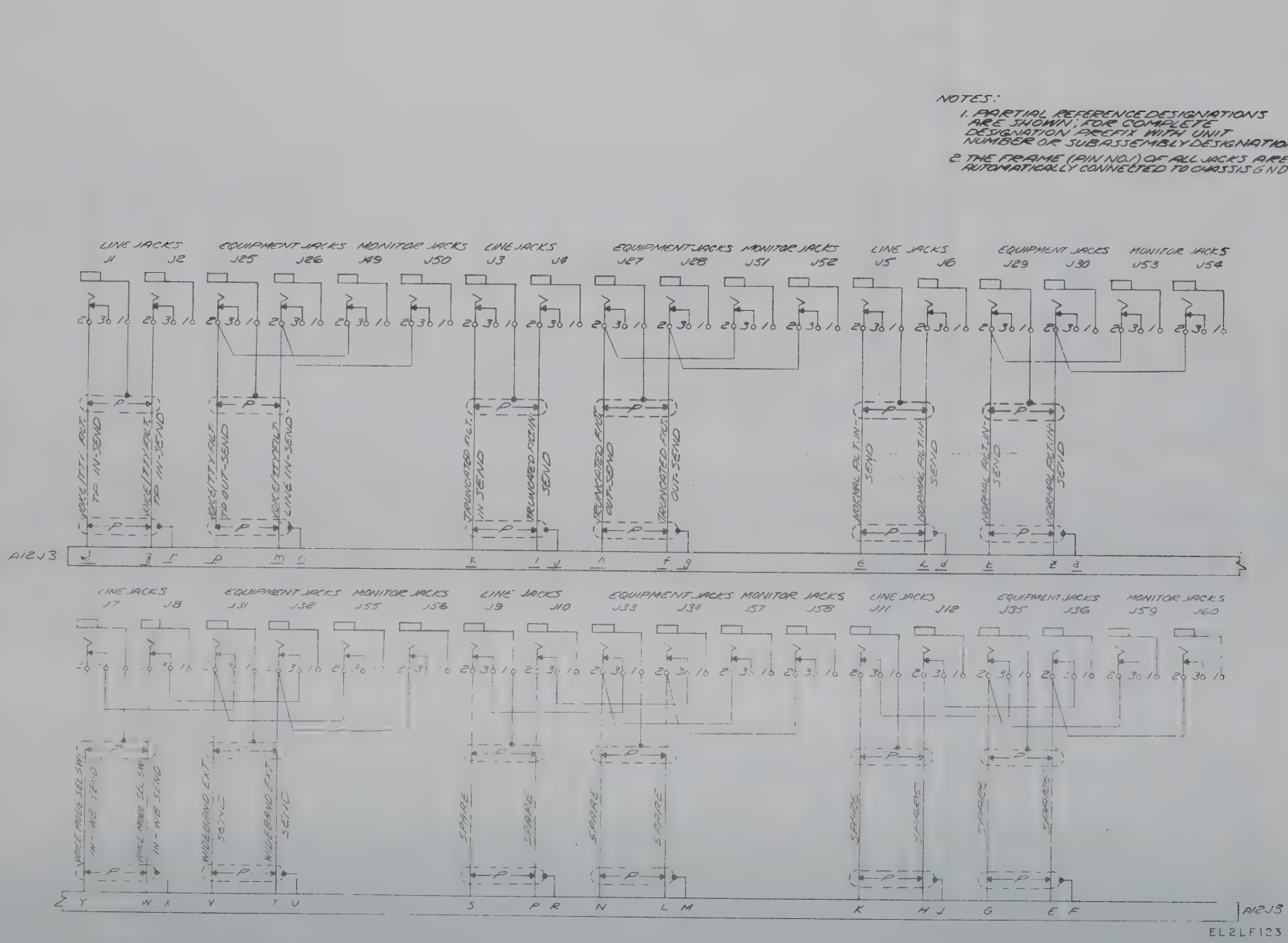


Figure 3-56. (2) Baseband patch panel 1A3A12, wiring diagram (sheet 2 of 9).

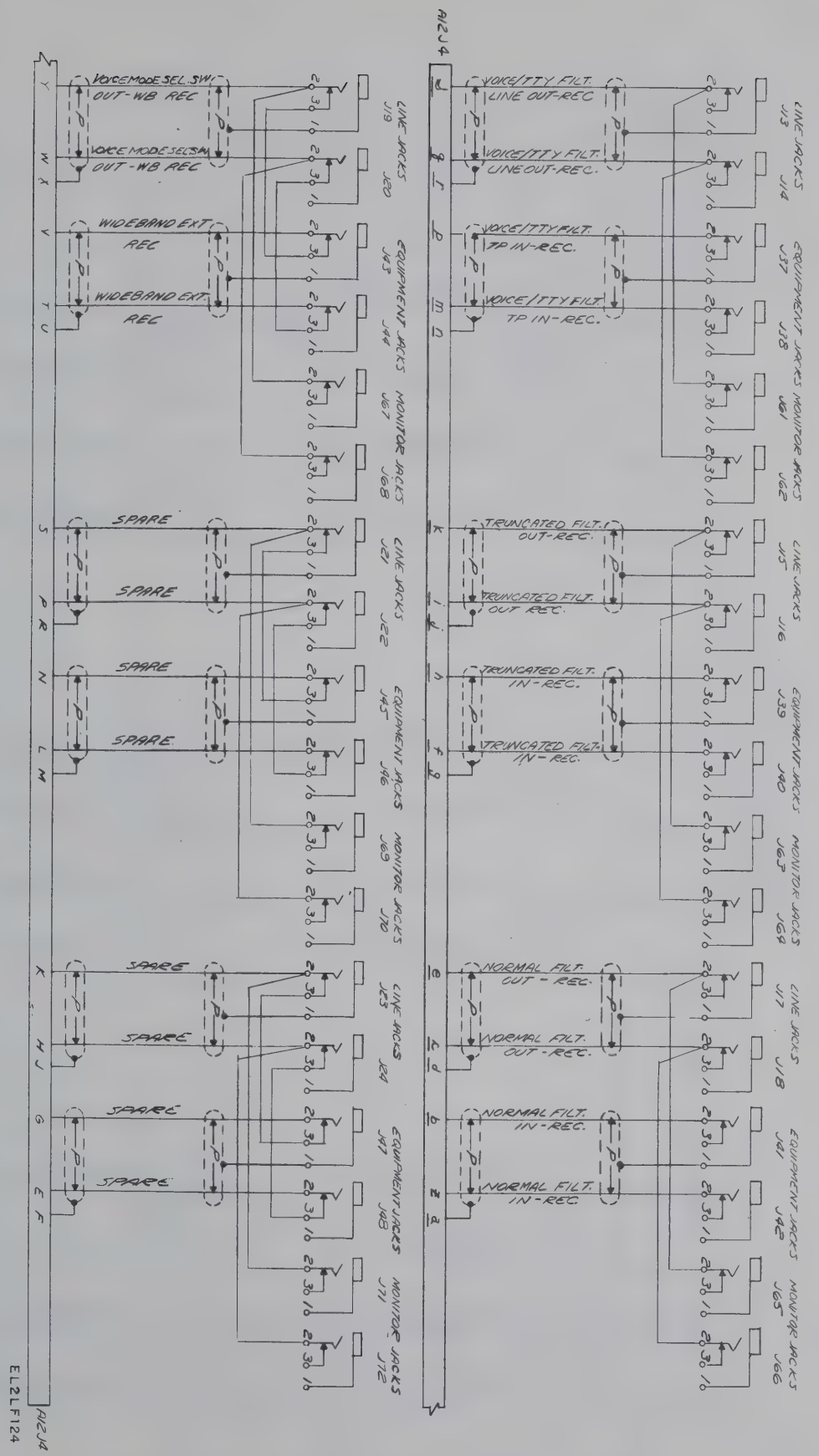


Figure 3-56.③ Baseband patch panel 1A3A12, wiring diagram (sheet 3 of 9).

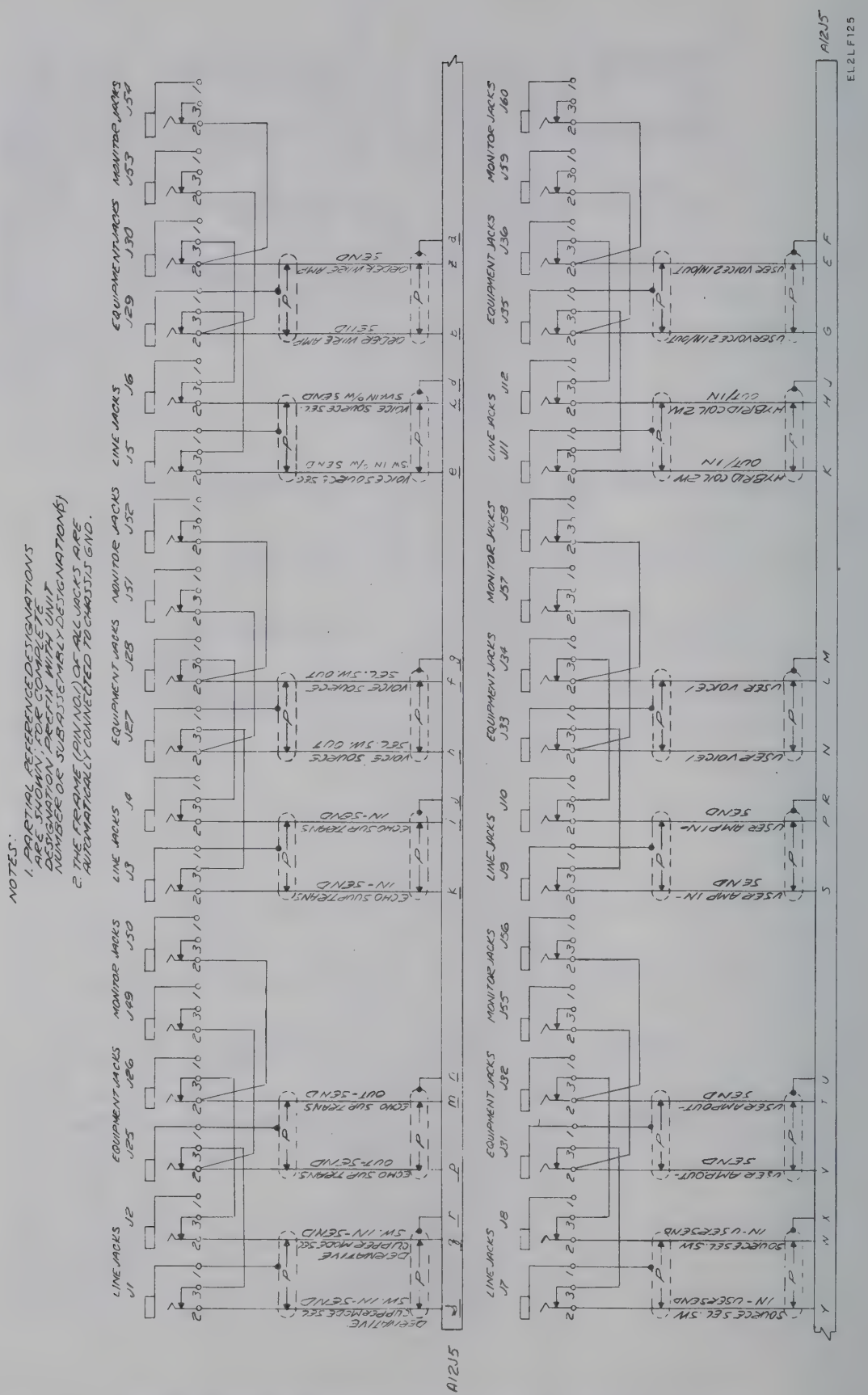


Figure 3-56.④ Baseband patch panel 1A3A12, wiring diagram (sheet 4 of 9).

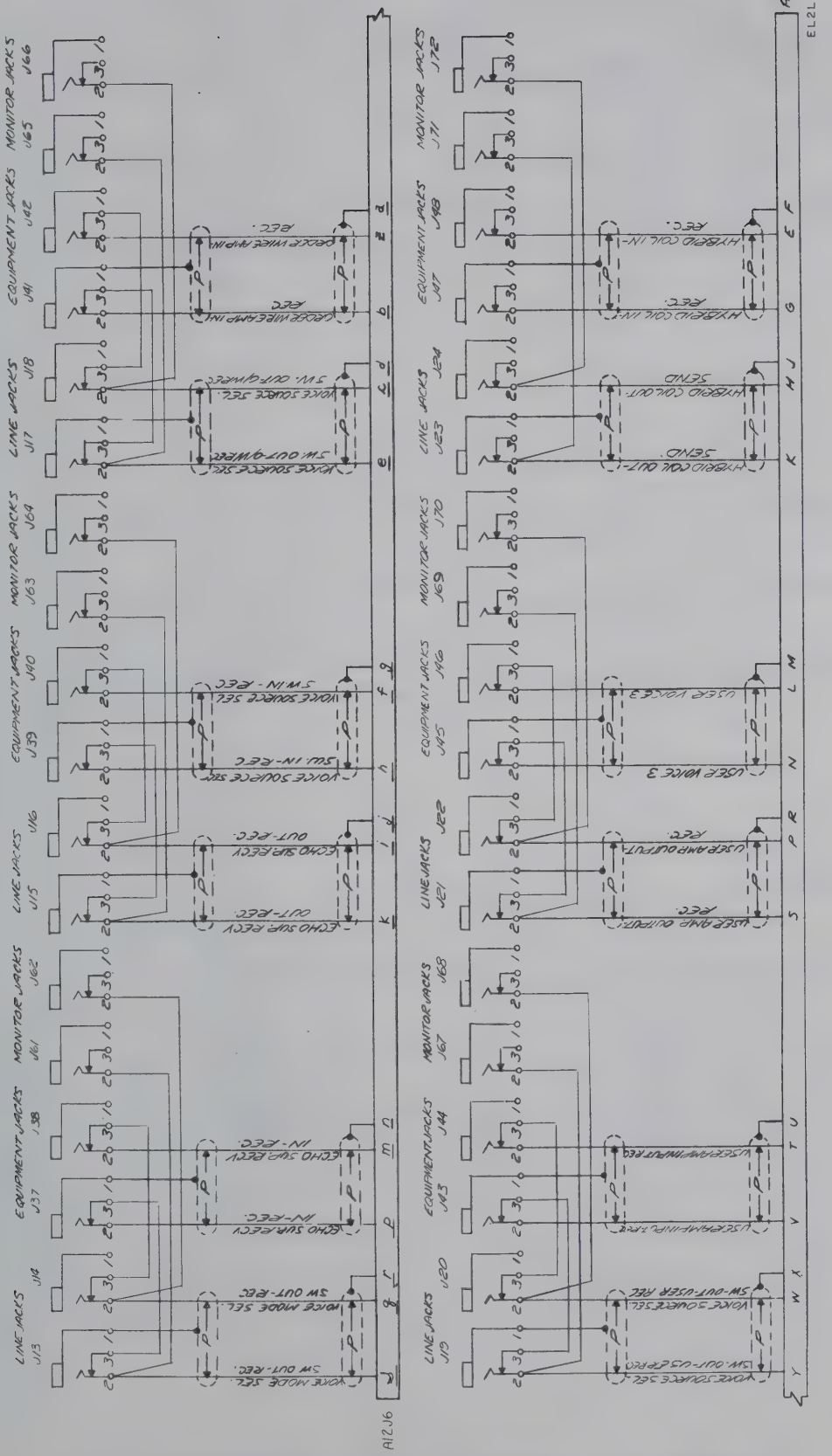


Figure 3-56.⑤ Baseband patch panel 1A3A12, wiring diagram (sheet 5 of 9).

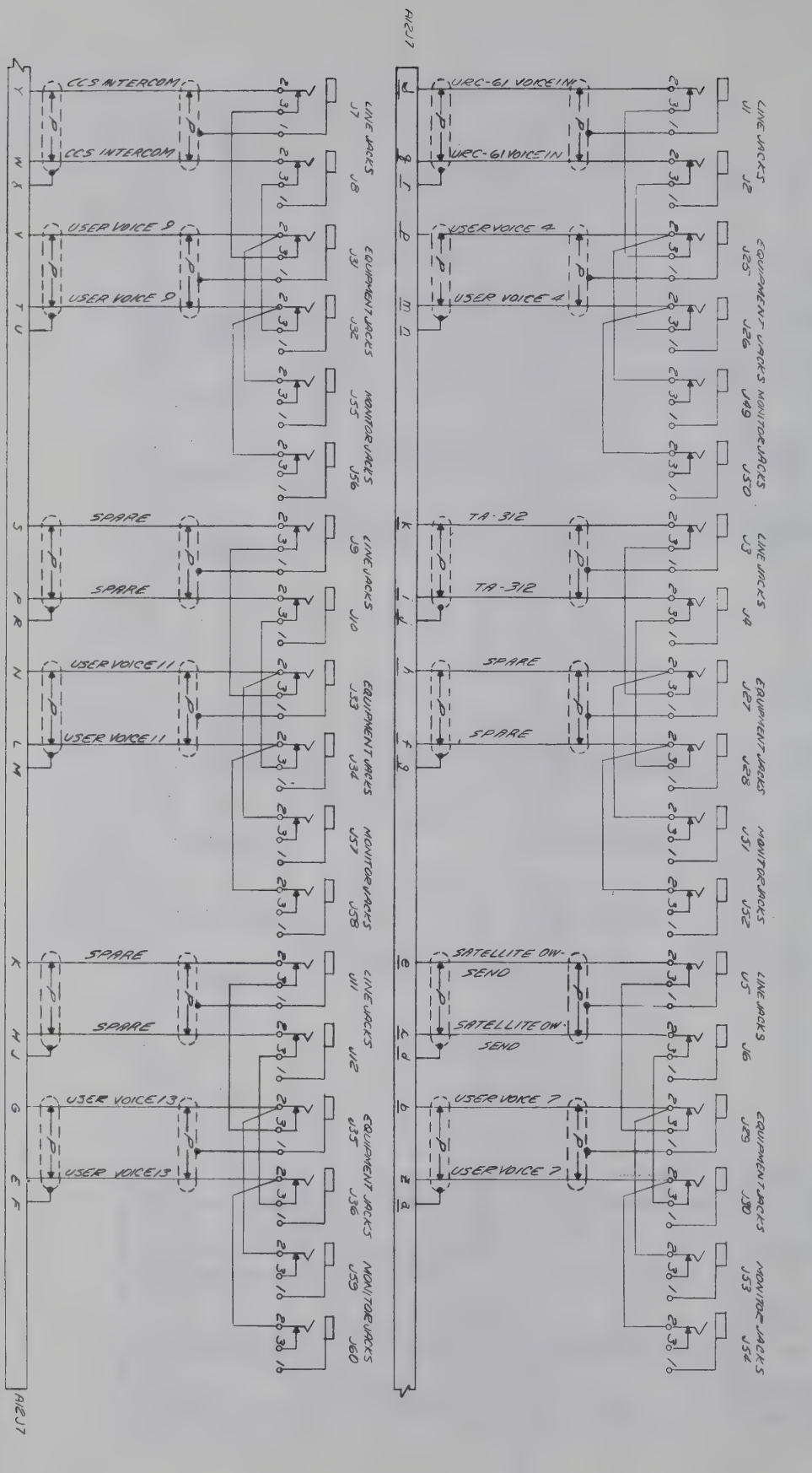


Figure 3-56.⑥ Baseband Patch panel 1A3A12, wiring diagram (sheet 6 of 9).

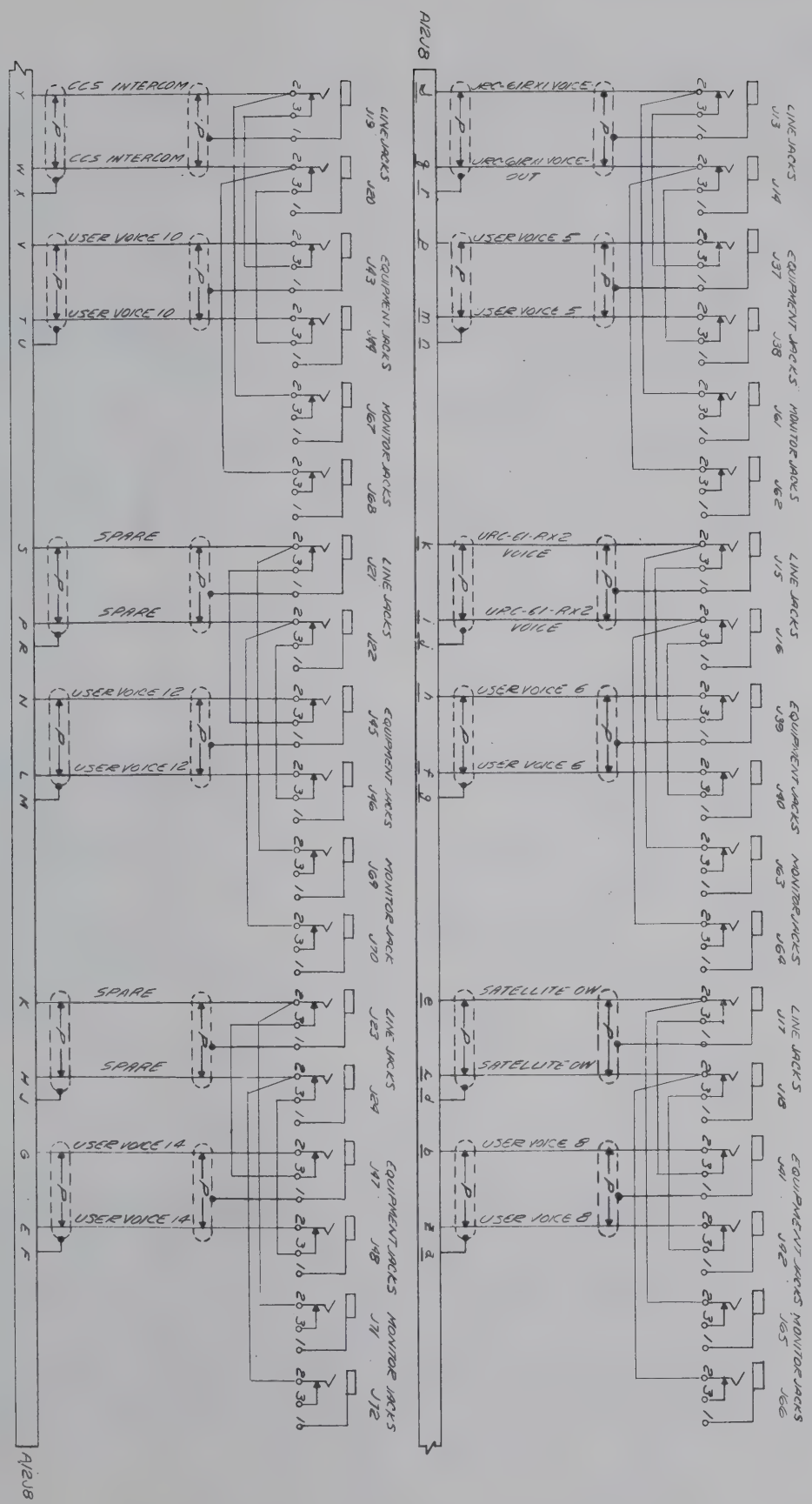


Figure 3-56.⑦ Baseband patch panel 1A3A12, wiring diagram (sheet 7 of 9).

NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
2. THE FRAME (PIN NO.1) OF ALL JACKS ARE AUTOMATICALLY CONNECTED TO CHASSIS GND.

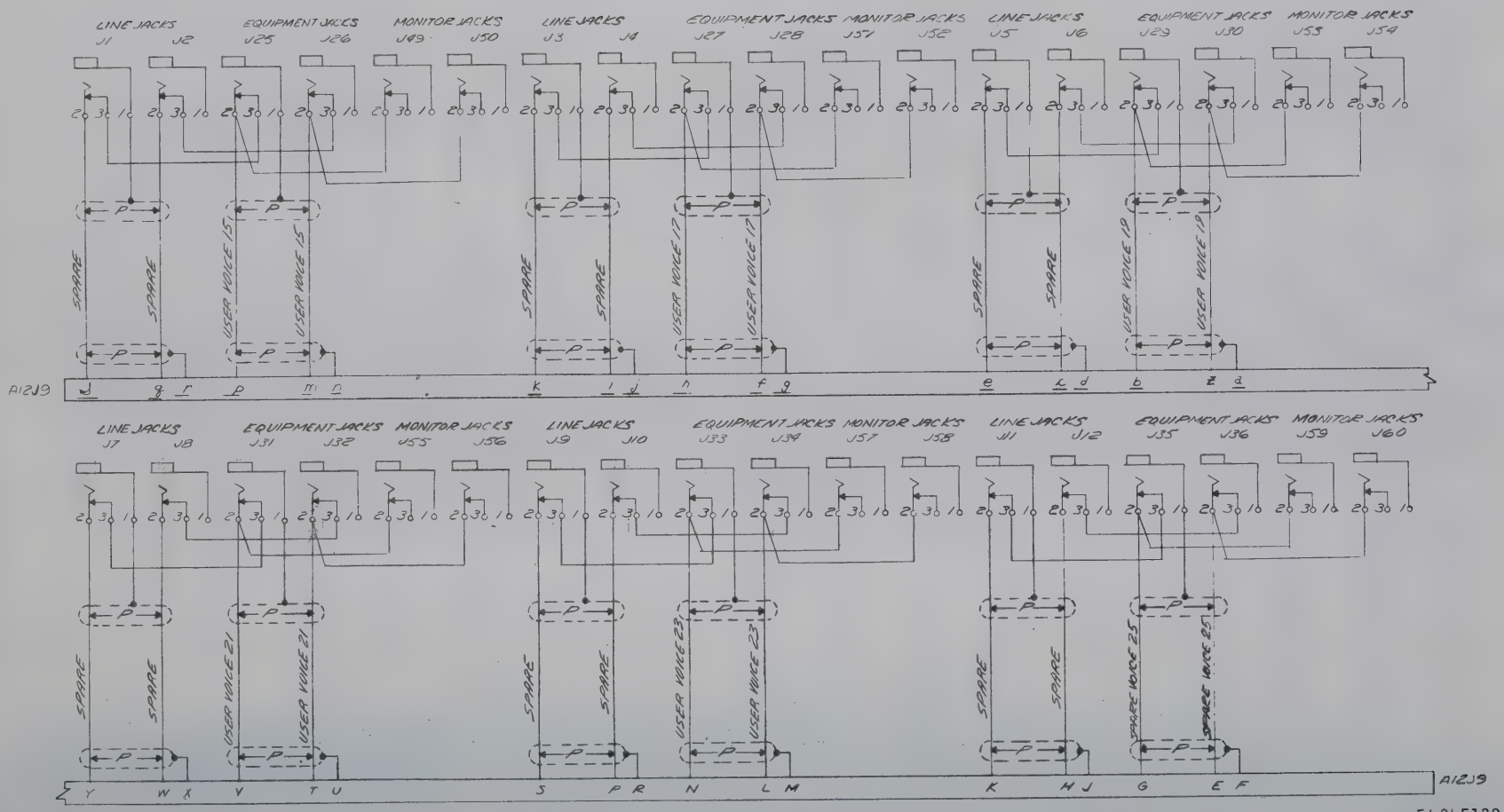


Figure 3-56.⑧ Baseband patch panel 1A3A12, wiring diagram (sheet 8 of 9).

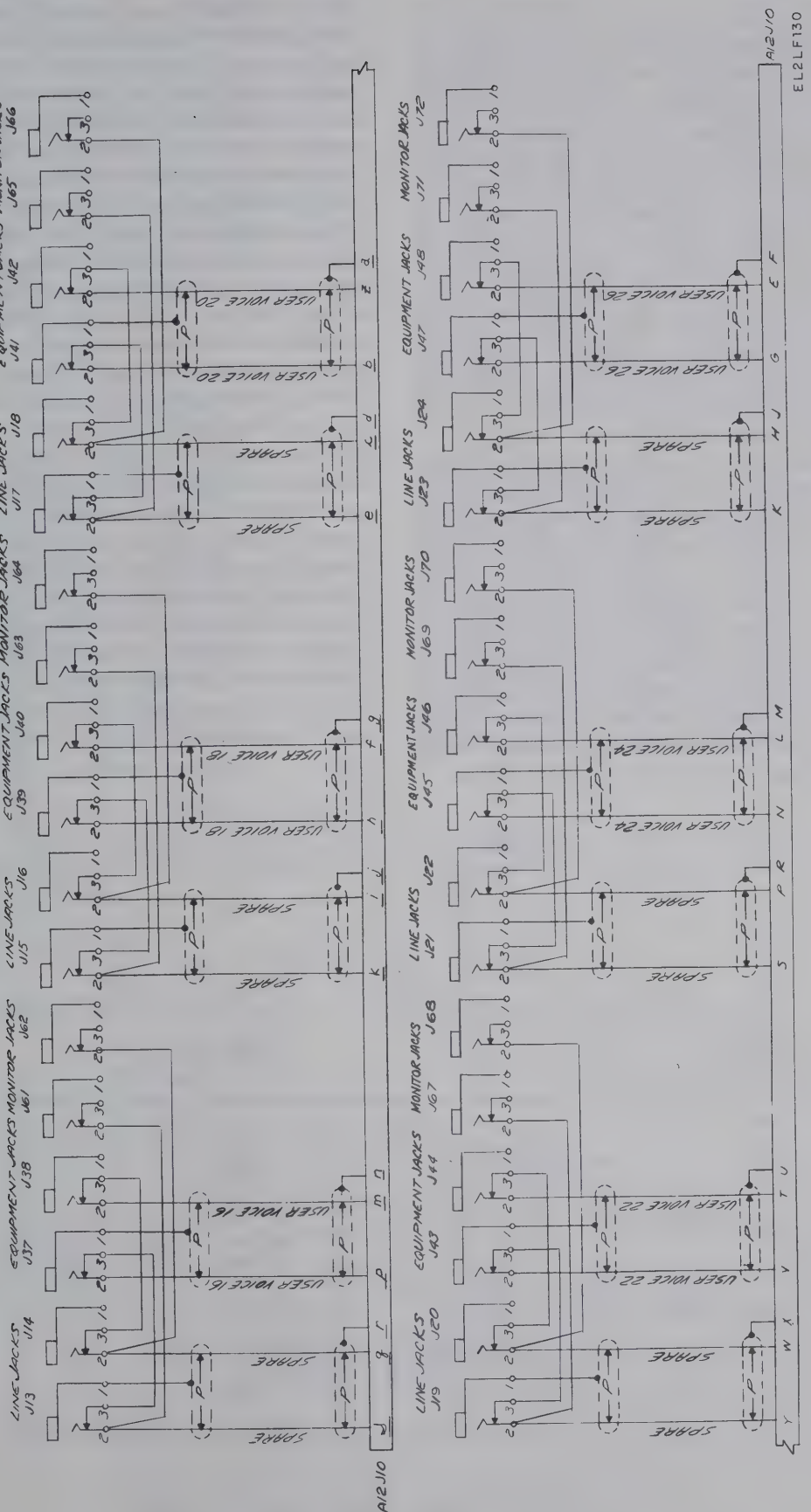


Figure 3-56.⑨ Baseband patch panel 1A3A12, wiring diagram (sheet 9 of 9).

3-22. Baseband Control Panel 1A3A13, Circuit Analysis.

(fig. 3-57 through 3-61 and FO 3-34)

Baseband control panel 1A3A13 selects and processes voice, teletypewriter, and wideband signals in the transmit and receive circuits of the AN/TSC-54. Filters, isolation transformers, clipper amplifiers, baseband operational amplifiers, and power amplifiers are used to process the various types of intelligence. Selection and filtering of the transmit and receive circuits is accomplished by means of manual switching. The major components which form part of the baseband control panel are discussed in *a* through *e* below. The individual functional configurations and their relationship to the overall transmit and receive functions are shown in the transmit and receive functional diagrams, respectively.

a. The baseband power amplifier of the transmit baseband functions as a derivative clipper circuit during degraded signal conditions. The basic circuit is shown on figure 3-57 and consists of a common emitter class A transistor amplifier-driver stage and a complementary-connected npn and pnp transistor output stage. The complementary output stage provides a push-pull output to drive a 70-ohm and a 300-ohm output circuit. The input signal is applied through resistor R9 and coupling capacitor C6 to the base of the driver stage, transistor Q3. Resistor R11 in the emitter circuit of transistor Q3 performs a swamping function and is signal bypassed by capacitor C6. Since transistor Q3 is operated class A, conduction occurs (during no signal condition) through diodes CR1 and CR2 and resistor R2, which establishes a slight forward bias on the bases of transistors Q2 and Q1. This avoids distortion in the push-pull output due to current crossover point of the two transistors. The collectors of transistors Q2 and Q3 are effectively at ac ground potential through capacitors C1 and C7, respectively. During the negative excursion of the input signal, transistor Q3 conducts less heavily causing a positive-going potential at the bases of transistors Q2 and Q1. This action forward biases npn transistor Q1 and reverse biases pnp transistor Q2. The positive-going signal is passed through transistor Q1 and across emitter resistor R4 to the output load. During the positive excursion of the input signal, transistor Q3 conducts more heavily causing a negative-going potential at the bases of transistor Q2 and Q1. This action reverse biases transistor Q1 and forward biases transistor Q2. The negative signal is passed through transistor Q2 and across emitter resistor R6 to the output load. This resultant push-pull output is applied across the primary of the line transformer. In addition to the outputs used for the 70-ohm and the 300-ohm loads, an output is made available for driving a volume unit (VU) meter.

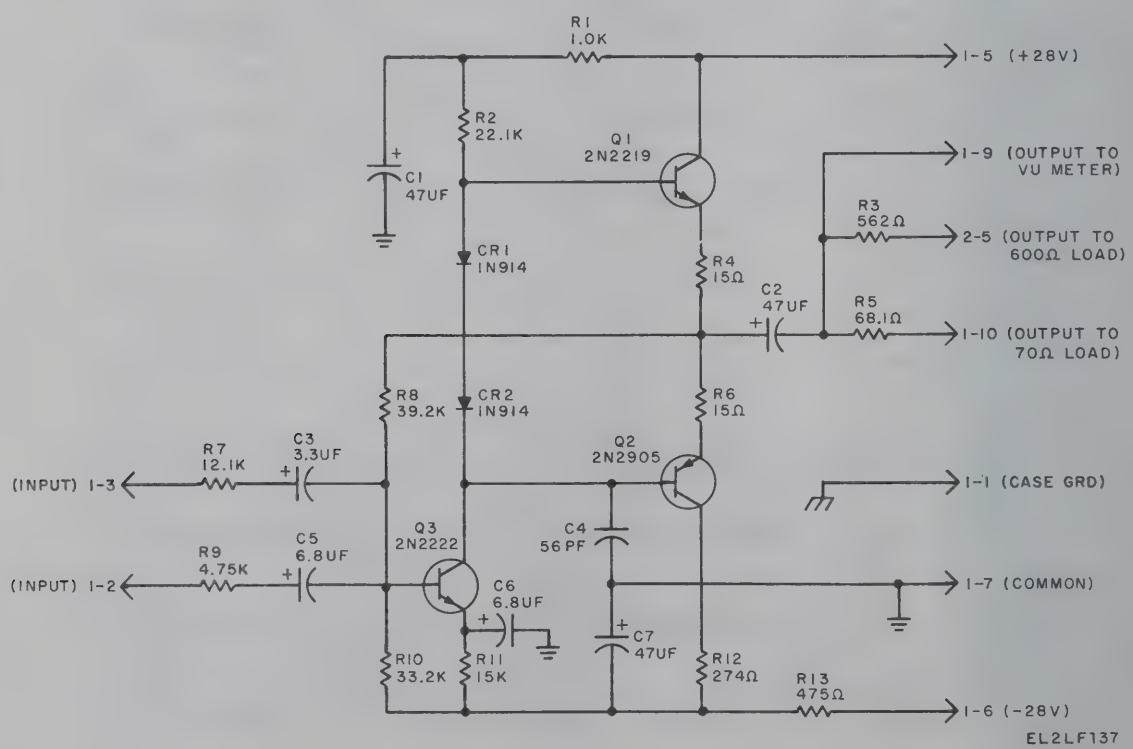


Figure 3-57. Baseband power amplifier, schematic diagram.

b. Baseband operational amplifier A3, A7, and A8 is used in a number of different applications to provide such functions as inverted and non-inverted amplification, integration and differentiation, differentiation and summing, and clipping amplification. In this application it is used as an inverting amplifier to provide the input drive to the power amplifier. The supplementary components used in this application are shown on figure 3-58. In association with the other amplifiers of the derivative clipper circuit, the baseband operational amplifier functions to shape the audio response for maximum power density under degraded signal conditions.

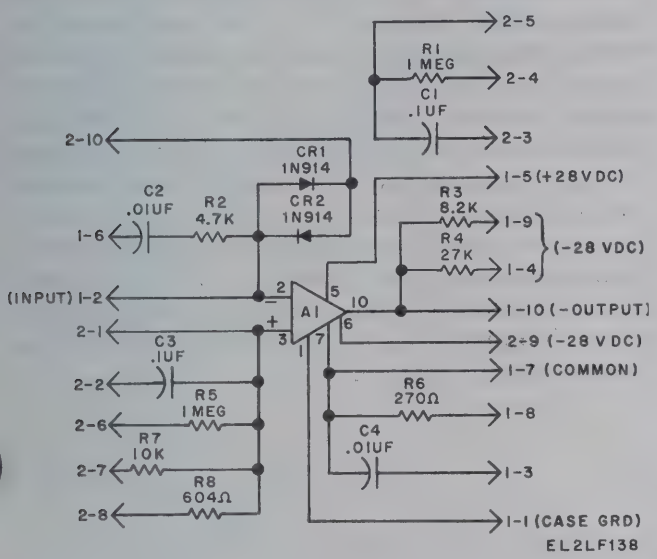


Figure 3-58. Baseband operational amplifier, schematic diagram.

c. The baseband tone filter is used on conjunction with a baseband operational amplifier similar to that discussed in *b* above, to provide a reduced level of noise-free 1 kHz test tone for injection into the baseband receive circuits. The circuit of the baseband tone filter is shown on figure 3-59 and consists of a pnp and npn transistor and a 1 kHz band suppression filter. The circuit is connected across the operational amplifier and insures that the 3 dB bandwidth of the 1 kHz signal is between 40 Hz and 65 Hz. The tone input signal is applied through pin 2-2 and resistor R9 to the inverting input of the associated 1 kHz keying amplifier whose output is fed back through pin 1-10 to band suppression filter N1. Undesired frequencies are filtered out and the desired bandwidth signal is applied to the base of transistor Q2. Transistor Q1 functions to clamp the feedback signal to the desired level of input to the keying amplifier. Resistor R5 establishes the bias for transistor Q1 which has its emitter clamped by Zener diode CR1 to 7.5 vdc. The output of the tone filter is developed across resistor R4 which is the emitter resistor for transistor Q2 and collector resistor for transistor Q1. The output is fed through resistor R7 and common connections pins 1-4 and 1-2 to the inverting input of the associated amplifier. Resistor R2 provides an offset voltage across the terminals of the associated amplifier.

d. Input/output signal characteristics for the 1 kHz band suppression filter are shown in figure 3-60.

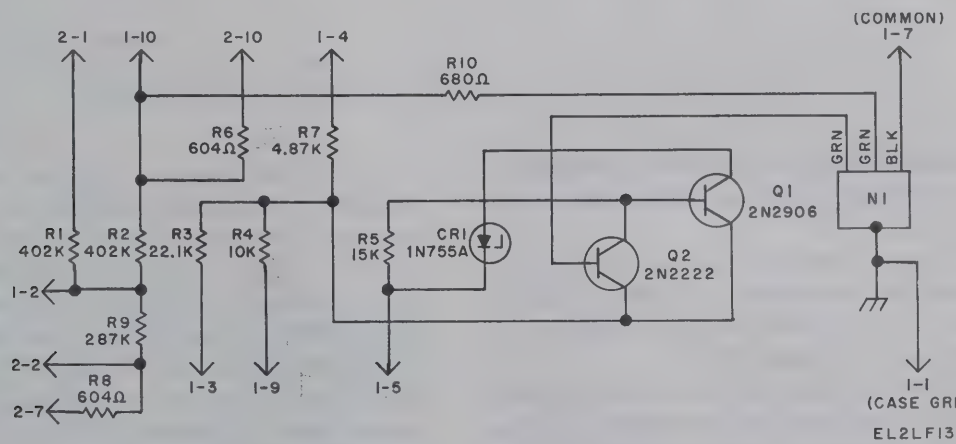


Figure 3-59. Baseband tone filter, schematic diagram.

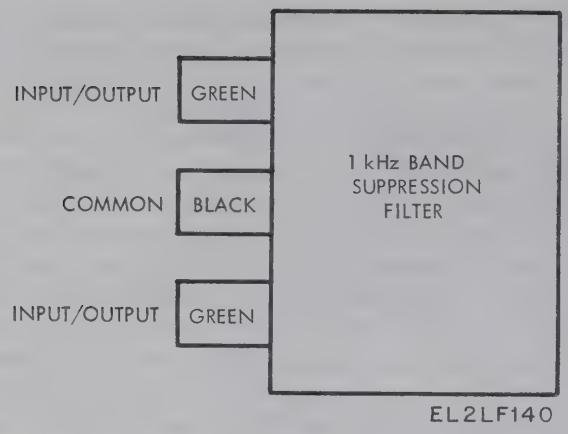


Figure 3-60. 1 kHz band suppression filter, schematic diagram.

e. The twin-tee network and level control is used in conjunction with the baseband derivative clipper circuit discussed above. In conjunction with the baseband operational amplifier, it functions to provide a 10 kHz oscillator for the derivative clipper circuit. It consists of an RC network arranged to divide a feedback path across the operational amplifier and includes a 10 kHz band suppression filter network. The circuit is shown on schematic diagram, figure 3-61. It provides negative feedback loops and reference level control for the associated amplifier. Its output can be manually controlled to regulate the drive to the derivative clipper amplifier as shown on the functional diagram (fig. FO 2-1, sheet 4). The network is effectively connected between the input and output of the baseband operational amplifier. It divides the feedback loop through connection pins 1-10 into two paths with one path being fed through resistors R5 and R4 and capacitor C1 to the INVERTING INPUT of the amplifier. The positive portion of this feedback signal is removed by diode CR1 so that a negative feedback reference is applied to the amplifier. The second path for the feedback loop is applied through the parallel combination of resistor R6 and capacitor C2 to the input of band suppression filter network N1. This portion of the feedback signal has its positive portion clipped by diode CR2. The output from the suppression filter is used as the reference to the NON-INVERTING INPUT of the amplifier. Resistors R2 and R3 are connected across the −28 vdc supply and provide a voltage divider network to establish an operating level reference. The resulting references at the inputs of the amplifier pulse it at a 10 kHz rate with the output being applied through resistor R1 and connection pin 1-4 to the clipper amplifier threshold level control.

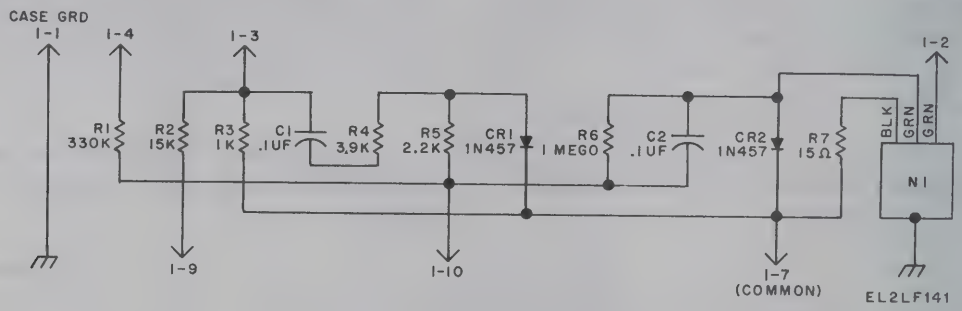


Figure 3-61. Twin-tee network and level control circuit, schematic diagram.

3-23. Modulator 1A3A14, Circuit Analysis.

(fig. 3-62 through 3-75 and FO 3-35 through FO 3-42)

The detailed circuit analysis for circuits within modulator 1A3A14 is covered in *a* through *r* below. The schematic diagram of the modulation amplifier is shown on figure 3-62.

a. The deviation monitor A2 (fig. FO 3-36) checks the amplitude of the baseband modulating signal and the output of the circuit drives a DEVIATION meter which provides the peak deviation indication of the 70-MHz rf carrier output of the modulator. The baseband signal, from phase-lock loop amplifier A9, is applied to the monitor circuit through pin 8 of jack J1. The signal is developed across input resistor R1 and is applied to dc amplifier AR1. The output of the amplifier is applied to a gain control circuit consisting of METER CAL ADJ potentiometer R9, common emitter transistor Q1, and resistors R6, R7, and R8, and R10. Resistors R6, R7, and R8 form a voltage divider network, to which a 3-position DEVIATION switch is connected. Thus, the DEVIATION meter is provided with three full-scale ranges (6 kHz, 60 kHz, and 600 kHz). Variable resistor R9 provides the meter calibration adjustment. The output of the gain control circuit is further amplified by dc amplifiers AR2 and AR3, and the peak-detected output is applied to the DEVIATION meter.

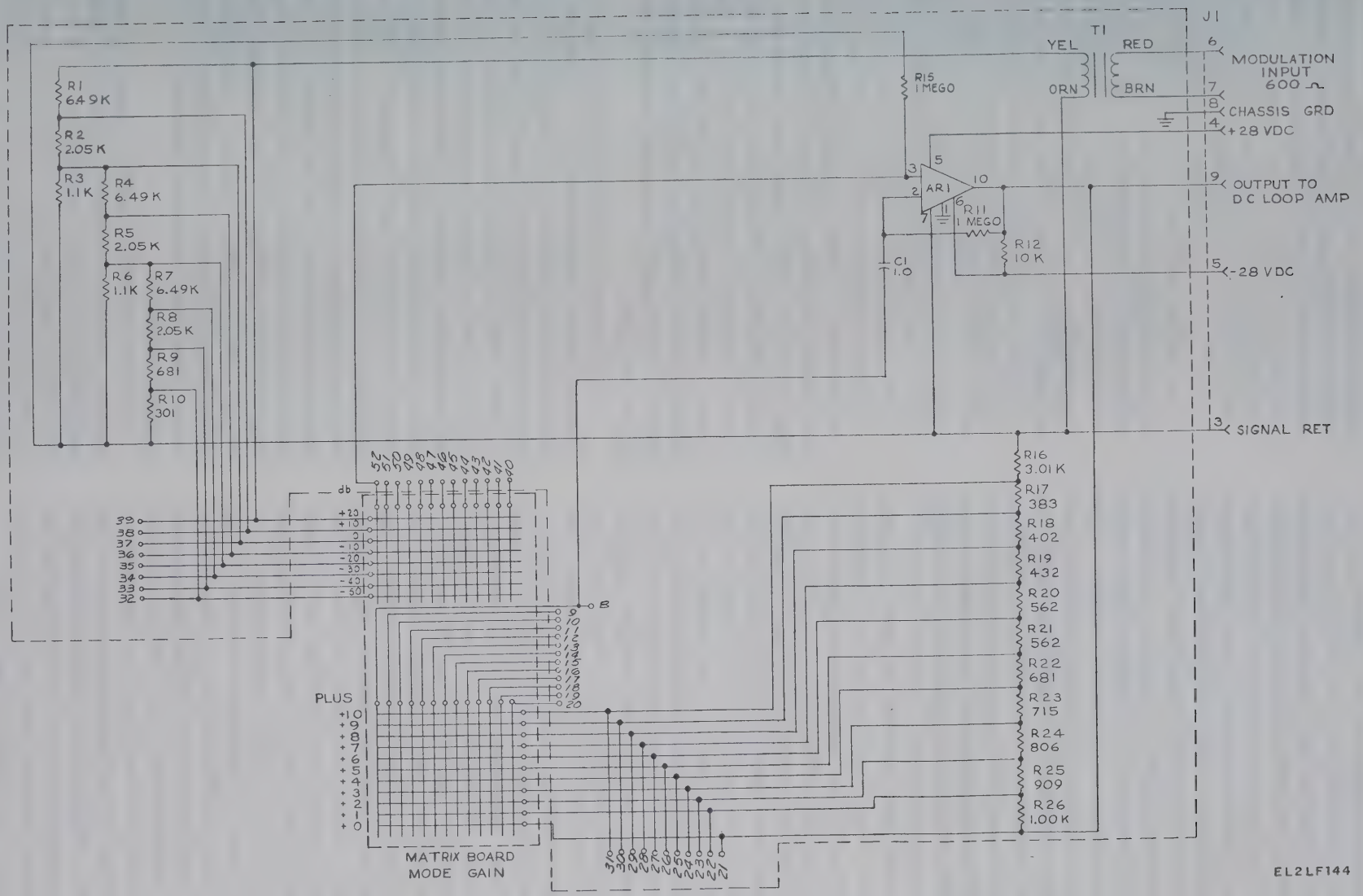


Figure 3-62. Modulation amplifier 1A3A14A1, schematic diagram.

b. The 10 MHz vco (A3) is comprised of an oscillator circuit, two buffer amplifier circuits, and an agc amplifier circuit and is illustrated in figure FO 3-37. The baseband signal from a phase-lock loop amplifier is applied through a 10 MHz vco tank circuit 1A1. The oscillator is frequency modulated by this input, and when the voltage amplitude is at 10 vdc, the 10 MHz center frequency is established. The output of the tank circuit is capacitance coupled to oscillator Q1. The drain terminal of oscillator Q1 is direct coupled to the emitter of current buffer transistor Q2 which is at a dc potential of +15 vdc. The rf current of oscillator Q1 is thus buffered by transistor Q2 which operates as a grounded base amplifier. A rf voltage is developed across variable indicator L2 and is rectified by diode CR2 for application to the age closed-loop network. This detected rf signal, coupled through resistor R35, is inverted and amplified by agc amplifier AR1, and is then applied to oscillator Q1 to close the age loop.

(1) The dc output of amplifier AR1 does not swing negative until the detected rf voltage is more positive than a preset level at the junction of resistors R33 and R34. The high gain of approximately 90 db that is provided by the agc amplifier enables the oscillator to operate as a constant voltage source across induction L2. The agc voltage ranges between −2 vdc and −5 vdc. Inductor L2 is tuned by measuring the agc voltage at test point TP4 with a vtvm and peaking indicator L2 for maximum negative voltage. The dc bias voltage for the agc amplifier and for the phase-lock loop amplifier is established by Zener diode CR5, operating as a shunt regulator. Temperature sensing diodes are contained in the 10 MHz vco tank circuit to provide compensation to the reference voltage developed by diode CR5. The subsequent voltage is applied through resistors R25 and R27 to the phase-lock loop amplifier that generates a positive offset voltage of approximately 10 volts. The vco frequency can be manually varied by adjusting potentiometer R25. The gain of the buffer amplifiers and transistor Q4 is controlled by feedback resistors R11 and R14 for transistor Q3, and by resistors R19 and R21 for transistor Q4.

(2) Each output is transformed-coupled into a 50-ohm load. The 10 MHz output is detected by diode CR7 in conjunction with resistance network comprised of resistors R36, R37, R38, and diode CR21. This output is subsequently monitored by a fault lamp through a fault lamp driver module. The rectified signal voltage across resistor R38 should measure approximately 0.5 vdc. The voltage can be measured using a vtvm at test point TP7 in the level detector and fault lamp driver circuit.

c. The 10 MHz vco tank (fig. 3-63) provides the oscillator frequency control in conjunction with the reference bias voltage network of the 10 MHz vco (*b* above). The tank capacitance is provided by varactor diodes CR1 and CR4 which are shunted across inductor L1 as a Hartley oscillator circuit. Temperature sensing diode CR5 provides temperature compensation for the reference bias voltage network.

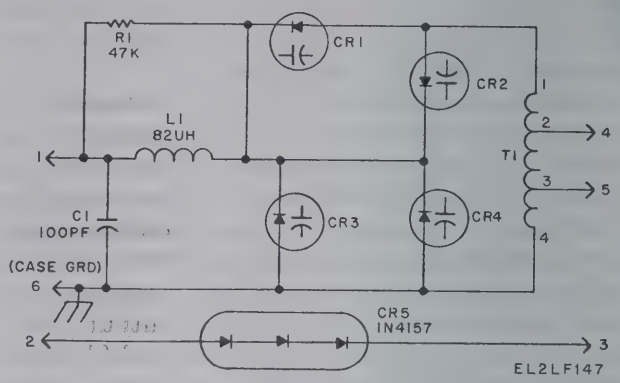


Figure 3-63. 10 MHz vco tank circuit 1A3A14A3, schematic diagram.

d. Power supply A4 furnishes +28 vdc, −28 vdc, +5.2 vdc, and −5.2 vdc regulated power for operation of the modulator. Figure FO 3-38 is a block diagram of the +28 vdc portion of the overall power supply unit. The +28 vdc portion is typical of the other three power supply circuits. The J designations in parenthesis, that appear in the blocks of figure FO 3-38, correspond with jack designations on the power supply schematic diagram shown on figure FO 3-39.

(1) Ac power is applied to the power supply through power transformer L1. Full-wave bridge rectification is performed by module A1. Filtering is provided by inductors L1 and L2 and capacitors C1 and C2 in module A2. The output of the filter is applied to series regulator transistor Q1 through voltage sensing resistor R1. The voltage across resistor R1 is sampled by an error amplifier in module A3, and an error signal is applied to the base of transistor Q1. This signal varies the collector-to-emitter resistance of the stage and since the transistor is in series with the line voltage, the voltage variation across transistor Q1 tends to keep the output voltage constant. Shunt regulator transistor Q3 functions the same way, except that the resistance of this stage is in parallel with the power supply load and therefore shunts dc to power supply common.

(2) The modulator power supply is protected against excessive output loading by means of solid-state switching. Normally, relay K1 in module A2 is deenergized, and +28 vdc is supplied as an output through make contacts of the relay. If the output voltage from series regulator transistor Q1 drops excessively, the low voltage sensing circuit of the error amplifier in module A3 is activated. The

error amplifier then generates a trigger pulse that fires silicon-controlled rectifier (scr) Q1 in module A2. The closed circuit provides a return for relay K1 that energizes the relay. Relay break contacts then remove the output voltage from the power supply load. After correcting the malfunction, the circuit can be returned to normal operation by resetting switch S1. The manual reset opens the relay armature circuit and turns the scr off. Filters FL1 through FL7 are rfi filters.

e. Power transformer T1 and filter inductors L1 through L4 are chassis-mounted components and are connected through cabling to printed wiring board assemblies A1 through A7. The output of transformer T1 is applied to bridge rectifier circuit (fig. 3-64) through connector J4 (fig. FO 3-39). The rectifier voltage is then applied through filter inductors L1 and L2 for the +28 vdc output, filter inductor L3 for the −28 vdc output, and filter inductor L4 for the −5.2 vdc output. Choke input filtering is used. Transistors Q1 and Q2 are used as the series regulators for the +28 vdc and −28 vdc outputs, respectively. Transistors Q3 and Q4 are used as the shunt regulators for the +28 vdc outputs, respectively.

f. The capacitor and relay circuit board provides filtering capacitors and the excessive loading protection relay for the modulator power supply. The schematic diagram of the circuit is shown on figure 3-65. Provided the voltage output remains at the proper level, relay K1 is deenergized. In this state, +28 vdc is applied through relay contacts 1 and 2, and the power supply common circuit is applied through relay contacts 4 and 5. Although +28 vdc is present at terminal 7 of the relay coil, the return circuit is open since scr Q1 is in series and is cut off. When a low voltage is sensed by the error amplifier, a trigger signal is received at either terminal 6 or 16. The signal fires scr Q1 into conduction, the return path is closed, and relay K1 becomes energized. This action removes all output voltages by opening the power supply common and +28 vdc circuits. The circuits are restored to normal by pressing switch S1 on the chassis.

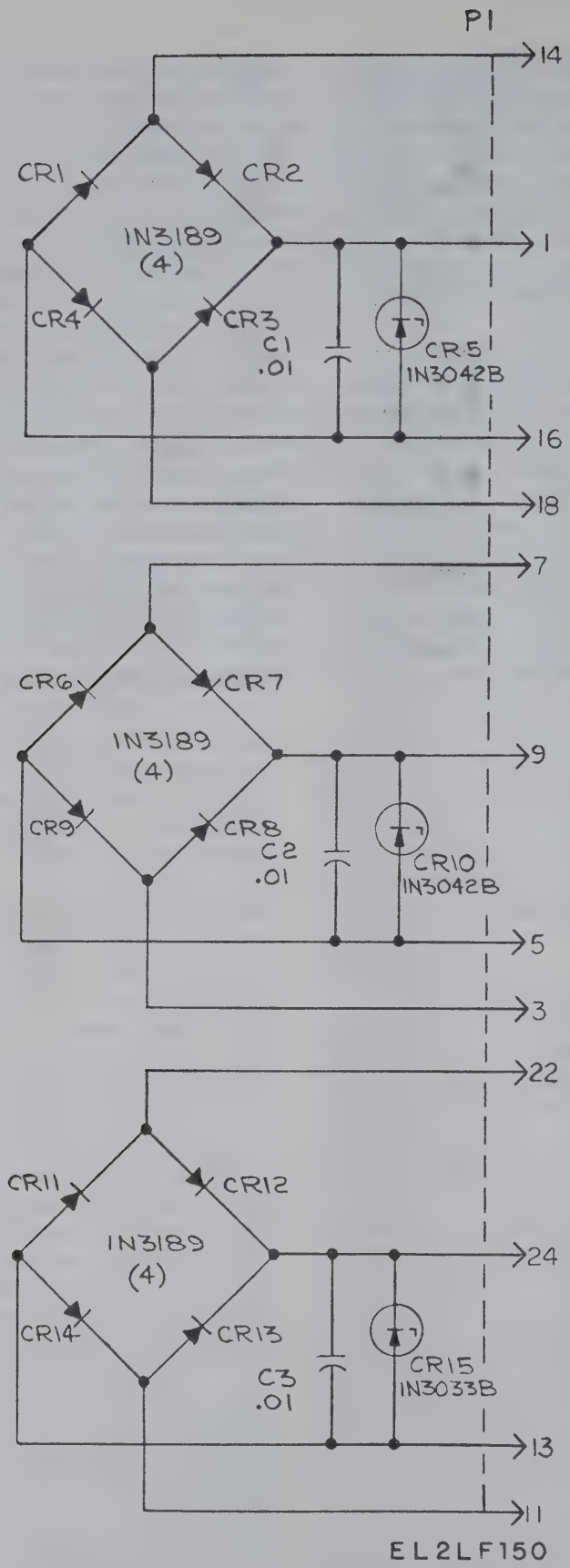


Figure 3-64. Electric rectifier, schematic diagram.

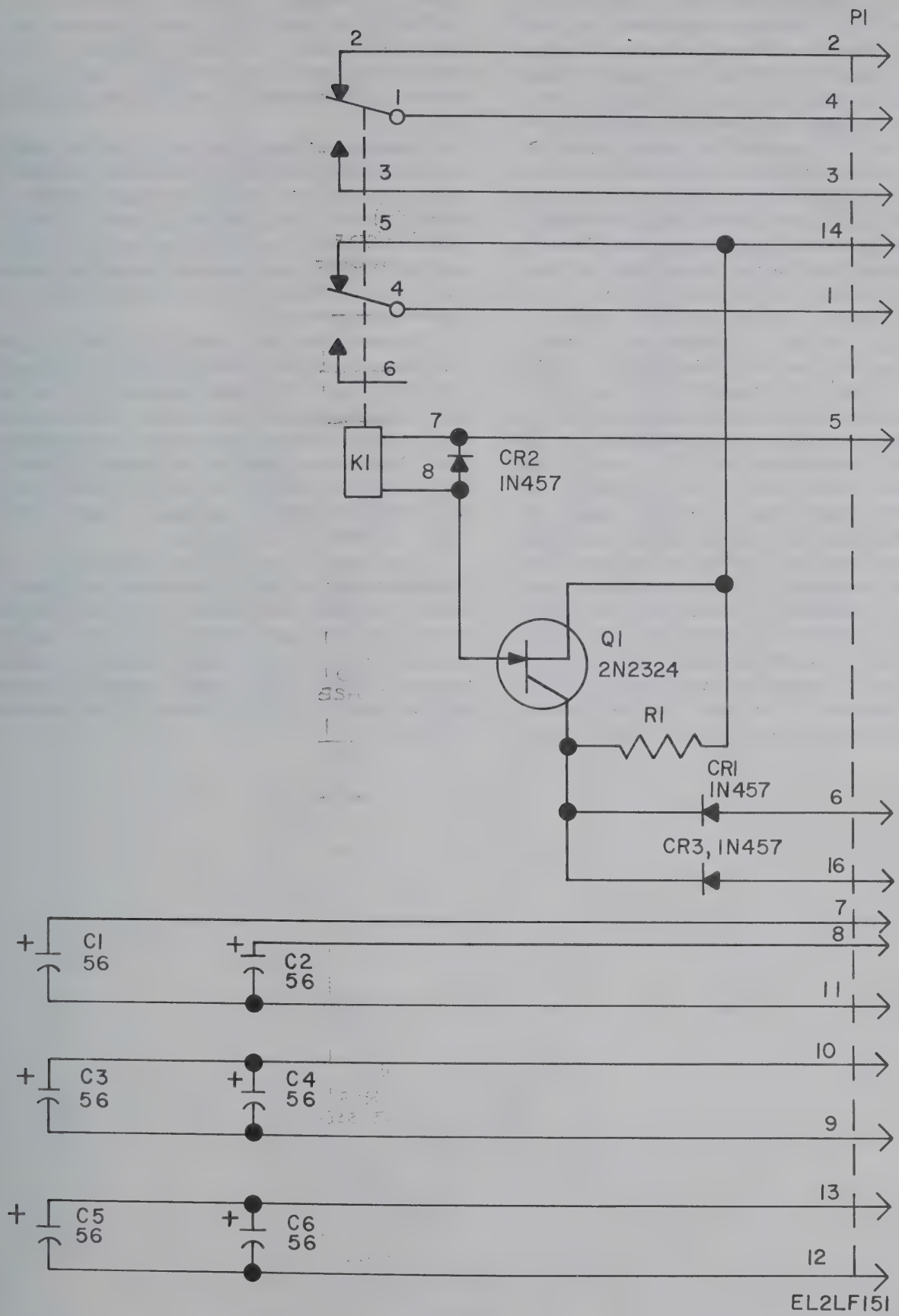


Figure 3-65. Capacitor and relay circuit board, schematic diagram.

g. Current voltage drivers A3 and A4 monitor the +28 vdc and −28 vdc levels, respectively (fig. 3-66). Module A3 senses the voltage drop across resistor R1 and module A4 senses the drop across resistor R2. The voltage drops across the respective resistor R2. The voltage drop acorss the respective resistor (R1 and R2) is sensed by being applied between the base and emitter of transistor Q1 (on module A3 and A4), which is operated class A. Zener diode CR1 is used to establish the reference voltage. Any sensed voltage change, aside from the normal voltage drop across the sensing resistor, results in a change in the collector current of transistor Q1. The output signal is directly coupled to transistor Q2, which is operated as a class A emitter-follower. The amplified voltage is then applied as a correction signal to the base of the applicable series regulator (transistor Q1 or Q2). The regulator then increases or decreases the output current to maintain the +28 vdc or −28 vdc output at the correct level. The error amplifier also provides the trigger power for power supply low-voltage protection. The output of the series regulator is monitored and applied to the base (B_2) of unijunction transistor Q3. The unregulated positive voltage is applied to the emitter. This voltage is divided by resistor R7, diode CR5, and Zener diode CR6 so that transistor Q3 is backbiased. If the power supply output voltage drops to the level at which transistor Q3 emitter is forward biased, the unijunction is turned on to develop an output signal as a trigger to turn on silicon-controlled rectifier Q1 in module A2. As soon as the load is removed by relay K1, the unijunction circuit returns to normal. Power supply output is not restored until the relay is reset by pressing switch S1.

h. The 5.2-volt regulator maintains the positive and negative 5.2 volt levels in a manner similar to the way modules A3 and A4 regulate the 28 volt level (*g* above). The schematic diagram of the circuit is shown on figure 3-67. Level detector AR2 is used as an error signal control amplifier to drive transistor Q1, which in turn, drives series regulator transistor Q2.

i. The reference and control amplifiers (fig. 3-68) operate in a manner similar to that of modules A3 and A4 (*g* above) to further regulate the +28 vdc and −28 vdc outputs. The output of the modules control shunt regulator transistors Q3 and Q4 (fig. 3-64). Since the regulators are operating class A, adjustments of variable resistor R7 in the control amplifier determines the steady state current value in transistors Q3 and Q4.

j. Bandpass filter A5 (fig. 3-69) receives the 70-MHz output of the X7 frequency multiplier (*k* below). It applies filtered outputs to the communications patching panel and to the level detector and fault lamp driver (*q* below). The filter is a Butterworth circuit using variable capacitor tuning and having a flat 1.4-MHz bandwidth at the center frequency.

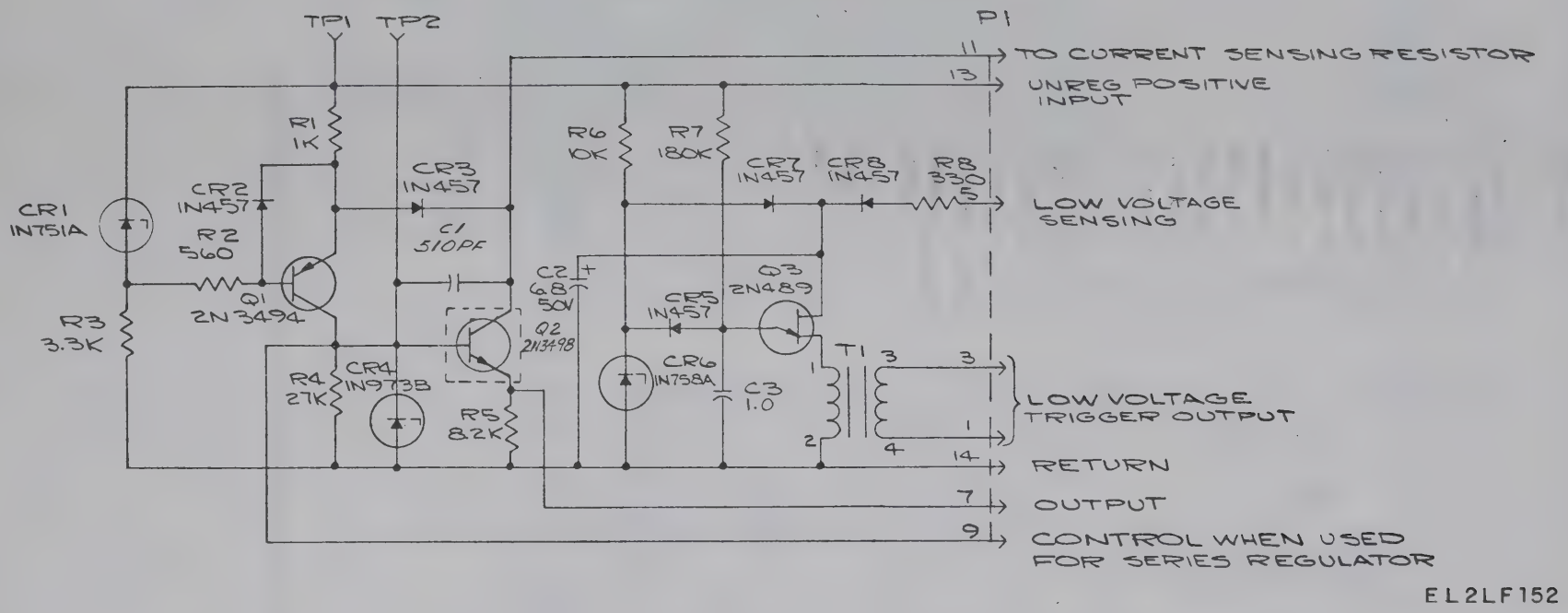


Figure 3-66. Current and voltage drivers A3 and A4, schematic diagram.

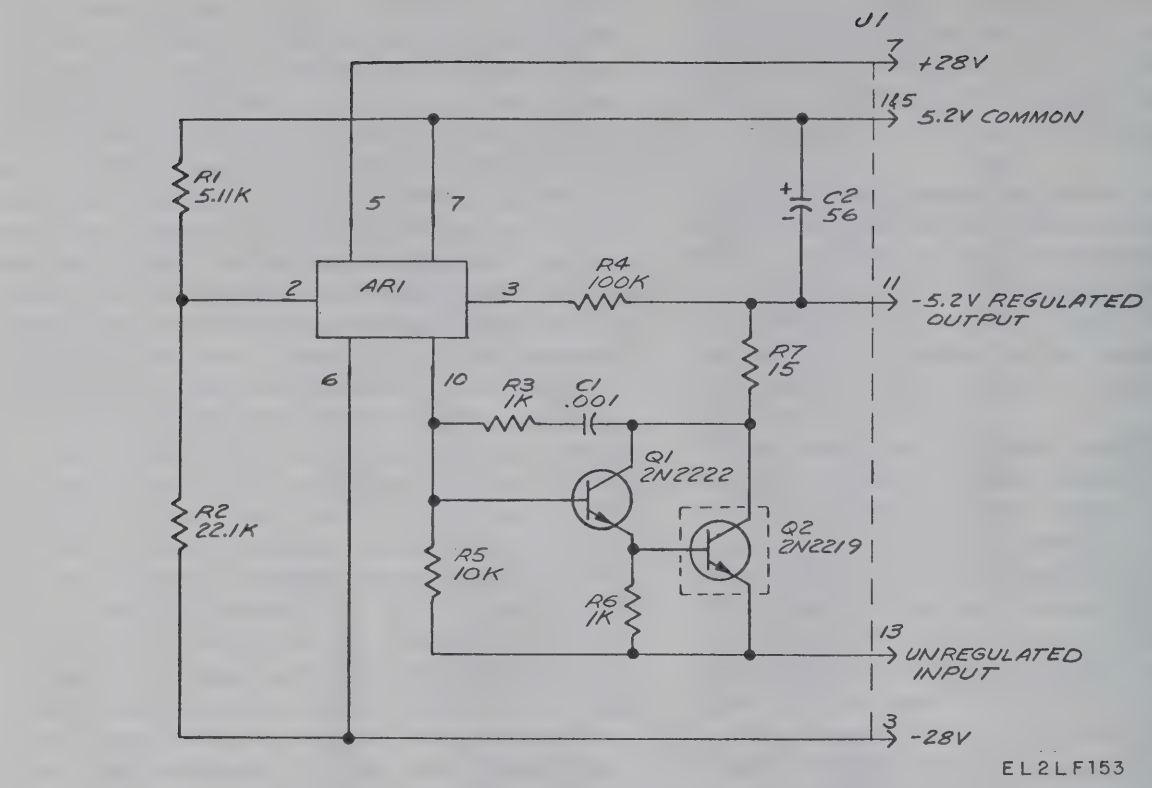


Figure 3-67. 5.2-volt regulator, schematic diagram.

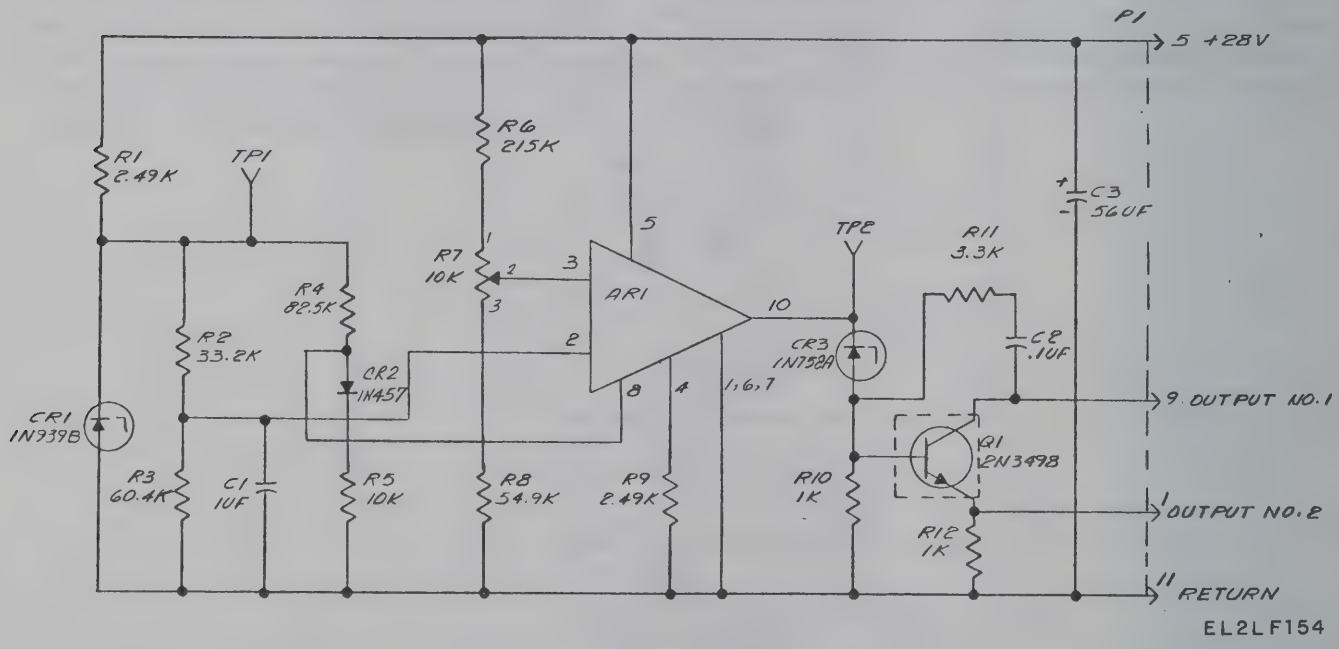


Figure 3-68. Reference and control amplifier, schematic diagram.

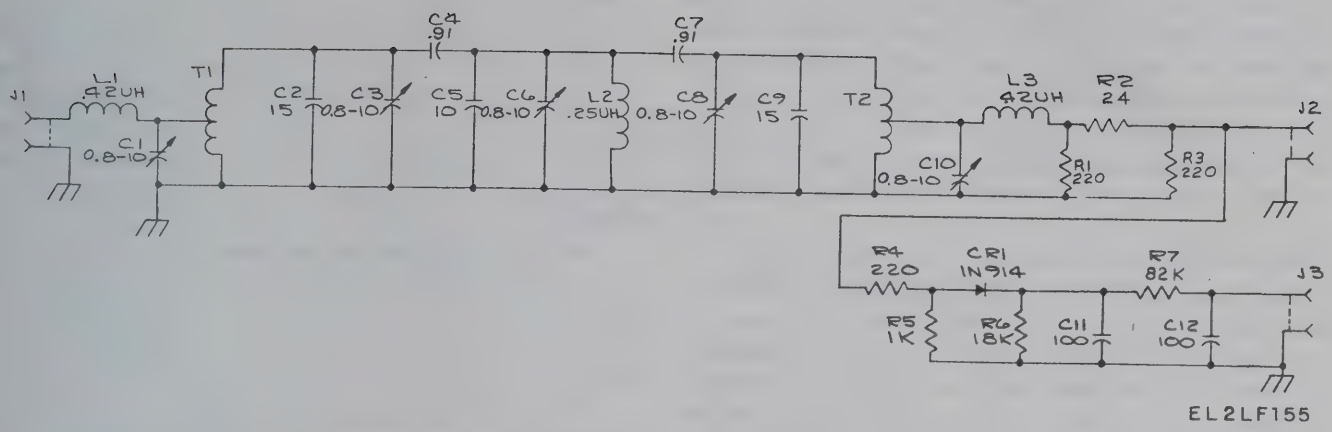


Figure 3-69. 70-MHz bandpass filter 1A3A14A5, schematic diagram.

k. The X7 frequency multiplier A6 (fig. FO 3-40) receives the 10-MHz fm signal from the vco *(b* above), multiplies the frequency by a factor of 7, and applies the resultant 70-MHz signal to the bandpass filter (*i* above). The multiplier consists of a three-stage amplifier with tuned interstage networks to suppress harmonics of the 10-MHz input signal. Input amplifier transistor Q1 operates as a frequency multiplier in conjunction with diode CR1. One milliwatt rf power from the vco is tuned to resonance with the secondary winding of transformer T1, using capacitors C1 and C2. The signal is nonlinearly amplified and applied through the double-tuned interstage network to the base of amplifier transistor Q2. Inductor L2 and capacitor C3, in the first stage collector circuit, form a series-tuned 10-MHz trap, which is loaded by resistor R2. The 70-MHz output response of the first stage is variable inductance tuned by adjusting inductors L3 and L4. Transistor Q2 operates as a linear amplifier. The collector circuit is tuned to 70 MHz resonance by adjusting variable capacitors C13 and C15. The output of the second stage is applied to transistor Q3, which operates as a power amplifier. The output of the third stage is tuned to resonance of 70 MHz by adjusting variable capacitor C18.

l. The ÷ 100 countdown circuit A7 (fig. 3-70) receives the 10-MHz signal from the vco (*b* and *c* above), counts it down to 100 kHz and developes a 100:1 counter fault signal. Negative logic is used in the countdown circuit. That is, a low level (+0.7 ±0.2 volts) represents a logic 1 and a high level (+1.57 ±0.2 volts) represents a logic 0. When a flip-flop is set the true output (pin 5) is low and the false output (pin 4) is high. The true output is high and the false output is low when the stage is reset.

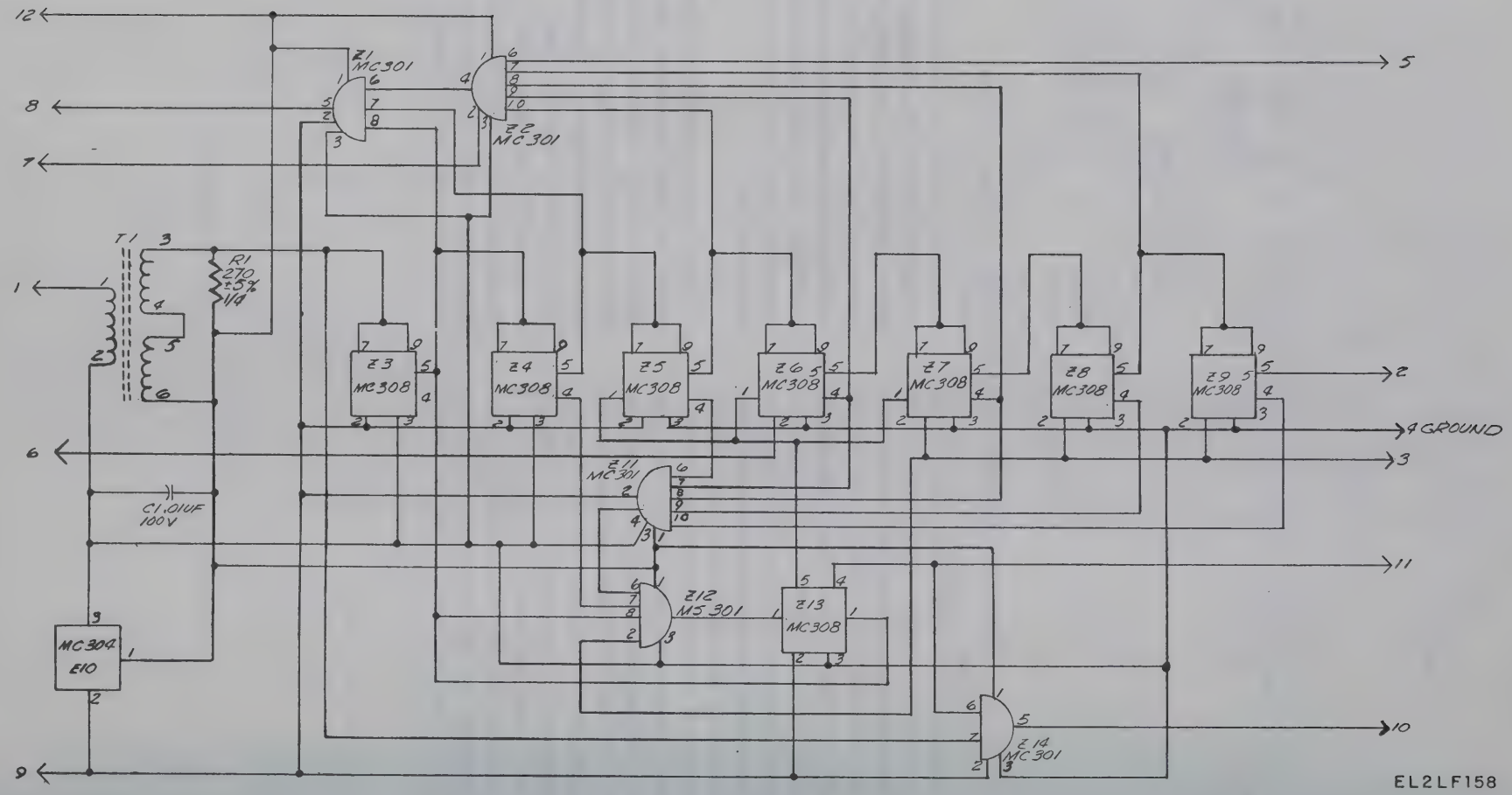


Figure 3-70. Divide by 100 countdown circuit A7, schematic diagram.

(1) The 10-MHz signal is coupled to the first stage of seven-stage counter through input transformer T1. The true output (pin 5) of the last stage (Z9) is applied to an input (pin 6) and AND gate A2, through an external connection between pins 2 and 5 of module AR1 (fig. 3-71). At the count of zero, all counter stages are reset and all inputs to AND gate Z11 are low. The resultant low output of Z11 is applied to NAND gate Z12 as is the low level from the false output of flip-flop Z4 (second counter stage). At the count of one, the first stage (Z3) of the counter is set and pin 8 of gate Z12 goes low, enabling the gate. As a result, the output of NAND gate Z12 goes high and resets flip-flop Z13. The flip-flop produces a high output at pin 5, which sets counter stages Z5, Z6, and Z7, thus, presetting the counter to count 28. At the count of 2, the true output of the first counter stage (Z3) goes high and sets flip-flop Z13 to allow stages Z5, Z6, and Z7 to count normally. The counter would normally clear after 128 Hz of the 10-MHz input. However, with the 28 count preset in the counter, it clears after 100 Hz of the 10-MHz input and the 100:1 countdown function is performed.

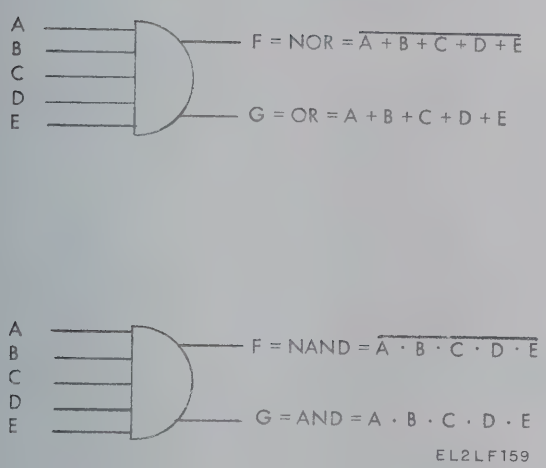


Figure 3-71. Integrated circuit device, typical logic diagram.

(2) During the time flip-flop Z13 is reset, a low level is applied to pin 6 of NAND gate Z41. The next negative half cycle of the 10 MHz input signal enables gate Z14, which produces a 50 nanoseconds high pulse at output pin 5 (module pin 10). This pulse is the 100 kHz 0° signal used to trigger a flip-flop phase detector in 100 kHz phase detector AR2 (*n* below). Because of the delay imposed by flip-flop Z13, the 100 kHz 0° is delayed by 1.5 Hz of the 10 MHz input from the count of 0 in the counter. Gates Z1 and Z2, which operate similar to gates Z11 and Z12, produce a pulse at the count of 103.

(3) The difference between the 128 count and 103 count is equal to 25 counts, which is equivalent to an angle of 90 (3.6 degrees per count). Since the 100 kHz 0° pulse is delayed by 1.5 Hz (5.4 degrees), the 100 kHz 90° signal from gate pin Z1-5 (module pin 8) leads the former by a total of 95.4 degrees. The 100 kHz 90° signal is also sent to phase detector AR2 to trigger another flip-flop. If the 100:1 countdown circuit is working properly, a 100 kHz negative-going pulse appears at pin 4 of flip-flop Z13 (module pin 11). This pulse is used in level detector and fault lamp driver circuit A8 (*q* below) to indicate proper operation of the 100:1 countdown assembly. Bias control Z10 supplies the proper voltage to gates Z1, Z3, Z11, Z12, and Z14.

m. The integrated circuit device (gig. 3-71) is a 5-input gate element that performs the OR/NOR function for positive logic and the AND/NAND function for negative logic.

n. The 100-kHz phase detector AR2 (fig. 3-72) compares the signal from ÷ 100 countdown assembly AR1 (*l* above) with the 100-kHz reference input from the electronic counter and detects any phase (frequency) difference. The detector phase error signal is applied to 100 kHz detector and fault circuitry units AR3 (*o* below) and AR4 (*p* below).

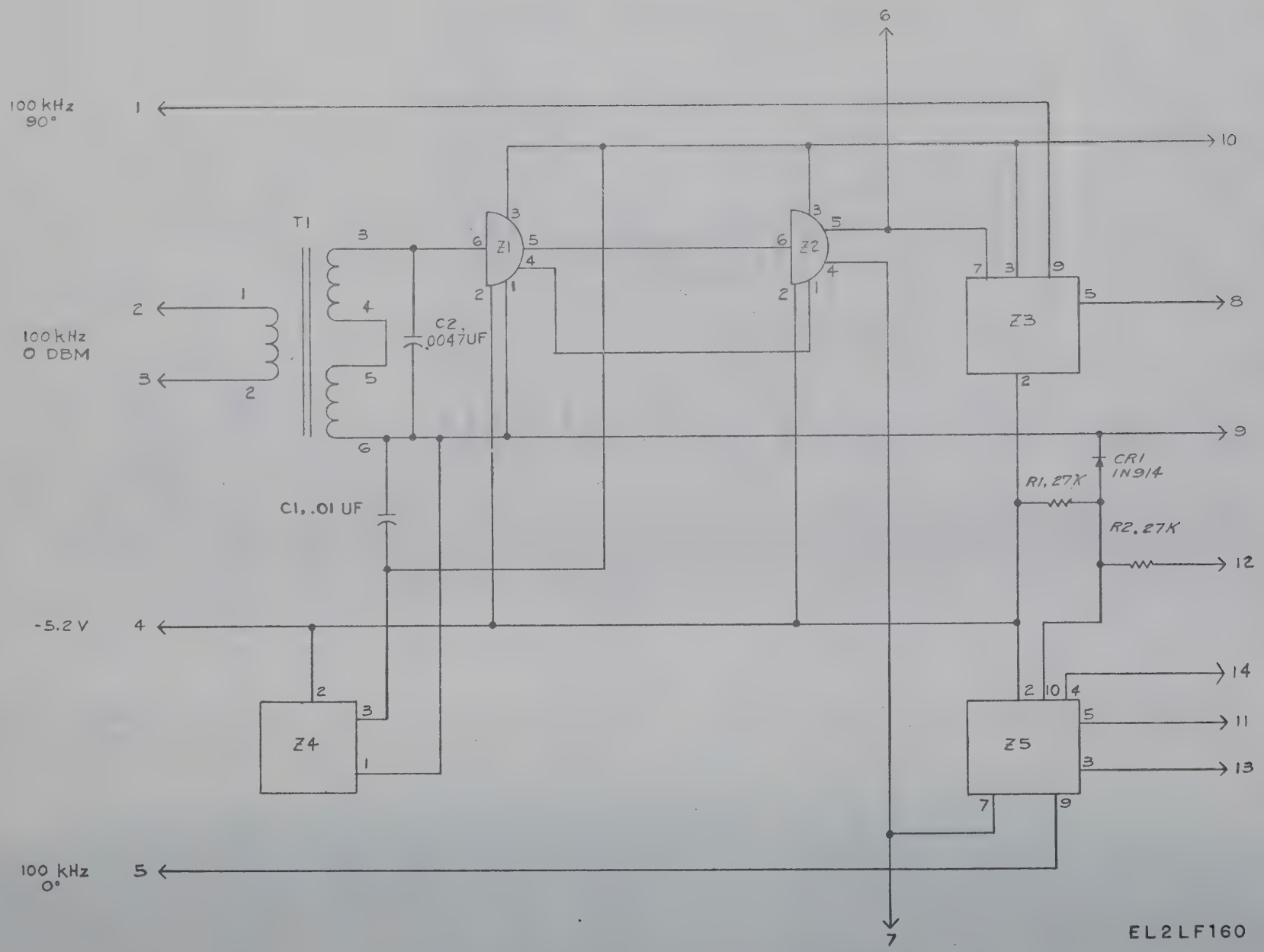


Figure 3-72. 100 kHz phase detector, schematic diagram.

(1) The 100-kHz reference signal is applied to the primary winding of input matching transformer T1. The secondary winding of transformer T1 is connected to integrated circuit device Z1 where the signal is amplified and converted to a square wave. The push-pull outputs of Z1 are applied to integrated circuit device Z2 where the square wave is further shaped (risetime shortened) and the 100-kHz output at pin 5 is applied to the $\overline{J}$ input (pin 7) of flip-flop Z3. The 100 kHz 90° signal (positive pulse), from ÷ 100 countdown assembly AR1, is applied to the $\overline{K}$ input (pin 9) of flip-flop Z3. The asymmetry of the resulting rectangular wave at pin 5 of flip-flop Z3 is a measure of the phase difference between the 100-kHz reference signal and the 100 kHz-90° pulse.

(2) This rectangular waveform is applied to 100 kHz detector AR3 where it is rectified. The resultant dc level is proportional to the asymmetry or phase difference. The output at pin 4 (complement of pin 5) of integrated circuit device Z2 is applied to the $\overline{J}$ (pin 7) input of flip-flop Z5. The 100 kHz 0° (positive pulse), from ÷ 100 countdown assembly AR1, is applied to the K input of flip-flop Z5. Flip-flop Z5 functions the same as flip-flop Z3 to produce a rectangular wave for application to 100 kHz detector AR4. A positive voltage, from an external source, applied to module pin 12, disables flip-flop Z5. Thus, detection of the 100-kHz 0° signal is inhibited. Bias control Z4 supplies the proper voltage to pin 1 of integrated circuit device Z1 and to pin 6 of transformer T1.

o. The 100 kHz detector AR3 (fig. 3-73) receives the 100-kHz rectangular wave and the 100-kHz fault signal from 100-kHz phase detector AR2 (*n* above). The 100-kHz detector rectifies the signals to develop the 100-kHz fault and phase lock fault signals for use in the level detector and fault lamp driver circuit (*q* below). The 100-kHz signal is applied to rectifier diodes CR3 and CR4, through capacitors C4 and C5. The average value of the negative dc voltage across diode CR3 and the average value of the positive dc voltage across diode CR4 are summed through resistors R4 and R5. The difference between the positive and negative voltages appears across capacitor C6 as the phase lock fault signal which is proportional to the asymmetry of the applied 100-kHz rectangular wave. The 100-kHz rectangular wave received at pin 4, from 100 kHz phase detector AR2, is applied to a voltage doubler composed of capacitors C1 and C2 and diodes CR1 and CR2. The signal is filtered by the low-pass filter consisting of resistor R1 and capacitor C3. If only dc voltage is received at pin 4, the dc voltage at pin 7 (the 100-kHz fault signal) is equal to the negative voltage drop across the two diodes (approximately −0.81 volt). When an ac voltage is applied to pin 4, the output voltage at pin 7 is −0.81 volt plus the peak-to-peak voltage applied.

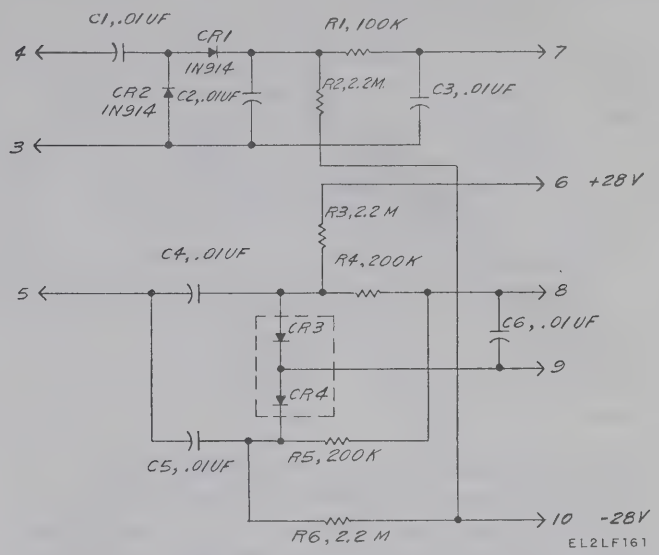


Figure 3-73. 100 kHz detector AR3, schematic diagram.

p. The 100 kHz detector AR4 (gig. 3-74) receives the 100-kHz recangular wave from 100 kHz phase detector AR2 (*n* above) and the 100:1 fault signal from ÷ 100 countdown circuit (*l* above). The unit rectifies the signals to develop the ÷ 100 counter fault signal to the level detector and fault lamp driver circuit and the phase error signal to the phase-lock loop amplifier (*r* below) and 10 MHz vco (*b* above). The push-pull, 100-kHz rectangular wave is applied to the two bases of matched transistor Q1 through pins 5 and 12. As a result, an amplified square wave is developed across resistor R7 and is applied through capacitors C4 and C5 to rectifier diodes CR3 and CR4. The rectified average negative dc voltage across diode CR3 is summed with the rectified average positive dc voltage across diode CR4. The summed dc signal at pin 8 is the phase error output, which is proportional to the asymmetry of the rectangular wave input. The rectangular wave received at pin 4, from ÷ 100 countdown assembly AR1, is applied to a voltage doubler composed of capacitors C1 and C2 and diodes CR1 and CR2. The signal is filtered by the low-pass filter consisting of resistor R1 and capacitor C3. If only dc voltage is received at pin 4, the ÷ 100 counter fault signal at pin 7 is equal to the negative dc voltage drop across the two diodes (approximately −0.81 volt). When an ac voltage is applied to pin 4, the output voltage at pin 7 is −0.81 volt plus the peak-to-peak voltage applied.

q. The level detector and fault lamp driver circuit A8 (fig. FO 3-42) receives five fault signals from units of the radio transmitter modulator and drives corresponding fault indicator lamps on the front panel. The circuits monitored include the ÷ 100 frequency and phase detector (100 kHz fault ÷ 100 fault and phase lock fault signals), 10 MHz vco,

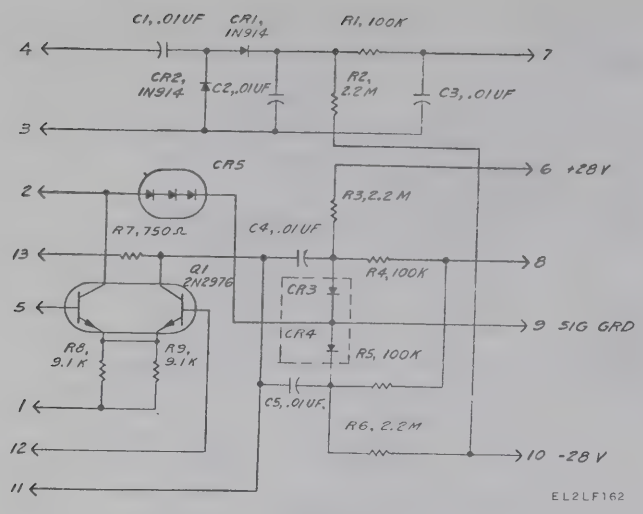


Figure 3-74. 100 kHz detector AR4, schematic diagram.

and X7 frequency multiplier. All five of the level detector and fault lamp driver circuits operate the similar way; therefore, only the 10-MHz vco circuit is discussed. During normal operation, a positive voltage is applied to pin 3 of level detector AR4 through module jack J1-6. In this condition, a positive output from AR4 turns on transistor Q7, the first stage of a cascaded amplifier pair. As a result, transistor Q8 cuts off and the 10 MC VCO indicator lamp is extinguished. When the vco signal drops below the level detector threshold level, transistor Q7 is cut off, transistor Q8 is turned on, and a ground level is applied to illuminate the 10 MC VCO indicator lamp.

r. The phase lock loop amplifier A9 (fig. 3-75) amplifies the baseband modulating signal as a second stage of amplification, acts as an error signal amplifier to correct the vco frequency, and is used a false lock detect circuit to disable the phase detector.

(1) The amplifier baseband signal from the modulation amplifier is applied, through pins 3 and 9, to input gain control potentiometer R3. The potentiometer is an internal adjustment and determines the maximum deviation of the modulator output 70-MHz rf carrier for a given input signal level. The output of gain control potentiometer R3 is amplified by operational amplifier AR1 and applied to the 10-MHz vco (*b* above) and to the frequency deviation monitor (*a* above). Operational amplifier AR1 input terminal 2 receives two input voltages that are summed as the reference input of the amplifier. One input voltage is the error signal from ÷ 100 frequency and phase detector if the vco is not phase locked to the 100-kHz external reference frequency. The other input voltage is the static bias voltage from the vco plus any incremental temperature compensating voltage.

(2) In the absence of a modulating signal, the resulting input voltage is amplified to generate approximately a +10 vdc offset output voltage. (This voltage is the input requirement for the vco for a 10-MHz frequency.) Any phase detector error signal causes the offset voltage to change and subsequently restores the 10-MHz vco frequency to the phase lock condition. The amplified modulating signal is added to the offset voltage bias. The false lock detect circuit is inserted as a second loop in the vco phasing loop to prevent false lock-on with spurious signals (normally during power turn-on). The circuit functions as an inhibit clamp on the phasing loop that holds for a short period of time so the vco can recover to the nominal 10-MHz center frequency. Resistor R7 and capacitor C4 form an integrating network. Dc and low-order ac voltages from the phase detector having sufficient amplitude to cause possible false lock-on are amplified by transistors Q1, Q2, and amplifier AR2. The amplified voltage is then applied to the phase detector as an inhibit voltage.

(3) The output of amplifier AR2 is connected to a time-constant network consisting of capacitor C5, resistor R14, and capacitor C6. Capacitors C5 and C6 charge so that an inhibit voltage is generated. Removal of the spurious signal allows the network potential to decay naturally and remove the inhibit from the phasing loop.

3-24. Baseband Amplifier 1A3A15, Circuit Analysis.

(fig. 3-76 through 3-84 and FO 3-42)

The baseband amplifier essentially processes the voice and teletypewriter send and receive signals and provides metering indications for each signal.

a. The baseband differential amplifiers are used as audio amplifiers and impedance matching devices. As used in the baseband control amplifier, and as illustrated in figure 3-76, pins 1-8 and 1-9 are externally connected to provide a 602-ohm balanced input imedance. The balanced input is applied to pins 1-2 and 1-3. Resistors R2 and R5 provide the 602-ohm input impedance. The input signal is coupled through capacitors C1 and C3 to the bases of transistors Q1 and Q2, respectively. A voltage divider network comprised of resistors R1, R3, R6, and R7 and capacitor C2, which is connected between +28 volts and ground, provides the forward bias for transistors Q1 and Q2. Transistor Q1 is an npn type and transistor Q2 is a pnp type. The emitters are connected together through resistor R4. The direction of dc is from the −28 volt source through collector resistor R8, transistor Q2, resistor R4, and transistor Q1. The two signals on the bases of transistors Q1 and Q2 are 180° out-of-phase and will increase and decrease conduction through the transistors at the same time. The output is taken from the collector of transistor Q2 and is coupled through capacitor C4 to output pin 1-10.

Figure 3-75. Phase lock loop amplifier 1A3A14A9, schematic diagram.

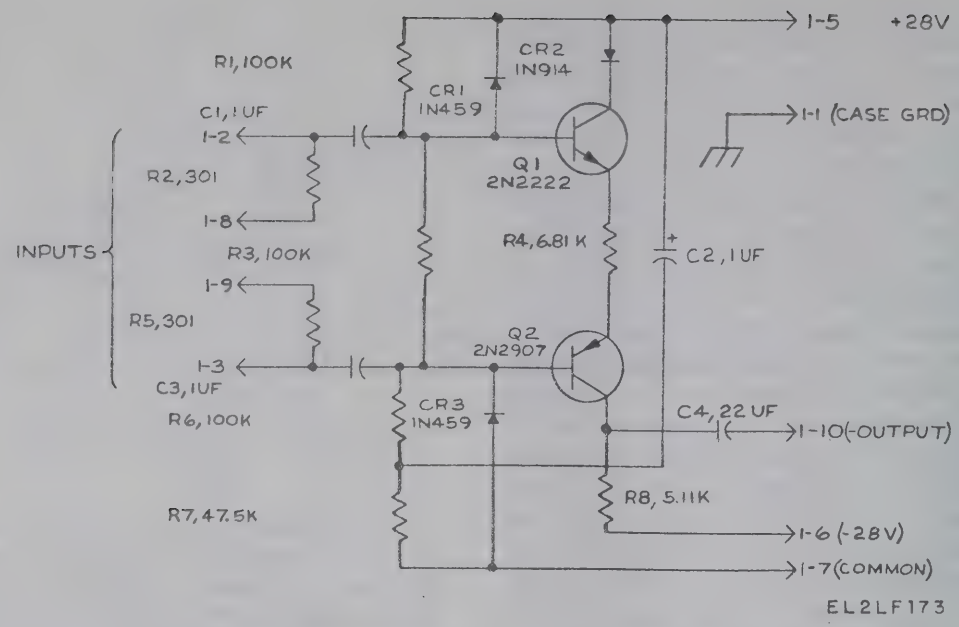


Figure 3-76. Baseband differential amplifier, schematic diagram.

b. The detailed circuit analysis for baseband operational amplifier A4 is the same as for baseband operational amplifier A3, except for the use of diode CR3 in place of resistor R4. The circuit is shown on figure 3-77. Diode CR3 is a field-effect current limiting diode. Diode CR3 is always forward biased and supplies a constant current to dc amplifier A1. Diode CR3 provides protection for the output transistors of dc amplifier A1 when the external circuit connected to pin 1-9 is interrupted during switching operations.

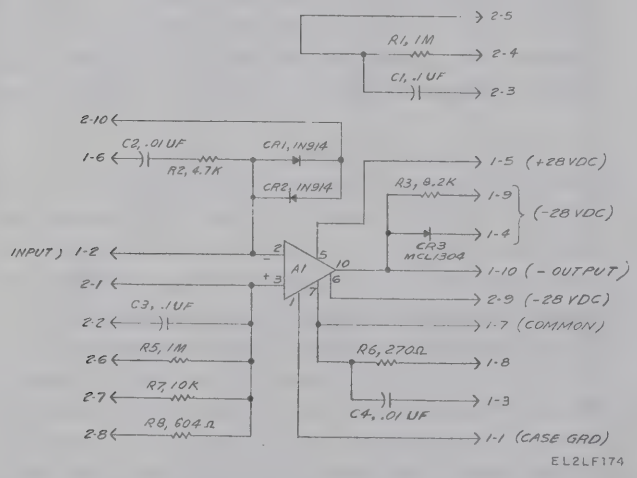


Figure 3-77. Baseband operational amplifier, schematic diagram.

c. The detailed circuit analysis for dc amplifier A1 is the same as for dc amplifier AR1 (para 3-28*c*), except for frequency response. Capacitor C2 (fig. 3-78) has less capacitance than the equivalent capacitor in the AR1 module.

d. The meter compensation network (fig. 3-79) has six transistors, two 5.6-volt breakdown diodes and a 4-diode bridge. By selectively connecting the

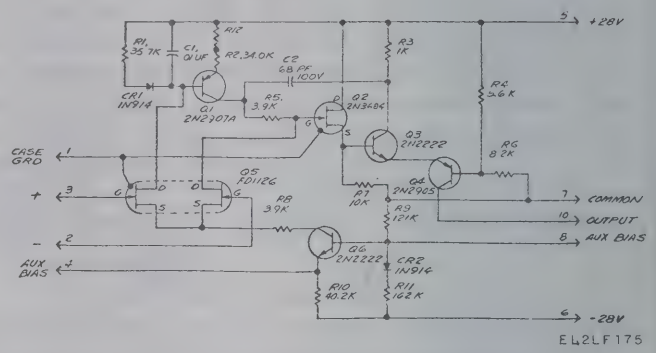


Figure 3-78. Dc amplifier A1, schematic diagram.

network in different configurations it is possible to use one meter to indicate different ranges of signal levels. The signal to be measured is applied to pin 4 and the meter is connected across pins 3 and 9. Breakdown diodes CR1 and CR2 are connected back-to-back to prevent the input level from exceeding +5.6 volts. The circuit is used in conjunction with an operational amplifier that supplies the input signal to pin 4. Diodes CR3 through CR6 are connected as a full-wave bridge in the feedback path of the amplifier. Resistor R5 is the meter shunt resistor and determines the full-scale reading of the meter. Since the meter is connected across the output of the full-wave bridge, the current polarity to the meter will remain the same, regardless of the polarity applied to the input.

e. The baseband preemphasis network A25 is used to accentuate the higher baseband frequencies by connecting sections of the preemphasis network as feedback networks across operational amplifiers to establish the response of the amplifiers. The circuit is shown on figure 3-80 and consists of four resistors and four capacitors connected in a series parallel arrangement.

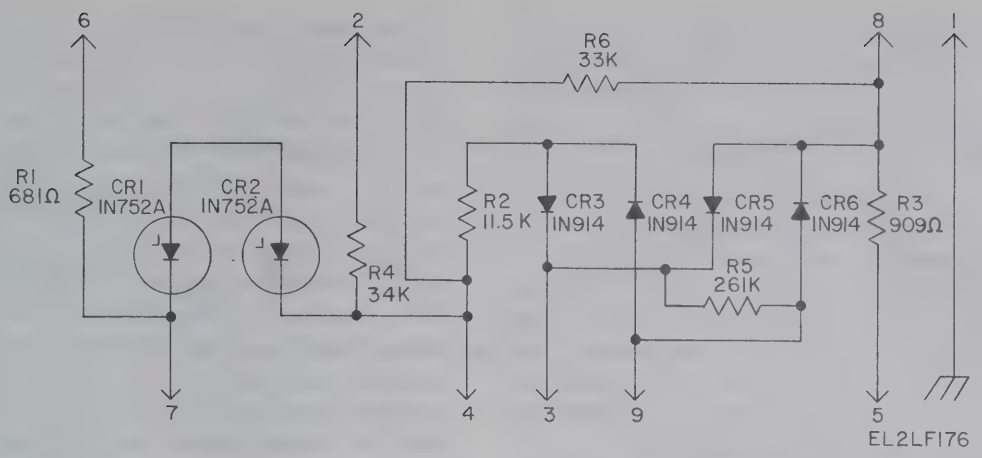


Figure 3-79. Meter compensation network, schematic diagram.

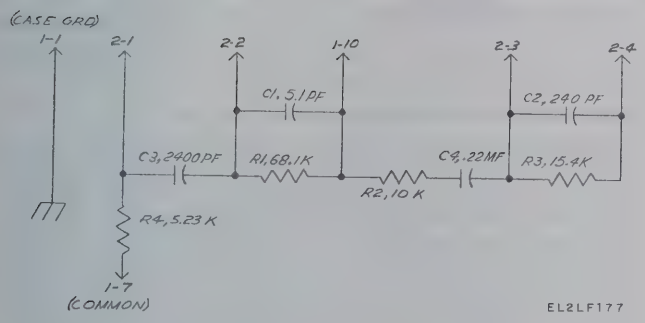


Figure 3-80. Baseband preemphasis network A25, schematic diagram.

f. The preemphasis network A32 consists of four resistors (fig. 3-81) that produce a flat frequency-versus-amplitude characteristics for normal fm transmission. This is accomplished by also connecting sections of the preemphasis network as feedback networks across operational amplifiers.

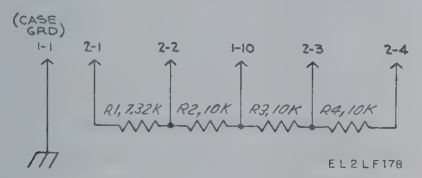


Figure 3-81. Baseband preemphasis network A32, schematic diagram.

g. The twin-tee network and level control circuit is used in conjunction with an operational amplifier to form a 1-kHz oscillator. The circuit is shown on figure 3-82 and is comprised of six resistors, two capacitors, two diodes, and band suppression filter N1. The 1-kHz input is applied through pin 1-10 to the junction of resistors R4 and R5. From the junction of resistors R4 and R5, the signal is applied through resistor R4 and the positive half-cycle is clipped by diode CR1. The remaining negative pulse is applied through resistor R3 and capacitor C1 to pin 1-3. Resistors R1 and R2 form a voltage divider to establish the dc reference level at pin 1-3. The negative 1-kHz output pulse at pin 1-3 is applied to the noninverting pin of the associated operational amplifier. From the function of resistors R4 and R5, the signal is applied through the combination of resistor R5 and capacitor C2 and the positive half cycle is clipped by diode CR2. The resulting negative pulse is applied through band suppression filter N1 to pin 1-2. The output at pin 1-2 is applied to the inverting pin of the associated operational amplifier. Resistor R6 provides the common return path for filter N1.

h. The baseband preemphasis network A37 is used to accentuate the higher baseband frequencies by connecting sections of the preemphasis network as feedback network across operational amplifiers to establish the response of the amplifiers. The circuit is shown on figure 3-83 and consists of five resistors and network N1.

i. Input/output signal characteristics for baseband preemphasis network N1 are shown in figure 3-84.

3-25. Converter-Keyer and Echo Suppressor 1A3A16, Circuit Analysis.

(fig. 3-85 through 3-89 and FO 3-44 through FO 3-46)

The converter-keyer and echo suppressor unit provides mounting and interconnection facilities for three frequency shift keyers, three frequency shift converters, and an echo suppressor. The detailed circuit analysis for circuits within the converter-keyer and echo suppressor is given in *a* through *e* below.

a. The frequency shift keyer as illustrated in figure FO3-45 is a transistorized digital tone device which converts dc binary inputs into two different output audio-frequencies representing mark and space pulses. These output frequencies are determined by crystals within the keyer.

(1) The dc intput from the send loop is applied across pins 16 (+) and 5 (−) through fuse F2 and resistor R4 to U1 (pin 5). Logic element U1 functions as a switch which controls the conduction of Q1. The output of Q1 is fed through R1 to S-M-L-OFF switch S1. When in this position, the Q1 out-

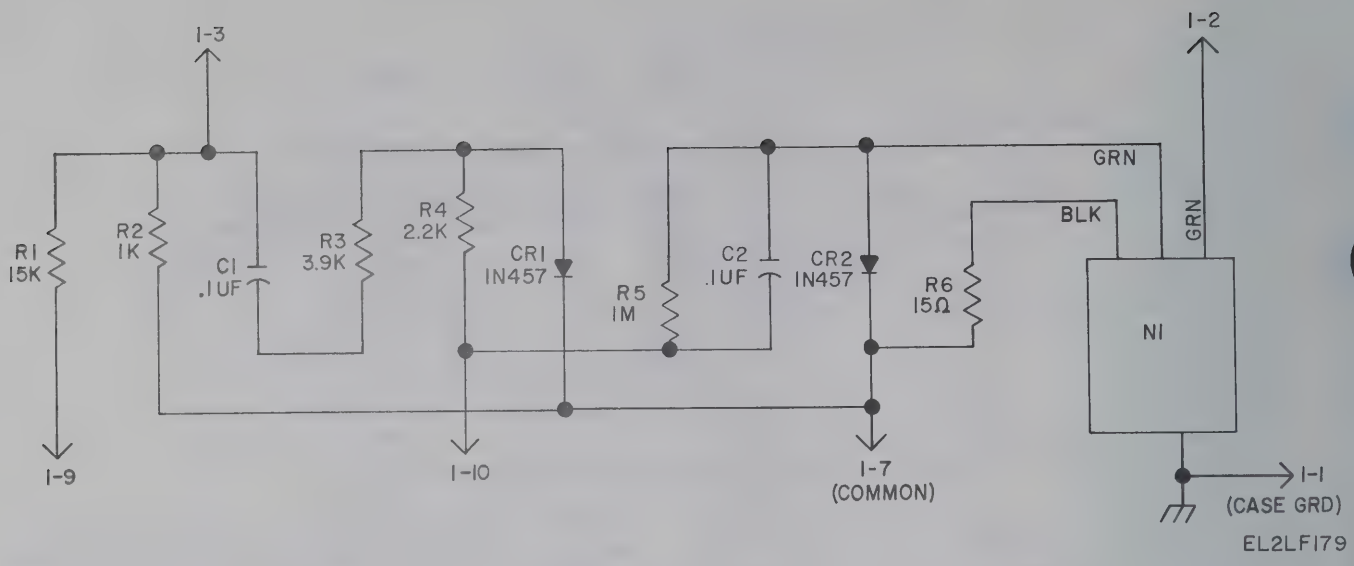


Figure 3-82. Twin-tee network and level control circuit, schematic diagram.

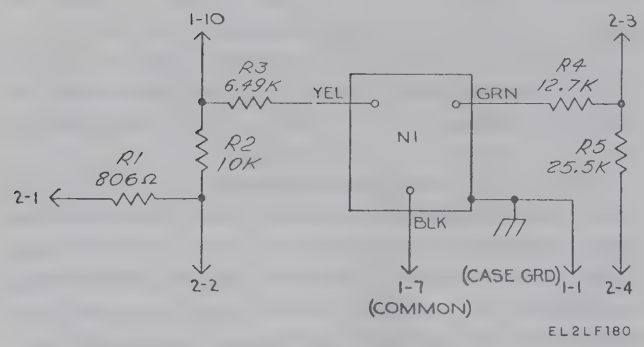


Figure 3-83. Baseband preemphasis network A37, schematic diagram.

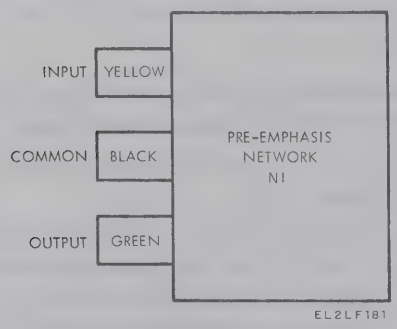


Figure 3-84. Preemphasis network N1, input and output characteristics.

put is fed through the switch to the Schmitt trigger. The switch is placed in the M or S position during test operation when a steady mark or space (respectively) is required. When the switch is in the M position, no signal is applied to the keyer Schmitt trigger resulting in the input transistor of the trigger being cut off. When the switch is in the OFF position, ground is applied to the keyer six-stage divider output and to the driver circuit to prevent the keyer from producing an output.

(2) The Schmitt trigger circuit consists basically of a Schmitt trigger and an inverter. The input signal from the input isolation relay is applied through coupling resistor R5 and taken across resistor R6 and clipper diode CR1 to the base of transistor Q1 of the Schmitt trigger. Transistors Q1 and A2 are from the Schmitt trigger circuit. Resistors R7 and R9 are collector bias resistors, while resistor R8 is the common emitter to ground resistor. The trigger shapes the input signal from the relay and produces a normalized square wave output representing the mark or space data. The output of the trigger is applied to the gating circuits and also through coupling resistor R10 to the base of inverter transistor Q3. Transistor Q3 inverts the square wave from the trigger and applies it to the keyer gating circuits. Therefore, the gating circuits receive two complementary square saves from the Schmitt trigger circuit, one the inverse of the other. Resistor R11 is the collector bias resistor for transistor Q3. Diode CR2 maintains the emitter of transistor Q3 slightly above ground potential, the remainder of the +12 vdc bias is dropped across resistor R12. If direct keying operation is used (this requires a special socket which replaces the input isolation relay K1), strap E is made.

(3) The gating circuits consists basically of sense switch S2 and diodes CR3 through CR6. To simplify the discussion of these circuits, three separate conditions will be analyzed; that is steady mark, steady space, and mark-space keying. If a steady mark condition exists, the normal mark signal from transistor Q2 of the Schmitt trigger is applied to pins 3 and 4 of switch S2; simultaneously, the inverted mark signal from transistor Q3 of the Schmitt trigger is applied to pins 1 and 6 of switch S2. Switch S2 selects either direct (mark frequency higher than space frequency) or indirect (space frequency higher than mark frequency) keying sense.

(4) With switch S2 in the DIRECT position, the

normal mark signal is applied through resistor R19 to the anode of diode CR4, reverse biasing the diode. Also the inverted mark signal is applied through resistor R18 to the anode of diode CR3, forward biasing the diode. The high frequency signal from the oscillator is coupled through resistor R35, capacitor C7, and the parallel rc network consisting of resistor R20 and capacitor C5, to the anode of diode CR3. The low frequency signal from the oscillator is coupled through resistor R22, capacitor C8, and the rc network consisting of resistor R21 and capacitor C6 to the anode of diode CR4. Since the normal signal from the Schmitt trigger circuit has reverse biased diode CR4, and the inverted signal has forward biased diode CR3, the high frequency signal is passed through the gate when the mark signal is applied.

(5) When the sense switch is in the INDIRECT position, the normal signal from the Schmitt trigger is applied to the anode of diode CR3 and the inverted signal to the anode of diode CR4. Therefore, in this condition, the low frequency signal is passed through the gate when the mark signal is applied. Series rc networks consisting of resistor R35 and capacitor C7 and resistor R22 and capacitor C8 shape the signals from the high and low frequency oscillator, respectively, into sharper positive-and negative-going edges. Diodes CR5 and CR6, respectively, clip the positive portions of these signals just above 0 volt. Parallel rc networks consisting of resistor R20 and resistor R10 and capacitor C5, and resistor R21 and capacitor C6, respectively, are *speedup* networks which further sharpen the signal edges for quicker saturation and cutoff of subsequent transistor stage. The output of the gating circuits is applied to the keyer oscillator output shaper. If the steady space condition exists, the normal space signal is applied to pins 3 and 4 of switch S2 while the inverted space signal is applied to pins 1 and 6.

(6) With switch S2 in the DIRECT position, diode CR4 becomes forward biased with diode CR3 reversed biased. Therefore, the low frequency signal is applied through the gate. If switch S2 is placed in the INDIRECT position, diode CR4 becomes reversed biased and diode CR3 forward biased. In this case, the high frequency signal is applied through the gate. In normal operation with both mark spaces being keyed, the operation of the gating circuit is a combination of the individual conditions discussed previously.

(7) The oscillator output shaper is a fast-switching Schmitt trigger circuit having rc coupling. The high or low frequency signals from the keyer gating circuits are applied to the base of transistor Q5 of the shaper. A positive-going edge of an input signal quickly saturates transistor Q5 resulting in a relatively sharp negative-going signal at the collector. Simiarly, a negative-going edge of an input signal quickly cuts off transistor Q5 resulting in a relatively sharp positive-going signal at the collector. Therefore, from input to output, the risetime and falltime of a signal are decreased, resulting in a *more square* signal. The collector of transistor Q5 is coupled to the base of transistor Q6 by a *speedup* rc network consisting of resistor R14 and capacitor C4. The network further sharpens the leading and trailing edges of the signal resulting in a further decrease in the risetime and falltime of the signal and an increase in saturation and cutoff of transistor Q4.

(8) The accumulative effort of decreasing risetime and falltime in the shaper circuit squares the sinewave mark or space signal from the high and low frequency crystal oscillator. This square wave output, taken from the collector of transistor Q4, is applied to the keyer six-stage divider. Resistors R13 and R16 are collector bias resistors for transistors Q4 and Q5, respectively. Resistor R15 is the common emitter to ground resistor for the shaper. Resistor R17 provides base bias for transistor Q5.

(9) The 6-stage divider is composed of two identical RC coupled high-speed counter circuits and four RC coupled common counter circuits connected in cascade. Each stage produces an output signal with a frequency one-half the input frequency. Hence, the output of the 6-stage divider is 1/64 the input frequency. Since the input signal is 64 times the required mark or space frequency, the divider output is at the required mark or spacing frequency. The squarewave input to the divider is fed to the first high frequency stage of the divider.

(10) Assuming the state of the stage is such that a positive output is at the collector of transistor Q13, then Q13 is cut off and transistor Q12 is saturated. The base potentials are zero vdc to transistor Q13, through base resistor R57; and above zero vdc to transistor Q12, through the various feedback networks. Under these conditions, steering diode CR7 is forward biased and steering diode CR8 is back-biased. The junction of capacitor C18 and diode CR7 is approximately zero vdc, and the junction of capacitor C19 and diode CR8 is approximately 12 vdc.

(11) When a positive square wave is an input, the leading and trailing edges are spiked through the differentiating circuit consisting of capacitor C18 and resistor R50. Steering diode CR7 blocks the positive spike and gates the negative spike to the base of transistor Q12. Transistor Q12 is cut off and the rising edge of the signal at the collector is high-speed coupled to the base of transistor Q13 through the RC network consisting of capacitor C20 and resistor R56. Transistor Q13 is saturated and the collector output goes negative. The state of

the stage is now reversed and the next negative-going edge of a square wave input will switch the stage back to the initially assumed state. Resistors R51 and R55 are collector bias resistors for transistors Q13 and Q12, respectively. Resistor R54 is the common emitter to ground resistor for the flip-flop. The RC network consisting of capacitor C18 and resistor R50, and capacitor C19 and resistor C58 are differentiating networks for steering diodes CR7 and CR8, respectively. Resistors R53 and R57 are the base resistors for transistors Q12 and Q13, respectively. The RC networks consisting of capacitor C17 and resistor R52, and capacitor C20 and resistor R56 are high-speed coupling networks in the feedback loops of the flip-flop Q12 and Q13.

(12) The remaining stages of the divider operate in a similar manner. The difference between the first two stages and the last four stages is in the input coupling used. In the past four stages, capacitors C25, C28, and C34 are used to couple the output of the preceding stage into the following stages. All other components serve the same functions as in the first stage. Resistors R76, R85, R94, and R103 provide discharge paths for the coupling capacitors. Capacitor C37 provides an ac discharge path to ground. The last stage produces two complementary outputs which are applied to the output driver circuit.

(13) The output driver circuit consists of emitter-follower transistor Q24 and impedance matcher transistor Q25. The base of each transistor receives complementary signals from the sixth stage of the divider. During one half-cycle of the output frequency signal, the normal mark or space signal saturates transistor Q24, thereby coupling the pulse to the bandpass filter and providing a 600 ohm impedance. When transistor Q24 is saturated, transistor Q25 is cut off since it receives the inverted mark or space signal. Now, during the second half-cycle, transistor Q24 is cut off representing an infinite impedance to the filter. However, transistor Q25 is saturated representing a 600 ohm impedance to the filter. Resistor R117 provides collector voltage for transistor Q24. Resistors R104 and R107 are base coupling resistors for transistor Q24 and Q25, respectively. Resistor R105 is the emitter resistor for transistor Q25.

(14) The bandpass filter converts the square wave input from the driver into an audio tone sinewave output which is coupled through inductor L1 across capacitors C40 and C47 to the output aggregate. The filter output is coupled through rf suppression filter L1, capacitor C40 and transformer T1 to pins 23 and 24 of connector P1. These terminals, with respect to ground, reflect an impedance of 600 ohms at the discrete bandpass frequencies. Also, this output may be used in parallel with other keyer outputs having different frequencies without changing the characteristics impedance.

(15) The output of transistors Q24 and Q25 is slightly less than 0 dBm. Transistor Q26 has been added to provide an additional stage of amplification. Transistor Q27 serves as an emitter-follower.

(16) The power supply operates off +28 vdc and produces +11.6 and +12.0 vdc regulated and +27 to +28 vdc unregulated. Fuse F1 protects the line power circuit. Inductor L4 and capacitors C43 and C44 constitute a line voltage filtering network. Resistor R109 drops the line voltage to +12.0 vdc which is kept constant by Zener diode CR19 and filtered by capacitor C41. +27 to +28 vdc unregulated is developed at the junction of resistor R110 and the positive side of capacitor C42 for use by transistors Q26 and Q27.

b. The frequency shift converter is illustrated in figure FO 3-46 and essentially converts discrete mark and space tones into corresponding dc binary signals as outlined in (1) through (15) below:

(1) Bandpass filter FL101 receives the input aggregate audio tone signal and filters out all frequencies except the discrete band of frequencies containing the mark and space tones of the particular channel under consideration. The input signal is applied across pins 24 and 12 of connector P1 to the input of the filter. The filtered tone signal is then applied to the push-pull amplifier-limiter. Resistor R103 establishes the output impedance of the bandpass filter.

(2) The push-pull amplifier-limiter is composed of a push-pull amplifier-limiter stage and a push-pull limiter stage. The total effect of the circuit is to provide a constant amplitude output by amplifying weaker signals and limiting stronger signals. The filtered tone input is transformer-coupled by transformer T1 to a push-pull amplifier-limiter stage composed of transistors Q1 and Q2. Resistor R5 is a common emitter to ground resistor. The center tap of the secondary of transformer T1 is biased by the voltage developed across the voltage divider consisting of resistors R3 and R4 (which is energized by −12 vdc capacitor C1 in an ac discharge path to ground). The output of the push-pull stage is transformer-coupled by transformer T2 to a push-pull limiter stage consisting of transistor Q2 and Q4.

(3) The push-pull limiter stage operates to limit all signals and provide a constant amplitude output. The common emitters of transistors Q3 and Q4 are connected to ground through resistor R8. The voltage divider consisting of resistors R6 and R7 bias the center tap of the secondary of transformer T2 and the output is transformer coupled by transformer T3 to the phase detector and is also fed from the collector of transistor Q3 to the phase-shift network. The center tap of the primary of trans-

former T3 is biased through resistor R9 by −12 vdc. Tip jack TP1 is a monitoring point for viewing or measuring the filtered frequency shift keyed tone input. Resistor R10 forms part of a voltage divider with resistor R101 in the phase shift network.

(4) The phase-shift network consists of inductor L101, resistor R101 and R102, and capacitors C101 and C102. Dc bias for the phase-shift network is provided through the voltage divider consisting of resistor R1 and R2. Capacitor C2 is an ac bypass. The phase-shift network is tuned to the center frequency and, therefore, when an ac voltage of the same frequency is impressed across the circuits, a 90 degree phase shift occurs in the output voltage. However, when a higher frequency ac signal is impresssed across the circuit, the phase shift is reduced below 90 degrees to a value depending on the frequency of the input signal and the values of capacitors C101 and C102, and inductor L101. *For example,* if the center frequency was 80 kHz, inductor L101 was 10 henries, capacitors C101 and C102 in parallel were 4 microfarads, and resitor R102 in parallel with the coil resistance was 1000 ohms, a frequency of 80.5 kHz would cause a 1 degree phase shift less than 90 degrees, and conversely, with 79.5 kHz frequency the phase shift would be 91 degrees. Therefore, with a mark frequency above center frequency, the phase shift is less than 90 degrees.

(5) The limiter consists of an emitter-follower isolation stage and a limiter stage. Transistor Q5 is an emitter-follower which isolates the shifted signal and feeds it to limiter transistor Q6. The output of transistor Q5 is taken across emitter resistor R11. Resistor R12 is the emitter resistor for transistor Q6; capacitor C3 is an ac bypass. The output of limiter Q6 is applied to the phase detector.

(6) The phase detector is arranged so that when the input from the limiter is 90 degrees out of phase with the input from the push-pull amplifier-limiter, the voltage across resistor R17 and R18 is zero vdc. If the phase difference is greater than or less than 90 degrees, the phase detector produces either a positive or negative dc voltage for the mark or space condition. The direction and amplitude of this voltage depends on the phase and time duration of the input voltage. The phase-shifted input signal is applied to the primary winding of transformer T4. The signal from the amplifier-limiter is coupled to the center tap of the transformer T4 secondary windings and the junction of output detector resistors R17 and R18. Diodes CR1 through CR4 detect the relative polarity of the two signals. The output signal is then applied to the trigger circuit.

(7) The trigger circuit is composed of sense switch S1, low pass filter consisting of inductor L1 and capacitor C103, impedance converter transistor Q7, a Schmitt trigger consisting of transistors Q8 and Q9, and phase inverter transistor Q10. The trigger shapes the phase detector output waveform into a square wave. Straps A, B, and C are made when the converter is used for nondiversity. The input from the phase detector is applied to sense switch S1, which allows for selection of direct and inverted sense keying. The output of the sense switch is applied through the post-detection low pass filter consisting of inductor L1, resitors R104 and R21, and capacitor C103, to the base of impedance converter transistor Q7. Bias voltage for the circuit is developed across potentiometer R20 and resistor R19. Bias potentiometer R20 determines the weight of the normalized output of the circuit. Capacitor C7 is an ac bypass. Resistor R22 is the emitter resistor for transistor Q7. The output of transistor Q7 is applied to Schmitt trigger transistors Q8 and Q9. Tip jack TP3 provides for monitoring the phase detector output.

(8) Schmitt trigger transistors Q8 and Q9 shape the input waveform and produces a square wave output. The input to the trigger is coupled to the base of transistor Q8 by coupling resistor R23. Diode CR5 provides temperature compensation for transistor Q8. Transistor Q8 is normally cut off with no signal applied and is turned on when a negative signal is applied to the base. Turn-on is rapid and causes transistor Q9, which is normally saturated, to cutoff producing a square wave output having short risetimes and fall times. Resistors R27 and R24 are the collector and emitter bias resistors, respectively, for transistor Q8. The low level output of the trigger is taken at the emitter of transistor Q9, and applied out of the converter as well as to phase inverter transistor Q10, and the AND gate. This output may be monitored at tip jack TP2 for the auxiliary converter. Protective resistor R49 is in series with the output. The square wave from transistor Q9 is coupled to the base of inverter transistor Q10 by resistor R28. The inverted square wave output at the collector of transistor Q10 is applied to the delay amplifier. Resistor R29 is the collector bias resistor for transistor Q10. The emitter of transistor C10 is kept slightly below ground by diodes CR6 and CR7. The remainder of the −12 vdc bias is dropped across resistor R30.

(9) The delay amplifier provides a time delay of the binary signal from the trigger circuit and feeds this delayed signal to the AND gate. The delay amplifier consists basically of transistor Q11, Q12, and Q13. Transistor Q11 and Q12 form a one-shot multivibrator circuit with transistor Q11 normally in cutoff condition and transistor Q12 normally saturated. The binary signal from the trigger circuit is applied through differentiating circuits comprised of capacitor C8 and resistor R31,

capacitor C11 and resistor R37, and diodes CR18 and CR11 to the base of transistors Q11 and Q12. The diodes direct the differentiated pulses to the transistor bases. This causes transistor Q11 to saturate and transistor Q12 to cut off. After a time delay determined by the RC time constant of the circuit containing capacitor C13, resistor R39, transistor Q11, resistor R40 and diode CR9, the multivibrator returns to its initial state. In this manner, the binary pulse may be delayed for an amount of time equivalent to the time constant of the one-shot multivibrator.

(10) DELAY potentiometer R40 allows adjustment of the time constant and consequently the delay time. At the instant that the one-shot multivibrator returns to its initial state, transistor Q13 conducts and provides a fast changing time for capacitor C13. The fast-coupline network consisting of resistor R35 and capacitor C9 provides feedback coupling. Resitors R34, R35, and R36 are collector bias resistors for transistors Q12, A11, and Q13, respectively. The inputs to transistors Q11 and Q12 are taken across load resistors R32 and R38, respectively. Diode CR10 protects transistor Q12 against excessive base-emitter bias. Capacitors C9 and C10 are ac bypass capacitors.

(11) The AND gate and transistor switch drive the converter polar relay in accordance with the input binary date from the delay amplifier and the trigger circuit. The binary signal from the delay amplifier is fed through differentiating circuits comprised of capacitor C14 and resistor R42, capacitor C15 and resistor R41 to diodes CR13 and CR14 which comprise an AND gate. In order for a pulse to pass through a diode, the anode of that diode must be biased at approximately zero vdc. The anode of diode CR13 is biased through resistor R42 by the low level output signal from the trigger circuit. The anode of diode CR14 is biased through resistor R41 by the binary output of the trigger circuit. These two signals are complementary; that is, one is the inverse of the other. Therefore, when diode CR13 is biased at zero dc, diode CR14 is at −12 vdc and vice versa. Consequently, the diodes will swtich on and off alternately and the pulses from the delay amplifier will pass through one diode and then the next.

(12) These pulses from the delay amplifier are applied to the bases of transistors Q14 and Q15 across load resistors R43 and R46, respectively. The emitters of both transistors are grounded through forward biased diodes CR6 and CR7 and the collectors are biased at −12 vdc. The pulses from the delay amplifier alternately base bias the transistors, causing them to turn on and off to effectively track the mark and space data received at the input to the converter. Resistors R44 and R45 in the feedback loop stabilize the status of the transistors between changes in input mark or space signals. When a transistor saturates due to receiving an input pulse, its collector goes to ground potential. When the transistor is cut off, its collector potential is −12 vdc. If the input pulse is applied to transistor Q14, a ground return is applied to pin D of polar relay K1 causing it to energize in the direction producing a mark output. If the input pulse is applied to transistor Q15, a ground return is applied to pin A of polar relay K1 causing it to energize in the direction producing a space output.

(13) In this manner, the transistor switch drives the polar relay to produce the required output. Resistors R47 and R48 couple the transistor switch outputs from transistors Q15 and Q14, respectively, to polar relay K1. Resistors R54 and R55 are bias resistors for the relay coils. Capacitors C16 and C17 are ac bypass capacitors. Diodes CR15 and CR16 suppress the inductive voltage spikes generated by the relay windings.

(14) Polar relay K1 is a bistable electrically polarized relay which receives switching signals from the transistor switch and produces the required output to the telegraph loop. When the transistor switch is in the space condition, transistor Q15 is saturated and current flows through pin A of the relay to resistor R55 and the −12 vdc source, causing the relay to close in the space position. When the transistor switch is in the mark condition, transistor Q14 saturates and the relay assumes the mark position. Capacitors C18 and C19 and resistors R50 and R51 provide spark suppression for the relay contacts. The external loop battery is applied through pins 9 and 20 to the mark and space contacts of polar relay K1. The tongue of the relay is brought out through pin 7 for connection to an external loop. Tip jack TP4 provides a high impedance monitoring point for the high level output. The auxiliary low level output is made available for driving an auxiliary output circuit if required.

(15) The power supply operates off −28 vdc and produces −12 vdc for use in the converter. Fuse F1 protects the line power circuit. Zener diode CR17 provides voltage regulation and capacitor C20 filters the −12 vdc applied to the converter.

c. The echo suppressor transmitter is illustrated in figures 3-85 and 3-86 and is used to reduce annoying effects of echoes and outlined in (1) through (10) below:

(1) Voice frequency signals from the talker enter on connector pins B and D and pass through transformer T1 to the echo switch (transistors Q1 and Q2). With this switch closed (transistors Q1 and Q2 conducting), the vf signals pass through transformer T2 to the vf amplifier (transistors Q3 and Q4), through impedance matching transformer T3,

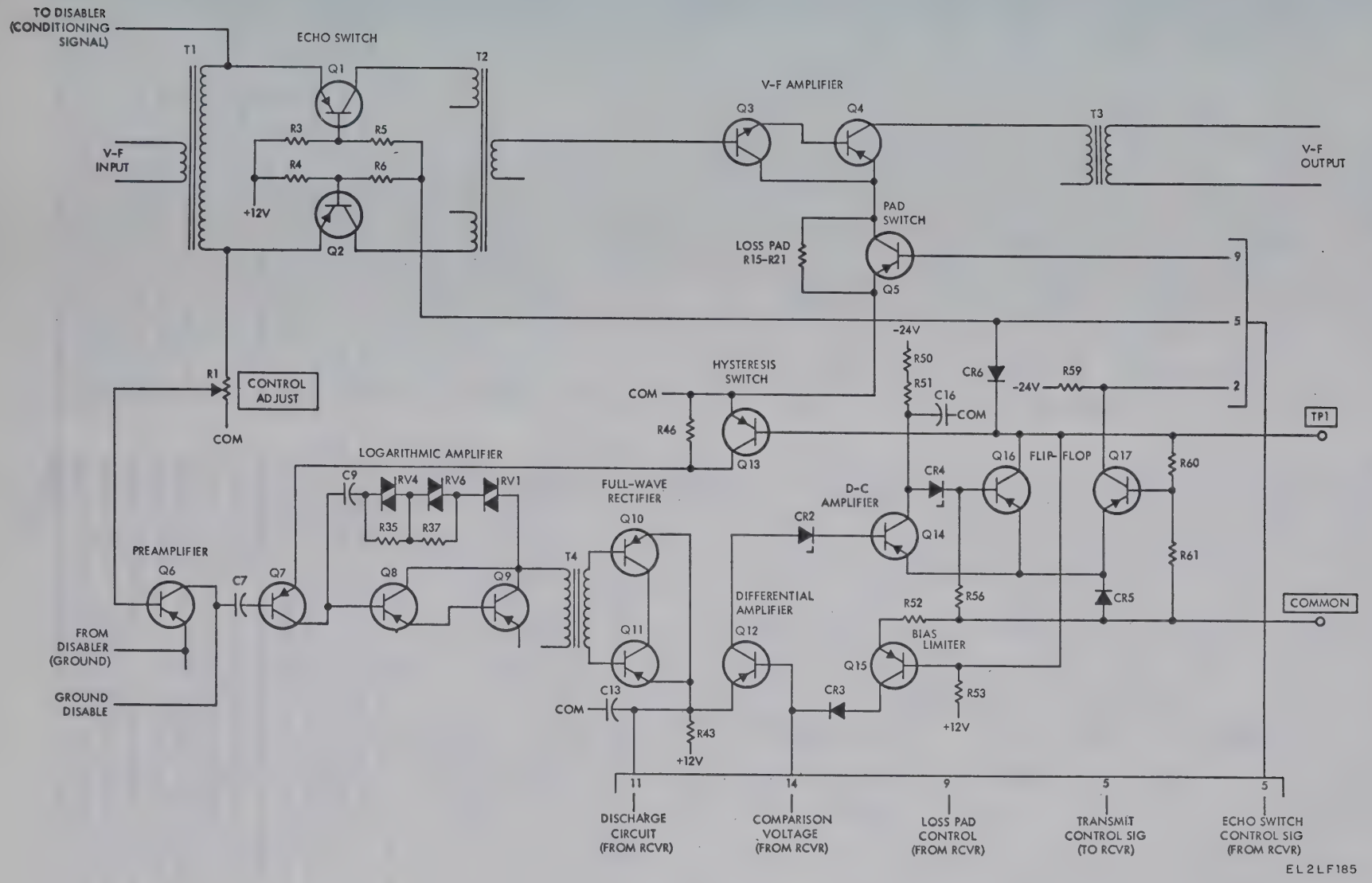


Figure 3-85. Echo suppressor transmitter, simplified schematic diagram.

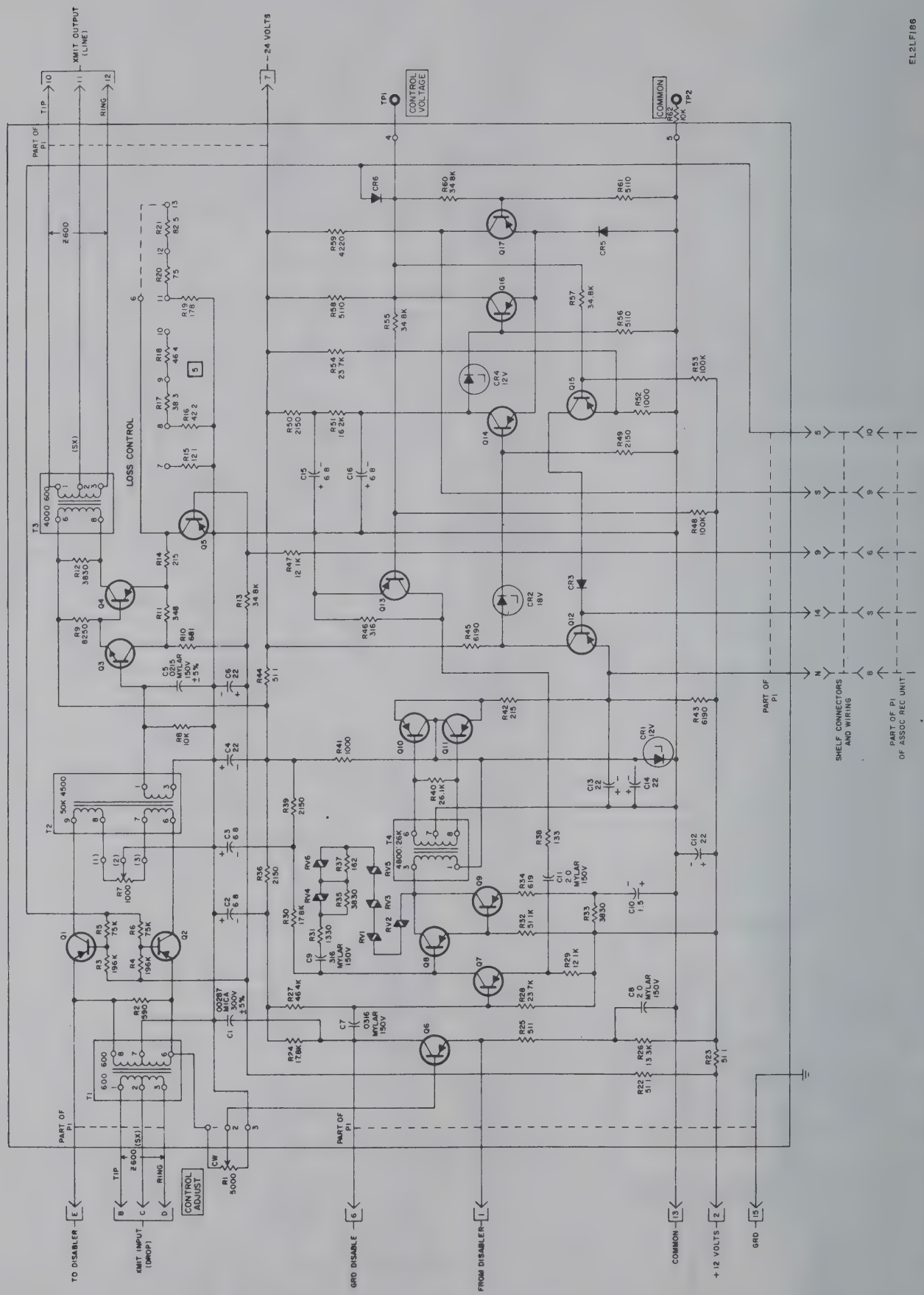


Figure 3-86. Echo suppressor transmitter, schematic diagram.

and transmitter output pins 10 and 12 to the line. Connector pins C and 11 provide simplex lead connections if dc bypassing of the unit is required. Resistor R7 is factory-adjusted to balance the primary winding of transformer T2 for suppressing clicks from switch transistors Q1 and Q2. Resistor R2 provides a 600-ohm termination for the drop transmit leg.

(2) A portion of the incoming vf signal is tapped from terminal 6 of transformer T1, through the CONTROL ADJUST potentiometer R1, and connected to preamplifier transistor Q6. This amplified control signal, under control of potentiometer R1, is connected through capacitor C7 to the logarithmic amplifier consisting of transistors Q7, Q8, and Q9 and transformers T4. Varistors RV1 through RV6, resistors R35, R37, R31 and capacitor C9 provide the feedback to attain logarithmic amplification. The control signal is then rectified by full-wave rectifier transistors Q10 and Q11 and applied to the emitter of transistor Q12, turning it off. Transistor Q12 is a differential amplifier that compares the levels of the transmit control signal and the receive control signal from an associated receiver unit.

(3) The control voltage from the receiver unit enters the transmitter on connector pin 14 and connects to the base of transistor Q12. With no input signal to the transmitter, transistors Q10 and Q11 will be in a nonconducting state and transistor Q12 will be switched on by the +12 vdc applied to the emitter through resistor R43. When transistor Q12 is switched off by the rectified control signal, the voltage applied to breakdown diode CR2 increases towards −24 vdc. This is adequate to overcome the 18-volt breakdown characteristic of the diode and will apply a negative potential to the base of dc amplifier transistor Q14, switching it on. Transistor Q14 drives flip-flop circuit transistors Q16 and Q17, which, along with the receiver unit control circuit, controls the echo switch (transistor Q1 and Q2) and the pad switch (transistor Q5).

(4) With no incoming signal, transistor Q14 will be cut off. Breakdown diode CR4 will then break down due to −24 vdc through resistors R50 and R51. The drop across resistor R56 applies a negative voltage to the base of transistor Q16, switching it on. Emitters of transistors Q14, Q16, and Q17 are held at −0.7 vdc by the drop-through diode CR5. When transistor Q16 is switch on, its collector voltage (and test point TP1 voltage) is −0.7 vdc. This is insufficient to turn transistors Q1 and Q2 on, thus the vf path is effectively opened. The collector of transistor Q17 is connected to the receiver unit through connector pin S. Circuitry in the receiver unit and resistor R59 will result in the application of —15 vdc on the collector of transistor Q17 while it is cut off. Transistor Q17, along with the control circuit in the receiver unit, controls the pad switches in both units and the hysteresis switch in the receiver unit.

(5) With an incoming signal, transistor Q14 is switch on. This removes the negative voltage on the base of transistor Q16, cutting it off. The collector of transistor Q16 (and TP1) will now change from −0.7 vdc to −15 vdc. This, in turn, is applied through diode CR6 to resistors R5 and R6 of the echo switch. The voltage drop across resistors R3 and R4 will provide a negative potential on the bases of transistors Q1 and Q2, switching them on, and thereby allowing the incoming vf signals to be transmitted even if the corresponding flip-flop in the receiver unit had them turned off. The −15 vdc at the collector of transistor Q16 and tip jack TP1 is also divided by resistors R60 and R61 to provide a negative voltage on the base of transistor Q17, switching it on. This changes the voltage on the collector of transistor Q17 from −15 vdc to 0.7 vdc, which again, controls the hysteresis switch in the receiver unit. The transmitter control circuit is now in a "set" condition.

(6) When the vf signal ceases, the transmitter control circuit will return to its original "reset" condition. Resistor R51 and capacitor C16 provide a 75 to 120 millisecond delay in the change from "set" to "reset" (turn-on of transistor Q16) to prevent switching between syllables.

(7) Transistor Q13 functions as a transmitter hysteresis switch to change the gain of transistor Q7. Resistor R46 in the emitter circuit of transistor Q7 decreases the gain of the logarithmic amplifier (transistors Q7, Q8, and Q9). With an incoming signal to the transmitter, the control circuit changes to a "set" condition putting −15 vdc on tip jack TP1. Part of this negative voltage is applied to the base of transistor Q13, turning it on. This shorts out resistor R46 to increase the gain of transistor Q7 by 5 dB. The purpose of the hysteresis switch transistor Q7 is to require a firm input signal to put the transmitter control circuit into a "set" condition, and to allow a lower level signal to hold it in the "set" condition.

(8) Transistor Q15 functions as a bias limiter to transistor Q12. With the transmitter in a "reset" condition, transistor Q15 will be cut off by the +12 vdc applied through transistor R53. The voltage on the base of transistor Q12 will then vary exactly as the rectified control voltage varies in the receiver unit. With this condition, the transmitter cannot be "set" unless the talker produces a speech level higher than that being received and thereby cutting off transistor Q12. Once the transmitter control circuit is "set", −15 vdc applied from transistor Q16 will turn transistor Q15 on and connect the base of transistor Q12 to common through capacitor CR3 and resistor R52, decreasing the ef-

fect of the receive signal on transistor Q12.

(9) Pad switch transistor Q5, functions to decrease the gain of the transmit amplifier (transistors Q3 and Q4) when the receive control circuit and transmitter control circuit are both in a "set" condition. The amount of gain decrease is attained by strapping options that use various combinations of resistors R15 through R21. From 0 dB to 6 dB of pad, in 1-dB steps, is provided.

(10) Transistor Q5 is controlled by the receiver unit control circuit through the lead from connector pin 9 of the transmit unit. With the receiver unit in a "reset" condition (no receive signal), or with the transmitter to a "reset" condition (no input to the transmitter), a negative potential on this lead from the receiver unit will bias transistor Q5 to conduction, shunting out the pad resistors. Connector pins 1 and E provide control connections to a separate disabler unit. Pin 6 can be used for either external enabling control or external disabling control.

d. The echo suppressor disable (fig. 3-87) inhibits the suppression function of the transmitter and receiver echo suppresssors, on command of an external tone signal, to allow for transmission of telegraph or data signals to the voice channel:

(1) Disabling of an echo suppressor is initially accomplished by the continuous and exclusive transmission of energy in a narrow conditioning band (2000-2250 Hz) for a period from 0.3 to 0.45 second. Unilateral disabling control (disabling upon detection of a conditioning signal from either the transmit or the receive side of voice path) is employed whenever suspension of echo suppressor operation in a voice channel is desired. Once executed, disabling may be continued by supplying energy (that is, data signals) anywhere in the useful voice band, provided signal absence does not exceed the release time (0.125 second, approximately). This broadband holding characteristic allows data systems to initiate and maintain disabling provided that the proper conditioning signal precedes the normal data.

(2) Initial and continued disabling action is provided by the operate and the hold circuits of the disabler, respectively. Normal echo suppressor operation is assured immediately after the disabling action is released (that is, after a signal absence greater than the 0.125 second release time), since the disabler has a guard circuit which opposes disabling by utilizing energy in the voice channel outside of the narrow conditioning band.

(3) All voice frequencies used in the echo suppressors are monitored by the disabler. The voice frequencies from the transmitter and receiver echo suppressors are applied to potentiometers R1 and R2, respectively. Potentiometers R1 and R2 are used to set the threshold level of the disabler with respect to the conditioning tone. The signals at the wiper arm of potentiometers R1 and R2 are amplified by transistors Q1 and Q2, respectively. Resistors R3 and R6 are collector load resistors for transistors Q1 and Q2, respectively. Resistors R4 and R7 are swamping resistors. Emitter resistors R5 and R8 are bypassed by capacitors C1 and C4, respectively. The high frequencies at the collector of transistor Q1 are bypassed to ground by capacitor C5, while the low frequencies are coupled through capacitor C2 and resistor R9 to resistor R10. The high frequencies at the collector of transistor Q2 are bypassed to ground by capacitor C6, while the low frequencies are coupled through capacitor C3 and resistor R11 to resistor R10 where they are summed with the frequencies from transistor Q1. The summed frequencies are limited by varistor RV1.

(4) The limited signal is applied through resistor R10 to the base of transistor Q3. The dc bias for the base of transistor Q3 is supplied by a voltage divider comprised of resistors R64 and R65. Resistor R12 is the collector load for transistor Q3, resistor R13 is the swamping resistor, and resitor R14 is the emitter resistor which is bypassed by capacitor C7. Diode CR1 provides temperature compensation. The output of transistor Q3 is coupled through capacitor C8 to three different circuits: operate, guard, and hold.

(5) The operate circuit controls the disabler output when the 2125 Hz tone is received. The guard circuit controls the output of the disabler prior to receiving the conditioning tone and prevents inhibiting the echo suppressors during this time. The hold circuit controls the disabler output after the conditioning tone is depleted and as long as continuous data is transmitted.

(6) During the guard condition, the negative voltage at the collector of turned off transistor Q13 is applied across resistors R15 and R17. The negative voltage at the junction of resistors R15 and R17 forward biases operate transistor Q4 and guard transistor Q5 and reverse biases hold transistor Q6. This is basically a safeguard voltage which prevents wideband signals from disabling the suppressors through the action of the hold circuits. The input to the guard circuit is applied through resistors R18 and R22 to the base of transistor Q5. Inductor L2 and capacitor C11 form a series resonant circuit which provides a low impedance path to ground for the frequencies near 2145 Hz. Capacitor C13 bypasses to ground the high frequencies at the base of transistor Q5. Resistor R30 is the collector load, resistor R28 is the swamping resistor, and resistor R29 is the emitter resistor which is bypassed by capacitor C15.

(7) The signal at the collector of transistor Q5 is applied through resistor R31 to the base of tran-

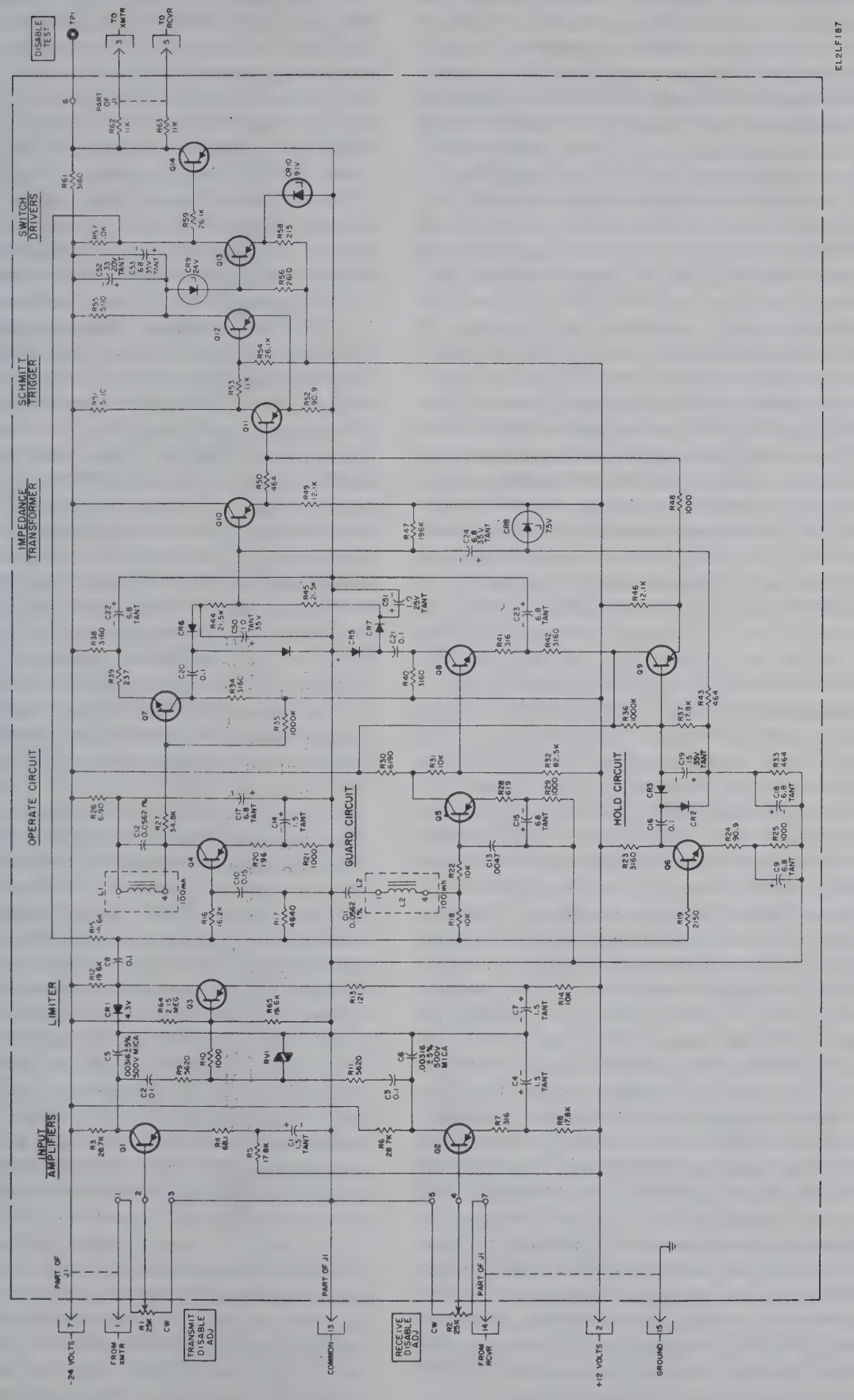


Figure 3-87. Echo suppressor disabler, schematic diagram.

sistor Q8. Transistor Q8 is biased by the voltage divider comprised of resistors R30, R31, and R32. Resistor R42 is the emitter resistor which is bypassed by capacitor C23. The output of transistor Q8 is coupled through capacitor C21 to a half wave rectifier circuit comprised of diodes CR5 and CR7. The positive half cycle forward biases diode CR7 and charges capacitor C51. The negative half cycle forward biases diode CR5 and is shorted to ground. The positive voltage across capacitor C51 is applied through resistor R45 to the base of emitter-follower transistor Q10. This positive voltage causes the emitter to go positive and the positive emitter voltage is applied through resistor R50 to the base of transistor Q4. The base of emitter-follower transistor Q10 is biased by resistor R47 and capacitor C24. A +7.5 vdc reference voltage for capacitor C24 is supplied by breakdown diode CR8. Resistor R47 is returned to +12 vdc.

(8) Transistors Q11 and Q12 and associated circuit components form a Schmitt trigger circuit. Resistor R51 is the collector load for transistor Q11. Resistor R52 is the common emitter resistor and resistors R53 and R54 form the between-stage coupling and base biasing network for transistor Q12. Resistor R55 is the collector load and capacitors C52 and C53 bypass resistor R55. The positive voltage at the base of transistor Q11 cuts off transistor Q11 and turns on transistor Q12. The positive-going collector of transistor Q12 causes the voltage across breakdown diode CR9 to fall below the 24 volt breakdown level. This allows the base of switch driver transistor Q13 to go positive, cutting off transistor Q13. Base biasing resistor R56 is connected to a +12 vdc source and supplies the positive base voltage. Resistor R58 is the emitter resistor and resistor R57 is the collector load. Breakdown diode CR10 supplies an emitter reference level of −9.1 vdc. When transistor Q13 is cut off, the collector goes negative and this negative voltage is applied through coupling resistor R59 to the base of switch driver transistor Q14, turning on Q14. The collector of transistor Q14 goes to near ground and this ground is applied through resistors R62 and R63 to the echo suppressors. This allows the echo suppressors to function normally. Resistor R61 is the collector load for transistor Q14.

(9)During the operate condition, the 2125 Hz conditioning tone is applied through resistor R16 to the base of transistor Q4. Capacitor C10 provides a low impedance path to ground for high frequencies. Resistor R26 is the collector load, resistor R20 is the swamping resistor, and resistor R21 is the emitter resistor which is bypassed by capacitor C14. Inductor L1 and capacitor C12 form a parallel resonant tank circuit which is resonant at 2125 Hz. Capacitor C17 is a decoupling capacitor.

(10) Amplifier transistor Q4 only responds to the 2125 Hz conditioning tone due to the tank circuit. The 2125 Hz signal at the collector is applied through resistor R27 to the base of transistor Q7. Resistor R35 provides the positive forward bias voltage to the base of transistor Q7. Resistor R34 is the collector load, resistor R39 is the swamping resistor, and resistor R38 is the emitter resistor which is bypassed by capacitor C22. The amplified tone at the collector is coupled through capacitor C20 to a half-wave rectifier circuit comprised of diodes CR4 and CR6. The positive half cycle of the tone is shorted to ground by diode CR4 and the negative half cycle forward biases diode CR6 and is filtered by capacitor C50 and resistor R44.

(11) The resultant negative voltage overrides the positive guard voltage and capacitor C24 discharges through resistor R47. The combined negative voltages across resistors R44 and R47 cause the emitter to go negative. This negative voltage triggers the Schmitt trigger circuit (transistors Q11 and Q12) and the collector of transistor Q12 goes negative. The negative output of transistor Q12 turns on switch driver transistor Q13 which, in turn, cuts off switch driver transistor Q14. The collector of cutoff transistor Q14 goes to approximately −15.5 vdc. This negative voltage is applied to the echo suppressors to inhibit the suppressors. When transistor Q13 is turned on, the collector goes positive and this positive voltage is applied through resistor R15 to the bases of transistors Q4, Q5, and Q6. This action biases operate and guard transistors Q4 and Q5 and turns on hold transistor Q6.

(12) The hold circuit is essentially a wideband circuit which receives the data transmission signal. The data transmission (wideband) signal is applied through resistor R19 to the base of transistor Q6. Resistor R23 is the collector load, resistor R24 is the swamping resistor, and resistor R25 is the emitter resistor which is bypassed by capacitor C9. The amplified wideband signal at the collector of transistor Q6 is coupled through capacitor C16 to a half wave rectifier circuit comprised of diodes CR2 and CR3. The cathode of diode CR2 has a positive reverse bias reference voltage applied from breakdown diode CR8 which is filtered by capacitor C18 and resistors R33 and R43. When the positive half cycle of the wideband data signal exceeds the reference level, it is shorted to the reference level and is filtered out. The negative half cycle forward biases diode and is filtered by capacitor C19, developing a negative voltage at the base of emitter-follower transistor Q9. This negative voltage turns on transistor Q9. Resistors R36 and R37 provide the dc bias for the base of transistor Q9. Resistor R46 is the emitter resistor.

(13) If the wideband signal is interrupted, the discharge of capacitor C19 will maintain transistor

Q9 turned on for 0.125 second. The negative emitter voltage is applied through resistor R48 to the base of Schmitt trigger transistor Q11. This negative voltage assumes control of transistor Q11 from the output of the operate circuit and maintains switch driver transistor Q14 turned off, provided that the data transmission is continuous. When the data transmission is terminated for longer than the hold circuit release time (0.125 second), the Schmitt trigger switches states and switch driver transistor Q13 is cut off. The resulting negative collector voltage turns on transistor Q14 which enables the echo suppressors. The negative collector voltage is also applied to the inputs of the operate, guard, and hold circuits. This negative voltage enables the operate and guard circuits and disables the hold circuit. At this time the output of the guard circuit assumes control of the disabler output.

e. The echo suppressor receiver (fig. 3-88 and 3-89) is used to reduce annoying echo effects as outlined in (1) through (12) below:

(1) Incoming vf signals are applied to the receiver unit at connector pins 3 and 5 and to the primary winding of transformer T2. The signal from the secondary of transformer T2, is applied through amplifier transistors Q12 and Q13 and transformer T3 to connector pins 12 and 14. Pins 4 and 11 provide simplex leads to the line and the "drop" if dc bypassing of the unit is required.

(2) A portion of the incoming vf signal is tapped from terminal 8 of transformer T2 and applied through resistor R36 and CONTROL ADJUST potentiometer R1, to the logarithmic amplifier transistor Q1, Q2, and Q3 and transformer T1. Varistors RV1 through RV6, resistors R3, R4, R5 and capacitor C1 provide the feedback to attain logarithmic amplification. This control signal is then rectified by full-wave rectifier transistor Q4 and Q5 and applied to the emitter of transistor Q8.

(3) Transistor Q8 is a differential amplifier that compares the level of the received control signal to the temperature-compensated base bias developed across resistor R22, diode CR5, and thermistor RT1. With an adequate receive signal, transistor Q8 will be cut off by the negative voltage from transistors Q4 and Q5. This increases the voltage applied to breakdown diode CR6 which overcomes the breakdown characteristic of the diode and applies a negative voltage to the base of dc amplifier transistor Q11.

(4) Transistor Q11 drives the flip-flop circuit comprised of transistors Q9 and Q10, which along with the transmitter unit control circuit, controls pad switch transistor Q14 of the receiver and the echo switch in the transmitting unit. With no receive signal, transistor Q11 will be cut off. Breakdown diode CR11 will then break down due to the −24 vdc applied through resistor R34. The voltage drop across resistor R33 applies a negative voltage to the base of transistor Q10. There is a slight delay before transistor Q10 will conduct after the incoming signal ceases. This delay is provided by resistor R34 and capacitor C9 to hold the transmitter unit echo switch open for a time period exceeding "drop" delay.

(5) If "drop" delay is longer than 25 milliseconds round trip, capacitor C9 should be proportionately increased. When transistor Q10 is conducting, its collector voltage (and test point TP1) becomes applied to the base of transistor Q9, cutting it off. This is called the "reset" condition of the receive control circuit. In this condition, −15 vdc from the collector of transistor Q9, is applied through diode CR9 and connector pin 10 to the echo switch in the transmitter unit. This will close the echo switch and condition the transmitter unit to accept speech without clipping. The negative voltage applied to the base of amplifier transistor Q11, due to a receive signal, will cause transistor Q11 to conduct. This removes the negative bias from the base of transistor Q10 by reducing the voltage at the junction of resistor R34 and diode CR11 to common value. Transistor Q10 will then be cut off and its collector voltage (and TP1) will change from −0.7 to −15 vdc.

(6) With transistor Q10 cutoff, the voltage drop across resistor R29 will provide a negative voltage to the base of transistor Q9. The collector of transistor Q9 will then change from — 15 to —0.7 vdc. This is called the "set" condition of the receive control circuit. The −15 vdc that previously closed the echo switch in the transmitter unit ((5) above) will now be removed, placing the echo switch under control of the transmitter unit control circuits only. Transistor Q7 functions as a hysteresis switch to change the gain of the logarithmic amplifier (transistors Q1, Q2, and Q3). Resistor R15, in the emitter circuit of transistor Q1, decreases the gain of the amplifier by 9 dB.

(7) With a receive signal, and no transmit signal, the −15 vdc from the transmitter unit control circuit (through resistor R26), and the −15 vdc from the receive control circuit (through resistor R27), will provide a negative voltage to the base of transistor Q7 by the voltage drop across resistor R30. This turns transistor Q7 on, which, in effect, shunts resistor R15, to increase the logarithmic amplifier gain. If the transmitter unit control circuit is "set" or if the receive control circuit is "reset", the voltage drop across resistor R30 will be less than that required to turn transistor Q7 on. The purpose of the hysteresis switch (transistor Q7) is to require a firm input signal to put the receive control circuit in a "set" condition, and allow a lower level signal to hold it in the "set"

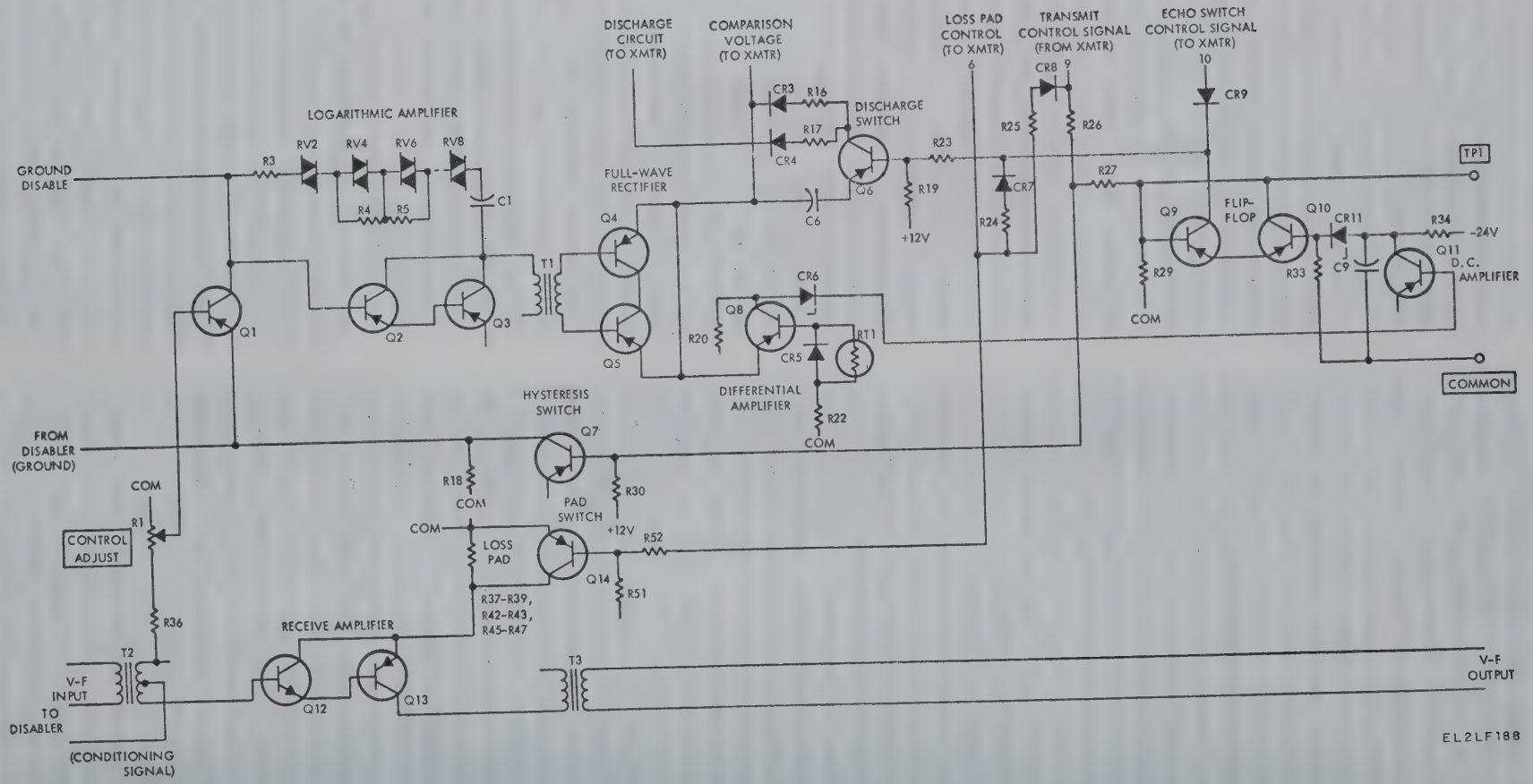


Figure 3-88. Echo suppressor receiver, simplified schematic diagram.

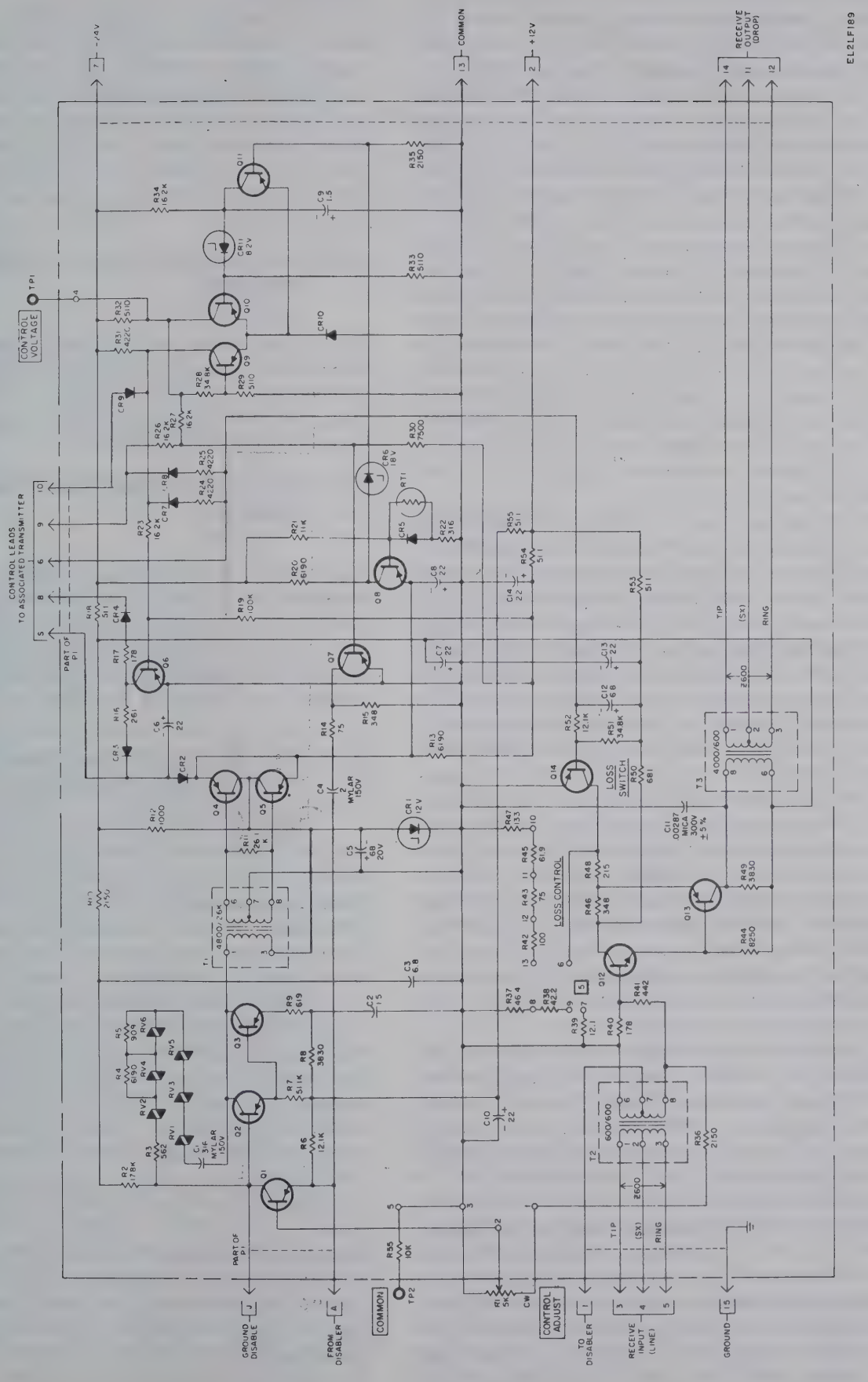


Figure 3-89. Echo suppressor receiver, schematic diagram.

condition so that switching between words and syllables is minimized.

(8) Pad switch transistor Q14 functions to decrease the gain of the receive amplifier (transistors Q12 and Q13) when the receive control circuit and the transmitter unit control circuit are both in a "set" condition. The amount of gain decrease is attained by strapping options that are various combinations of resistors R37, R38, R39, R42, R45 and R47. Transistor Q14 is controlled by the voltage applied to its base through resistor R52 and dropped across resistor R51. This voltage is determined by the receive control circuit (from the collector of transistor Q9 through diode CR7 and resistor R24) and from the transmitter unit control circuit (receiver connector pin 9, through diode CR8 and resistor R25). With either the transmitter unit control circuit "reset" or the receive control circuit "reset", −15 vdc will be applied from the control circuits and transistor Q14 will conduct. This shunts the strapped-in pad resistors of the receive amplifier (transistors Q12 and Q13) and increases the gain to unity.

(9) When both control circuits (transmit and receive) change to a "set" condition (bidirectional operation), the voltage from the control circuits changes to −0.7 vdc. This turns transistor Q14 off and decreases the gain of the receive amplifier by removing the shunt across the pad resistors. Pad switch transistor Q14 and the pad switch in the transmitter unit have a common control. The transmitter unit switch is connected to the common control point through receiver unit connector pin 6.

(10) Transistor Q6 functions as a discharge path for capacitor C6 in the receiver and capacitor C13 in the transmitter unit when the receive control circuit is in a "reset" condition. These capacitors provide filtering to reduce the ripple in the output of the full-wave rectifiers in the control circuits. They also provide a small delay when, under the conditions explained in (11) below, the transmitter unit or the receiver changes from "set" to "reset" or vice versa.

(11) With the receive control circuit in a "set" condition, the +12 vdc applied through resistor R19 will cut transistor Q6 off. When the control circuit changes to a "reset" condition, −15 vdc will be applied from the collector of transistor Q9, through resistor R23, and transistor Q6 will be turned on. With transistor Q6 conducting, capacitor C6 will discharge through diode CR3, resistor R16 and transistor Q6, which will immediately remove the negative voltage from the base of the differential amplifier (transistor Q12) in the transmitter unit (connected through connector pin 8 of the receiver unit). The transmitter unit can now attain a "set" condition immediately, without having to overcome the bias on the base of transistor Q12 that would remain due to the charge on capacitor C6.

(12) The filter capacitor (C13) in the transmitter unit will be discharged through diode CR4, resistor R17 and transistor Q6 when Q6 is conducting. This prevents capacitor C13 in the transmitter unit from controlling the transmitter "reset" condition. Connector pins 1 and A provide control connections to a disabler unit. Pin J can be used for either external enabling control or external disabling control.

3-26. Line Isolation Panel 1A3A26, Circuit Analysis.

(fig. FO 3-47)

The line isolation panel consists of three identical line isolation units (ref TO 31WA-2T-102) and a ±6 vdc power supply. Refer to figures FO 3-47, FO 2-1 (sheet 2), FO 2-2 (sheet 17), FO 2-7 (sheet 6), FO 2-7 (sheet 9) and FO 2-8 (sheet 2).

3-27. Fan Control Assembly 1A3A19, Circuit Analysis

(fig. 3-90)

The fan control assembly consists of two circuit breakers and three blower motors and basically provides cooling for the communications console. Circuit breaker CB2 is used to apply power to blower motors B1, B2, and B3. Circuit breaker CB1 is used to route power through the fan control.

3-28. 2.0 Kw Static Frequency Converter 1A2A35, Circuit Analysis

(fig. 3-191, 3-92, FO 3-48 and FO 3-49)

a. The 2.0 kw static frequency converter 1A2A35 (fig. FO 3-48) converts 208 vac, 400 Hz, three-phase input power applied by 10A circuit breaker CB1 to 120 vac ±10%, 60 Hz, single-phase output power. The output power is applied to the AN/UGC-77 teletypewriter and 60 Hz convenience outlet.

b. Full-wave bridge rectifier CR1 through CR6 receives the three-phase input power through transformer TI which provides isolation and scales the input voltage. The 200 vdc rectifier output is applied to single-phase inverter CR7 through CR10 which receives switching instructions from the logic assembly A5, through driver amplifier A6 and A7.

c. The logic assembly (fig. FO 3-49) provides a sinewave synthesized signal and incorporates voltage amplitude control, using the output from a signal comparator. Voltage control is maintained by reducing the output voltage of the single-phase bridge inverter to zero for a predetermined portion of time once every 30°, or 12 times each cycle.

(1) The output of crystal oscillator-pulse

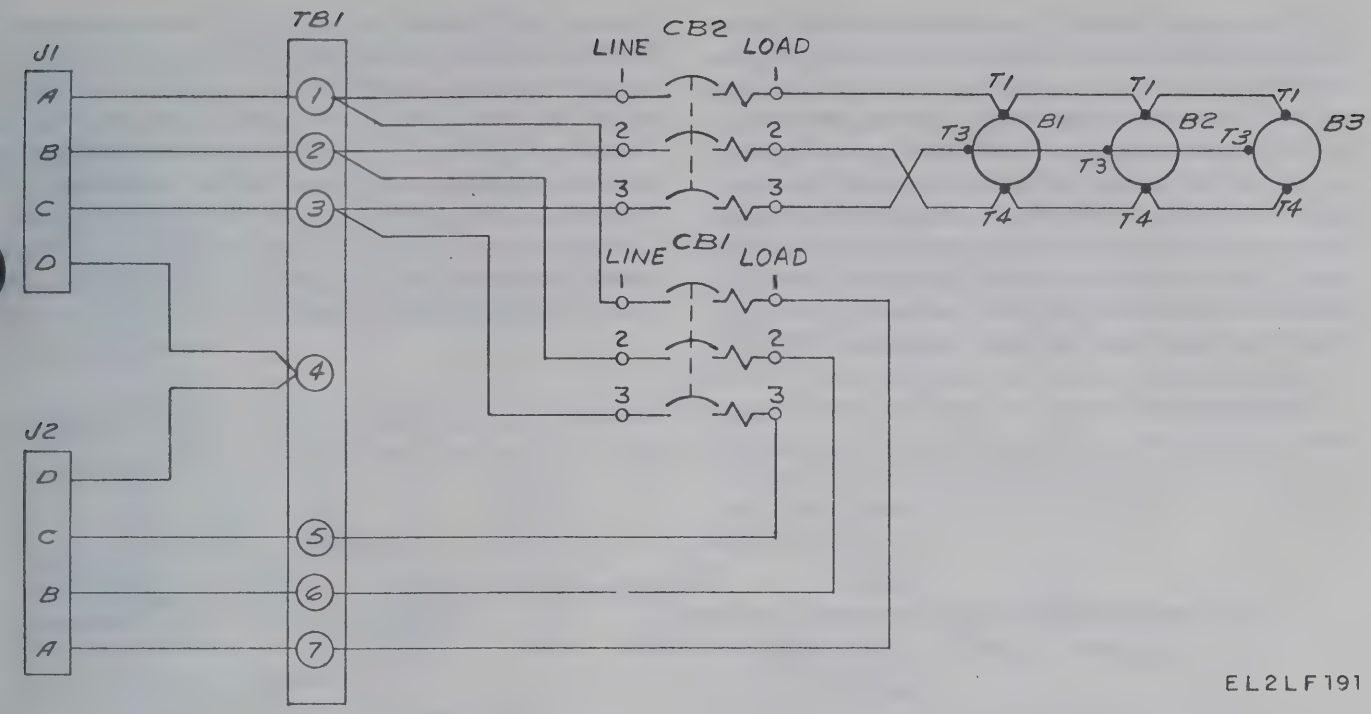


Figure 3-90. Fan control assembly 1A3A19, schematic diagram.

shaper IC7 is applied to divide-by-six and divide-by-two counter IC8 with its output TP1 a 43.2 kHz clock signal. The 43.2 kHz clock signal is applied to a divide-by-two counter (p/o IC6) its output of which clocks divide-by-fifteen counter is IC4. Pulse width information from the divide-by-fifteen counter is extracted in gate logic IC5, IC10 and IC12 to provide control switching information to six-stage Johnson Counter IC11. IC13 and IC14. In addition, IC5 clears the divide-by-fifteen counter and clocks a divide-by-two counter (p/o IC6).

(2) The six-stage Johnson Counter uses J-K flip-flops which are designated A through F to allow input correlation at phase A logic IC15 through IC18 and phase B logic IC19 through IC22. The J and K inputs to each flip-flop are enabled by the preceding one except flip-flop A, which is set enabled from IC10 and reset enabled from flip-flop F in IC14. A 720 Hz output TP3 from the divide-by-two counter clocks the Johnson Counter. After all flip-flops are set (representing six 720 Hz clock periods), reset begins at flip-flop A and continues until all flip-flops are reset (representing six additional 720 Hz clock period). Therefore, the output voltage of the single-phase inverter is reduced to zero 12 times each cycle to maintain voltage control.

(3) Phase A logic IC15 through IC18 supplies switching information to pulse gating IC36 and delay IC37 circuits which provide lower and upper (snap) signals and lower delay and upper delay (drive) signals to drive A6. The drive signal is delayed in order to prevent currents flowing through series connected power blocks A1 and A2. Phase B logic IC19 through IC22 and pulse gating IC34 and delay IC35 circuit supply similar information to driver A7 the delayed drive signal of which protects series connected power blocks A3 and A4.

(4) Signal comparator (consisting of IC9, IC31 and IC32 and transistors Q3, Q4, Q5, Q7 and Q8) output TP4 is applied to gate logic IC12, phase A logic IC15 and phase B logic IC19. Dual voltage comparator IC9 compares a voltage feedback signal J4D and E and a current feedback signal J4K and N to a precise Zener reference and provides voltage regulation unless an overload condition exists in which current regulation overrides voltage regulation. The output voltage level and current limit are factory-adjusted. When looking from the front of the drawer, the voltage adjust A5R18 is on the left and the current limit A5R19 on the right. If a further adjustment is desired for any reason, turn the appropriate potentiometer counterclockwise to achieve an increase. The feedback circuits provide constant voltage output; ±10% regulation for no load to full load change and from low input line to high input line.

(5) Precision voltage regulator IC2 and transistor Q1 provide a highly stabilized output voltage V_{cc} of +5 vdc that is used throughout the 2.0 kw static frequency converter.

(6) Current limiting is provided by dual voltage comparator IC33, transistor Q6 and overload relay K1 to protect the equipment and load against possible malfunctions.

(7) Modules IC23 through IC28 are not used.

d. Drivers A6 and A7 (fig. 3-91) amplify the drive signal from logic assembly A5 to a level sufficient to assure switching in the power block. The delayed drive signal is applied to the base of transistor Q4, amplified and applied to the base of transistor Q3 for further amplification to a level to drive the power block. Resistor R7 and diode CR3 provide a negative bias so that transistor Q4 turns off rapidly when so commanded. The collector emitter circuit of transistor Q2 provides a snap off low impedance path for the base emitter junction of transistor Q3. Simultaneously, with the removal of the drive signal to transistor Q4, a snap signal is applied through transistor Q1 to the base of transistor Q2, which conducts heavily. Conduction of transistor Q2 causes the cathode of diode CR2 to go positive, and the stored energy across capacitor C2 forces the base emitter junction of transistor Q3 to be biased off sharply. The output of driver amplifiers A6 and A7 is applied to power blocks A1 and A2, A3, and A4, respectively.

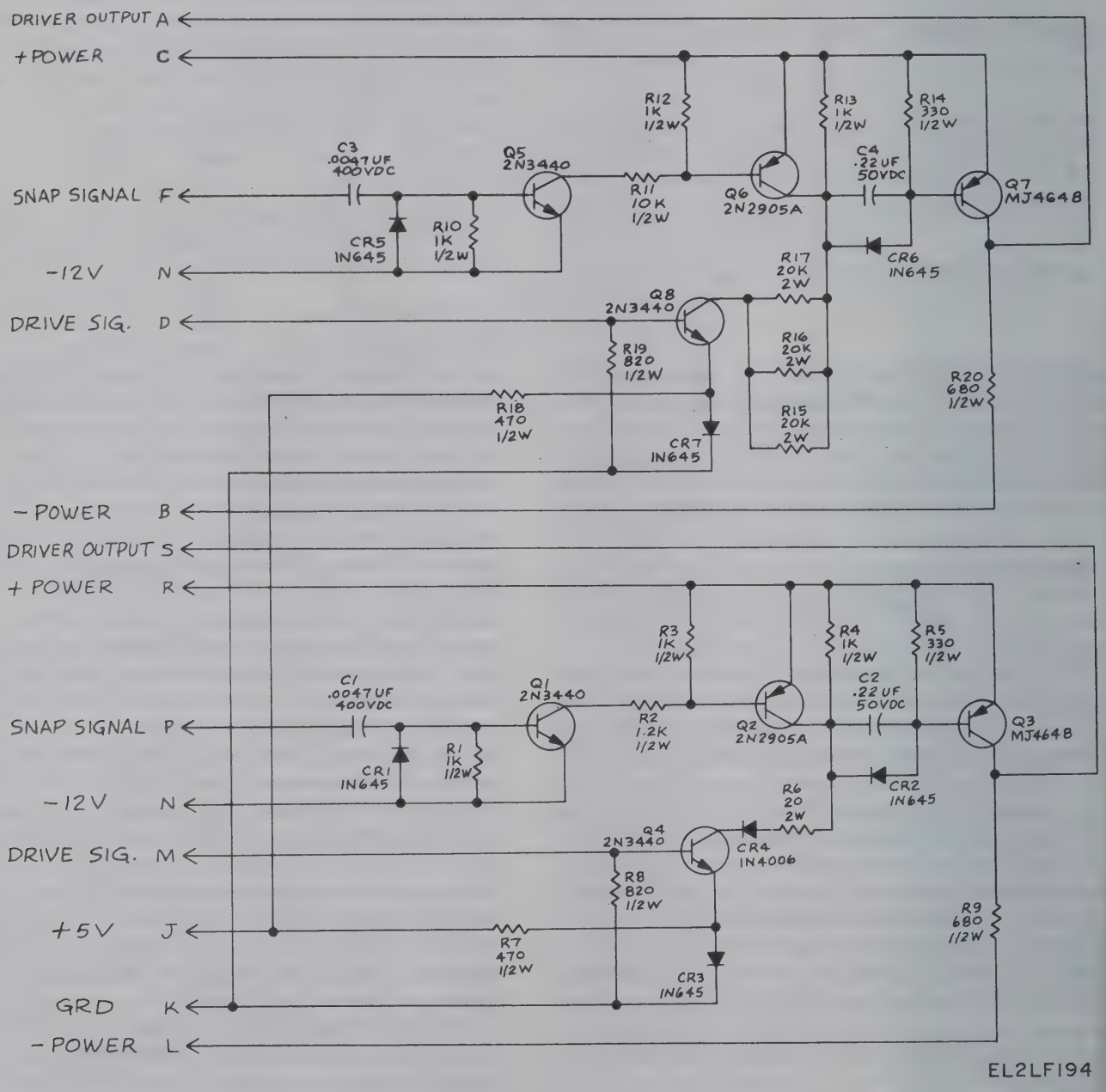


Figure 3-91. Driver amplifiers A6 and A7, schematic diagram.

e. Each power block (fig. 3-92) is a three-terminal network that conducts current in each direction. A low impedance path is provided between the collector and base of the transistor Q1, when the driver amplifier causes conduction. Transistors Q1 and Q2 form a darlington pair that conducts load current as required. Transistors Q1 and Q2 are operated in the linear portion of the collector voltage-

current characteristics to automatically adjust the current demanded from the drive amplifier because of varying load conditions. When the drive signal is removed, diode CR1 and capacitor C1 provide negative bias to the bases of transistors Q1 and Q2 to assure rapid turn off. Diode CR2 permits reactive currents to flow when the output voltage and current are out of phase. All drive current to the power block, including the current which flows in the output stage of the driver amplifier, is useful load current.

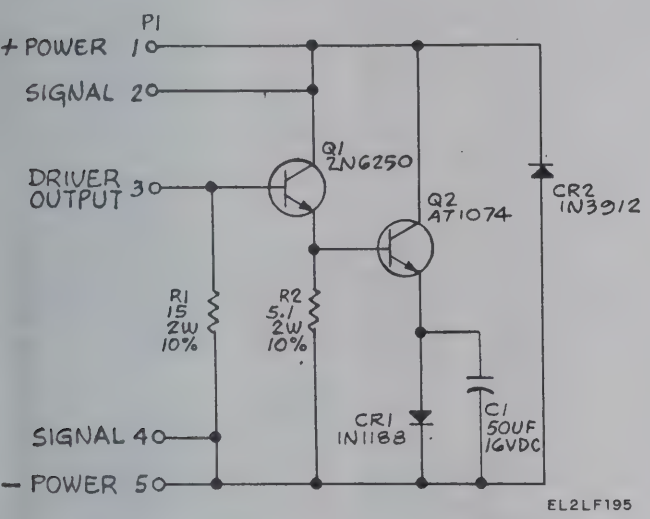


Figure 3-92. Power blocks A1, A2, A3, and A4, schematic diagram.

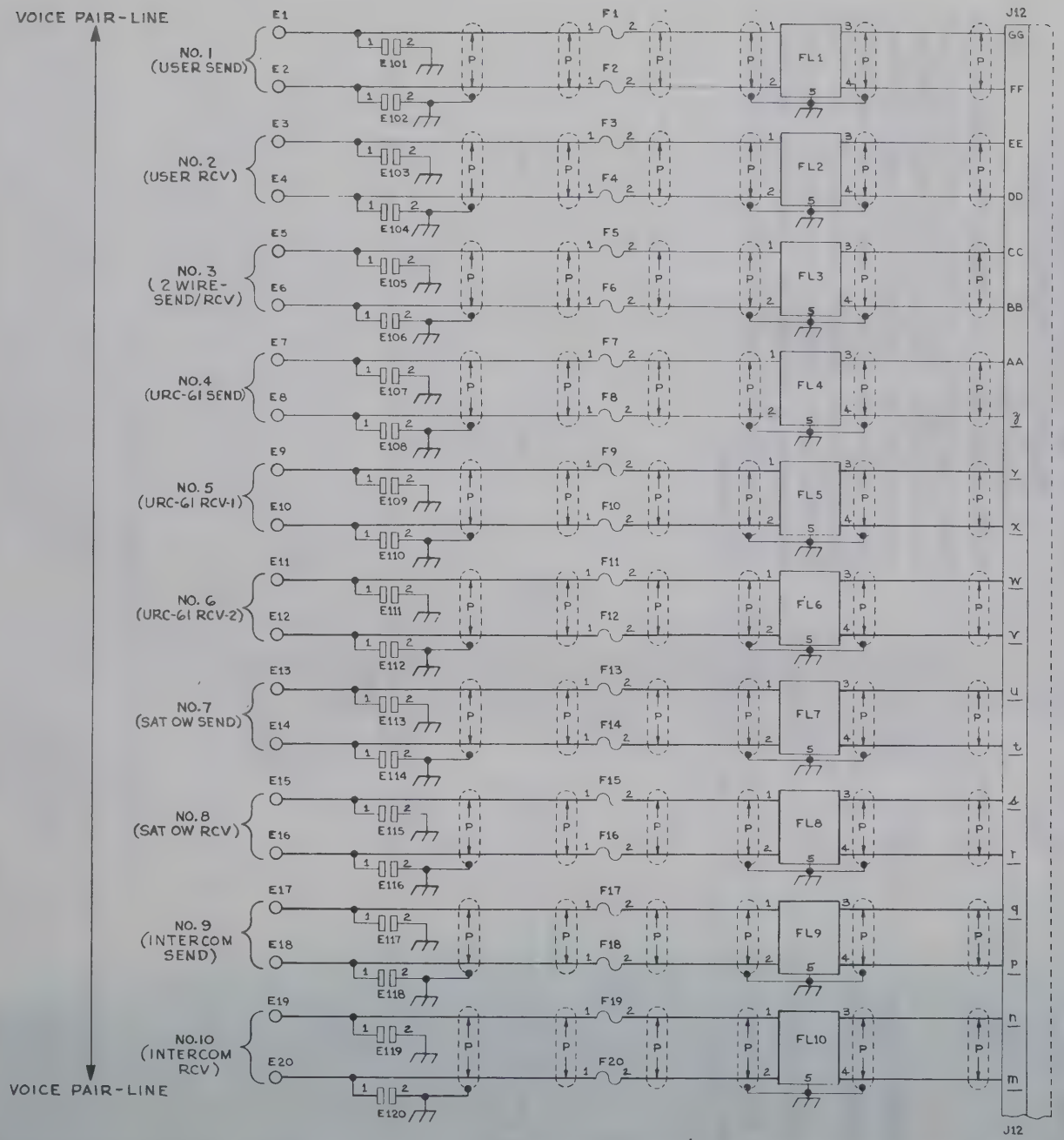
f. The 120 vac ±10%, 60 Hz, single-phase output power (fig. FO 3-48) is applied to the AN/UGC-77 teletypewriter through 10A circuit breaker CB2 and output power connector J2. Output power is also supplied to convenience outlet J3 through 10A circuit breaker CB3. The maximum load current that can be applied to either utility power or output power connector is 10A. Maximum total load current that can be drawn from the system is 17 amperes, continuous at unity power factor or 21.3A under 0.8 power factor.

g. Inrush limiter A8 (fig. 3-87) contains resistor R4 which protects the 2.0 kw static frequency converter from input surges. After a delay of approximately 200 milliseconds, relay K1 energizes to bypass resistor R4. Protection against low input voltage is also provided by A8 and output voltage does not appear until the input line is approximately 185 vac.

3-29. External Signal Distribution Box 1A10, Circuit Analysis

(fig. 3-93)

The external signal distribution box provides the interfacing facilities between the external user and the shelter. The input and output lines are protected by spark gaps E101 through E204 and fuses F1 through F104. Filters FL1 through FL52 provide the necessary rf rejection. Filters FL51 and RL52 offer minimum impedance to frequencies between 0 and 23 kHz. Coaxial cables W105, W106, and W107 provide for transmission of the 70 MHz signal.



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S).
2. FL27 THRU FL31 AND FL38 THRU FL48 ARE SPARES.

HIGHEST REFERENCE DESIGNATION				
CP4	E252	F112	FL52	J16
T2	TB2	W111		
REFERENCE DESIGNATIONS NOT USED				
E98 THRU 100		FL49-52		J7
J8	J11	J14	W2-107	TB1

EL2LF196

Figure 3-93.① External signal distribution box, wiring diagram (sheet 1 of 9).

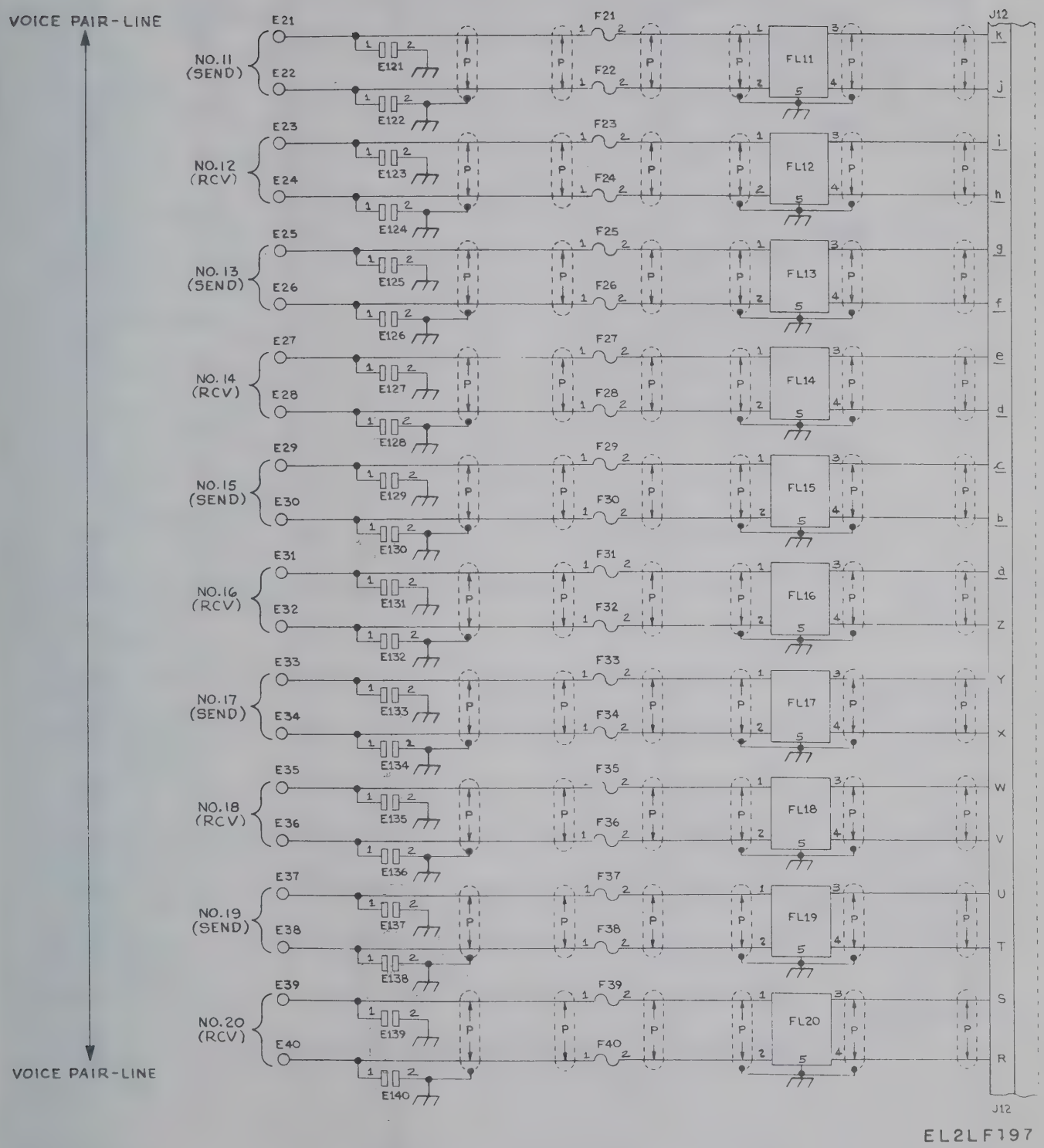


Figure 3-93.②External signal distribution box, wiring diagram (sheet 2 of 9).

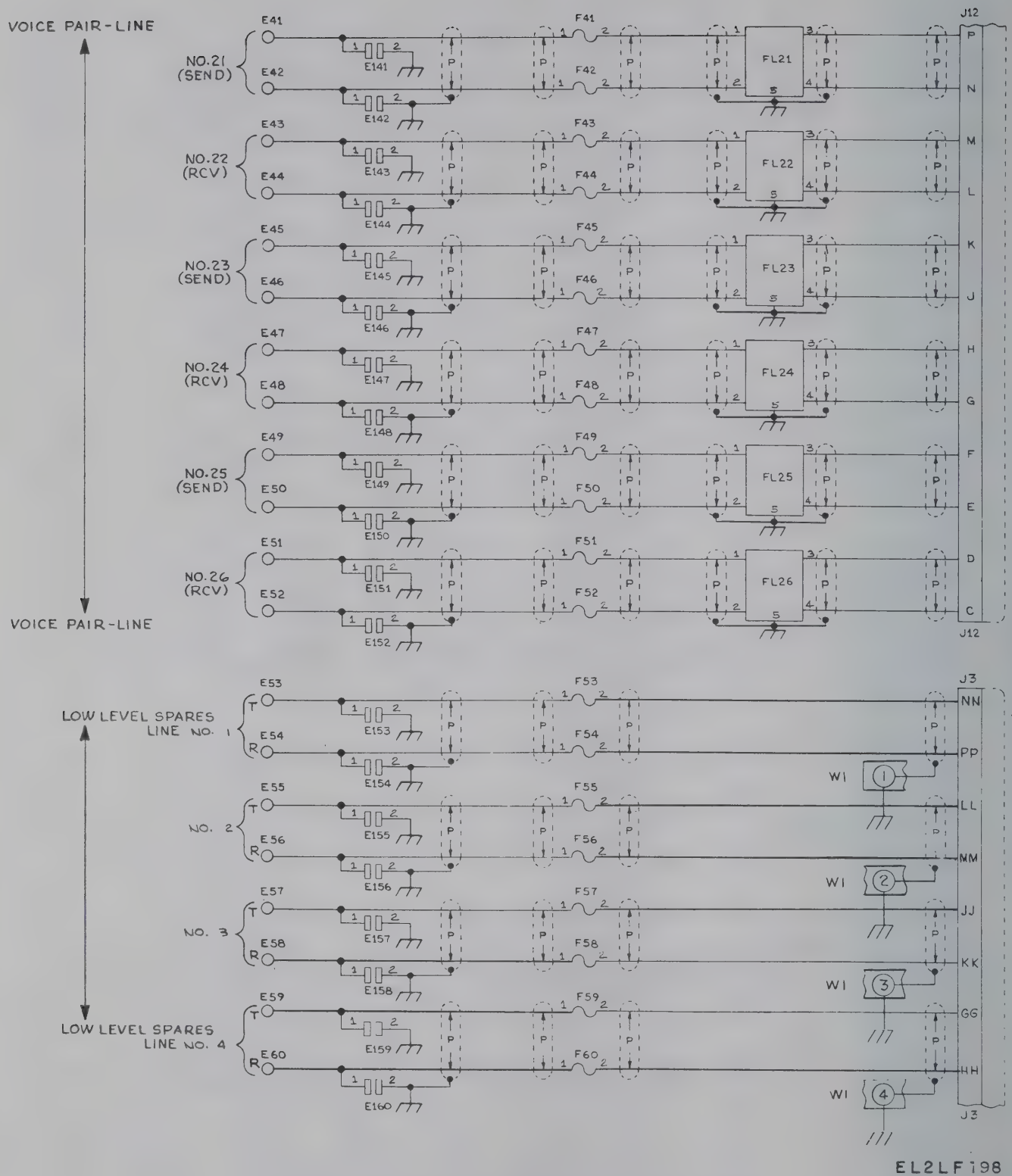


Figure 3-93.③External signal distribution box, wiring diagram (sheet 3 of 9).

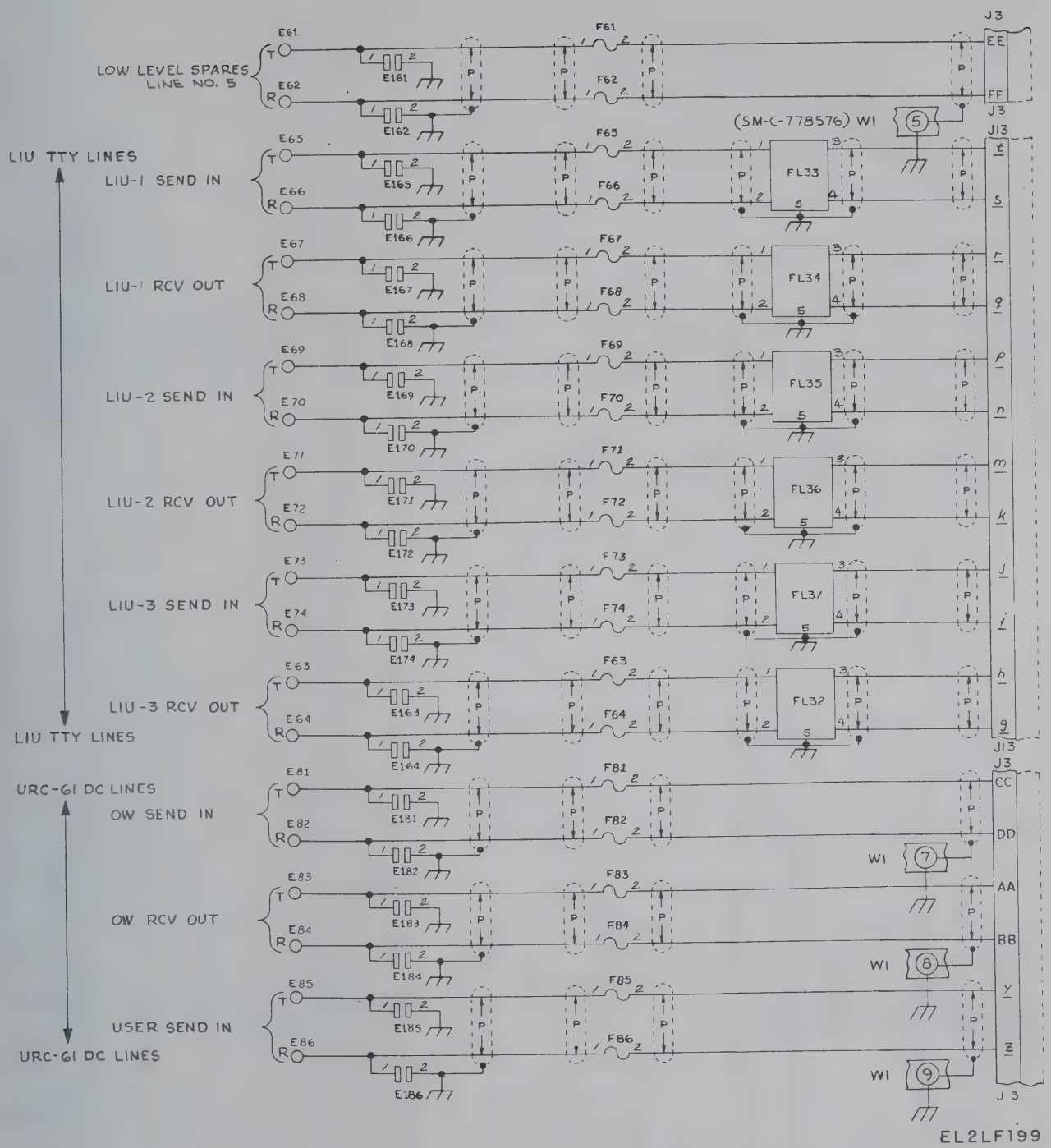


Figure 3-93.④External signal distribution box, wiring diagram (sheet 4 of 9).

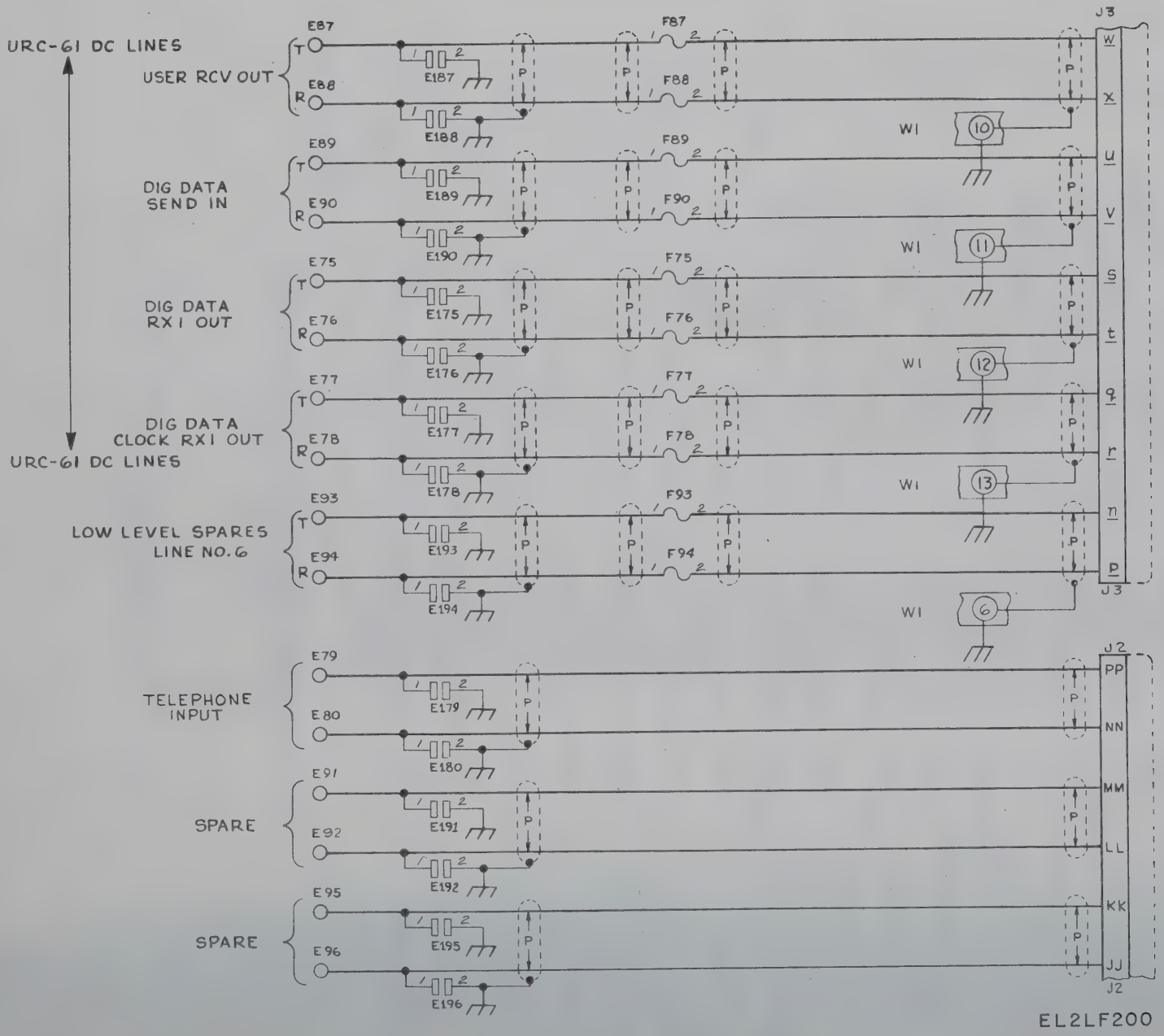


Figure 3-93.⑤External signal distribution box, wiring diagram (sheet 5 of 9).

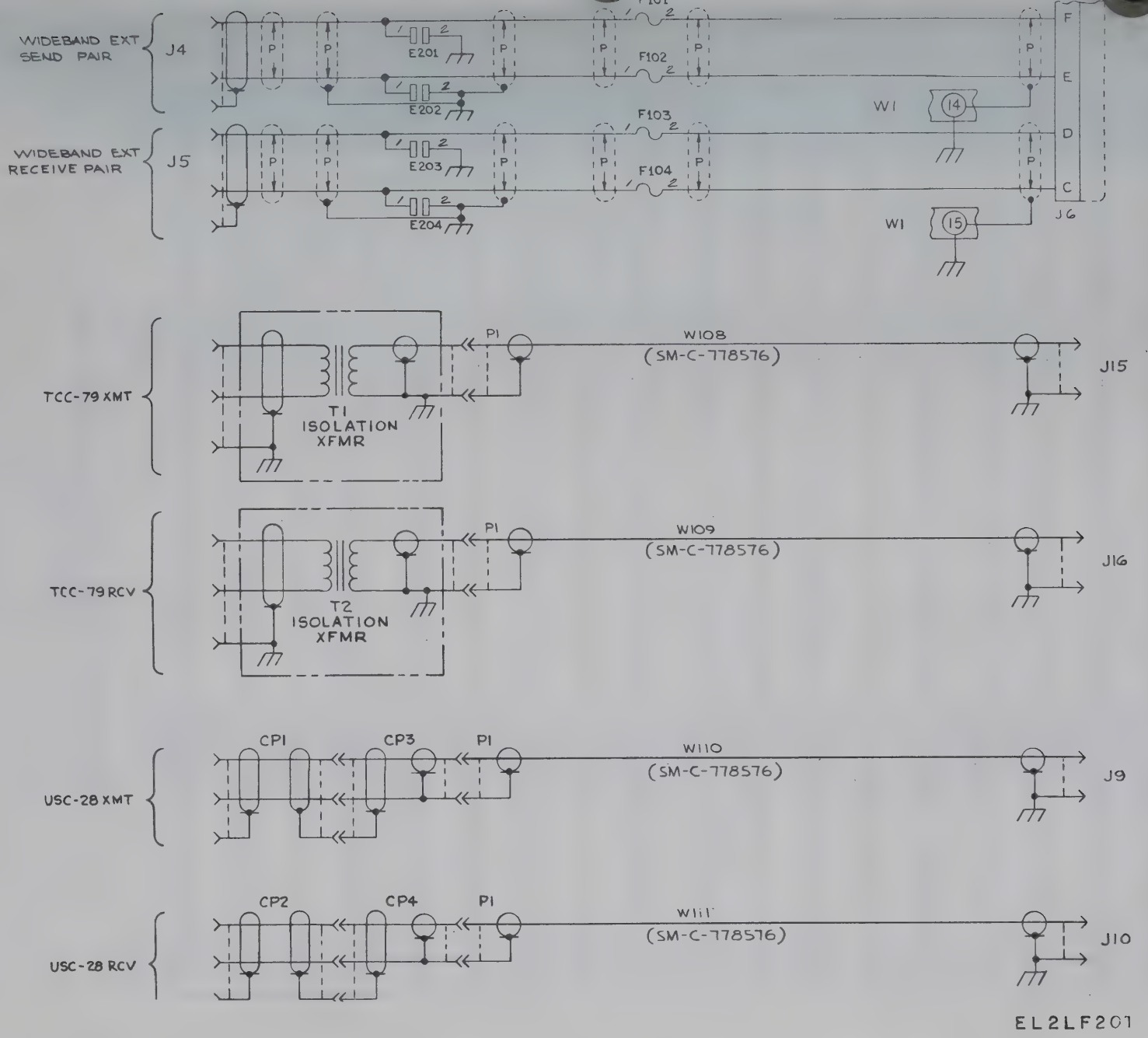


Figure 3-93.⑥ External signal distribution box, wiring diagram (sheet 6 of 9).

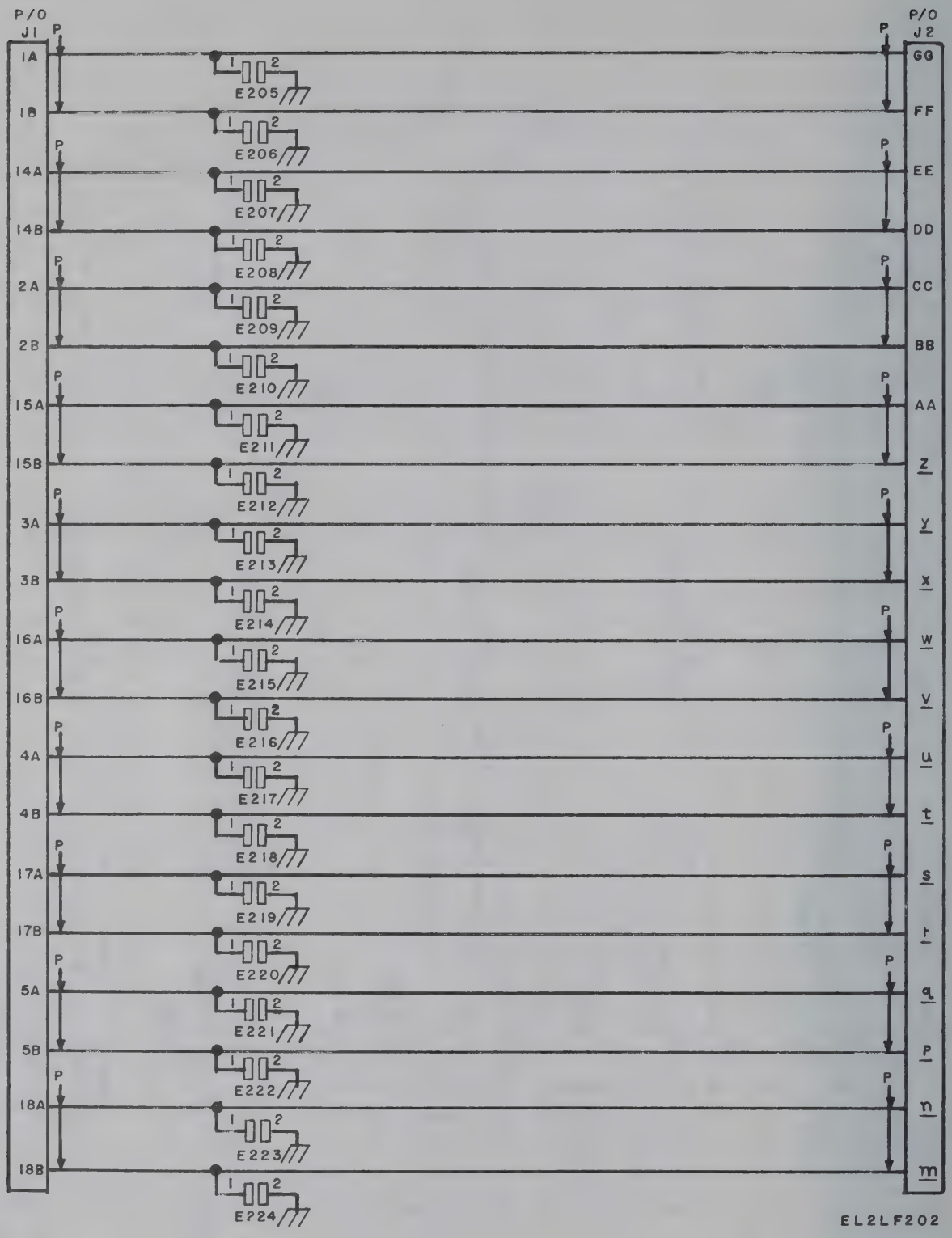


Figure 3-93.⑦External signal distribution box, wiring diagram (sheet 7 of 9).

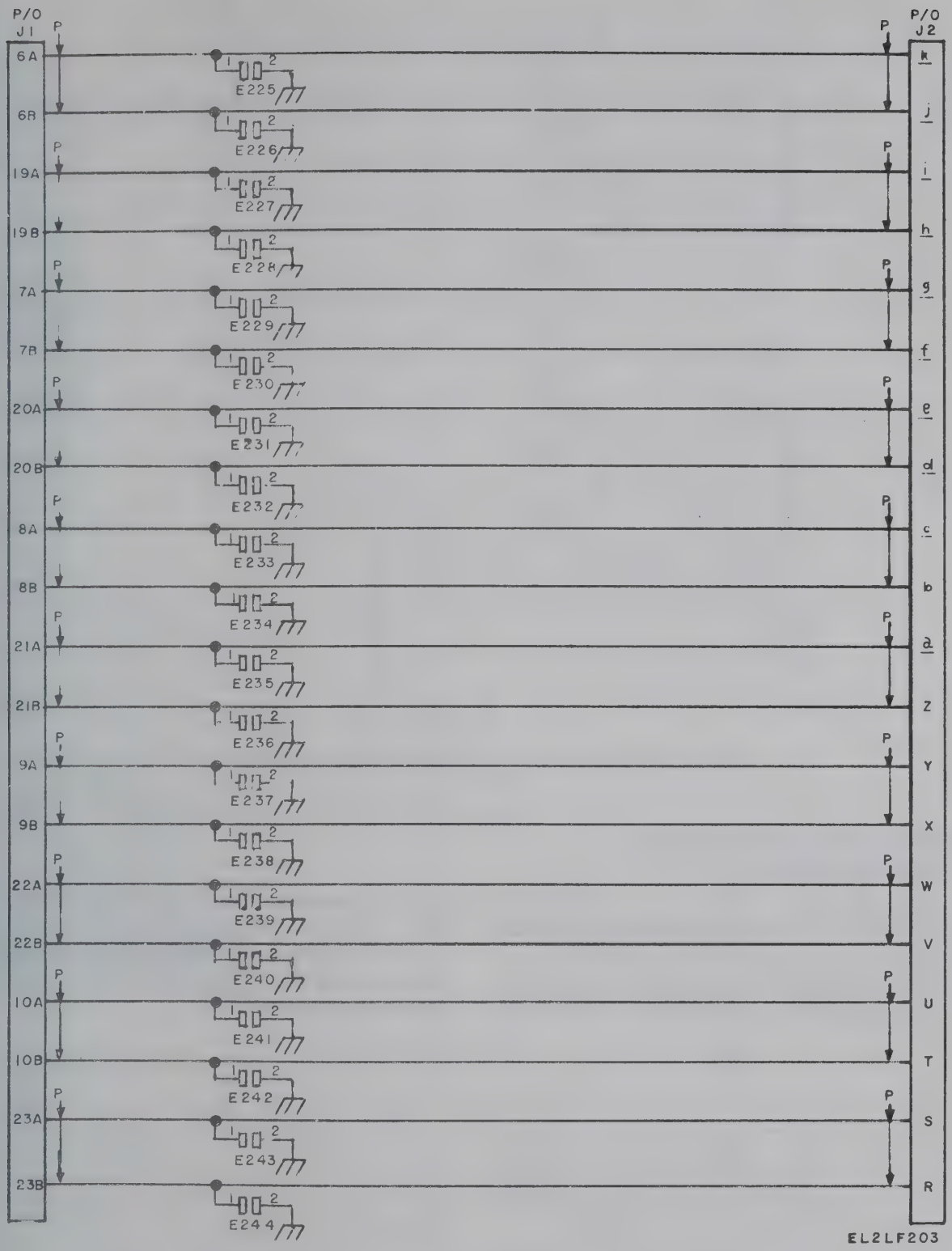


Figure 3-93.⑧External signal distribution box, wiring diagram (sheet 8 of 9).

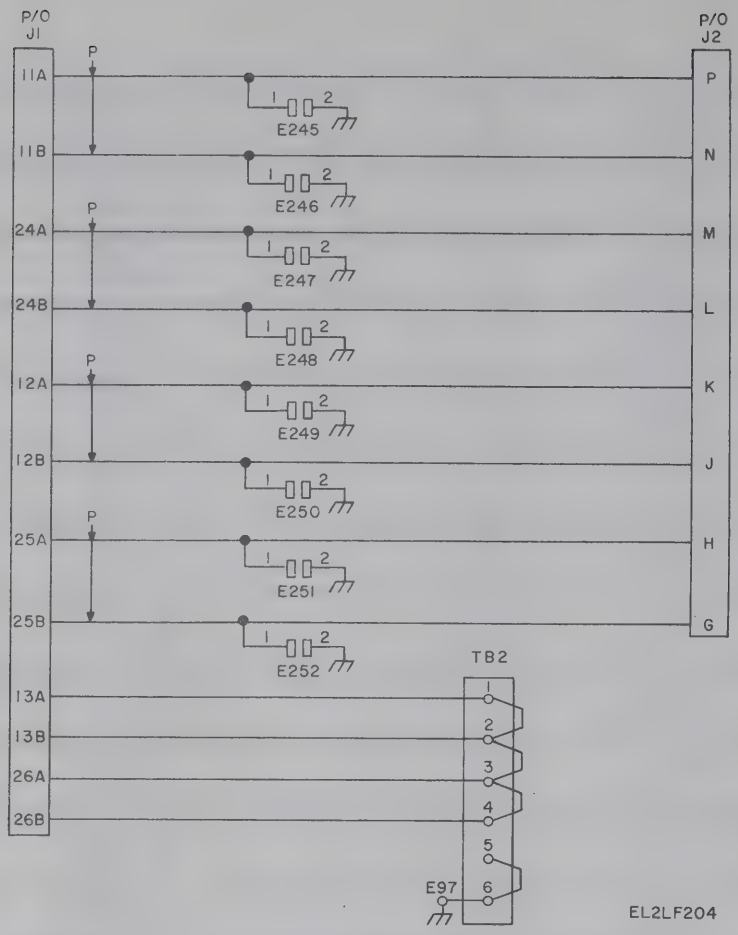


Figure 3-93.⑨External signal distribution box, wiring diagram (sheet 9 of 9).

3-30. Primary Power Distribution Assembly 1A12

(fig. 3-94)

The power distribution panel provides the controls for distributing 3-phase prime power within the shelter. This assembly contains two elapsed time meters which provide indications of operating hours for sensitive power and critical power circuits. The primary power filter 1A13 consists of four rfi filters for the 3-phase prime power applied to the shelter. The external power distribution box is shown in figure 3-95.

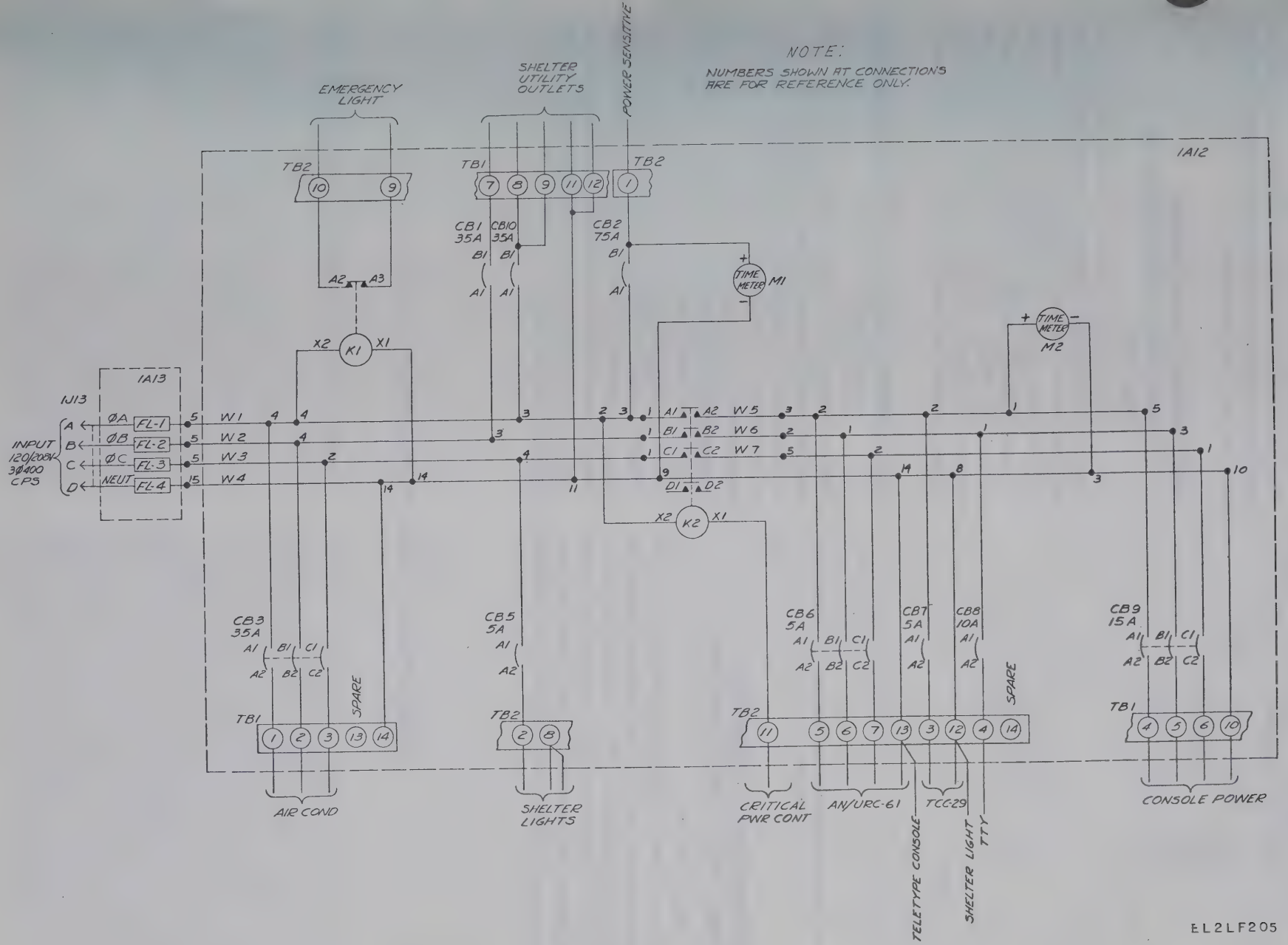


Figure 3-94. Primary power distribution assembly 1A12, schematic diagram.

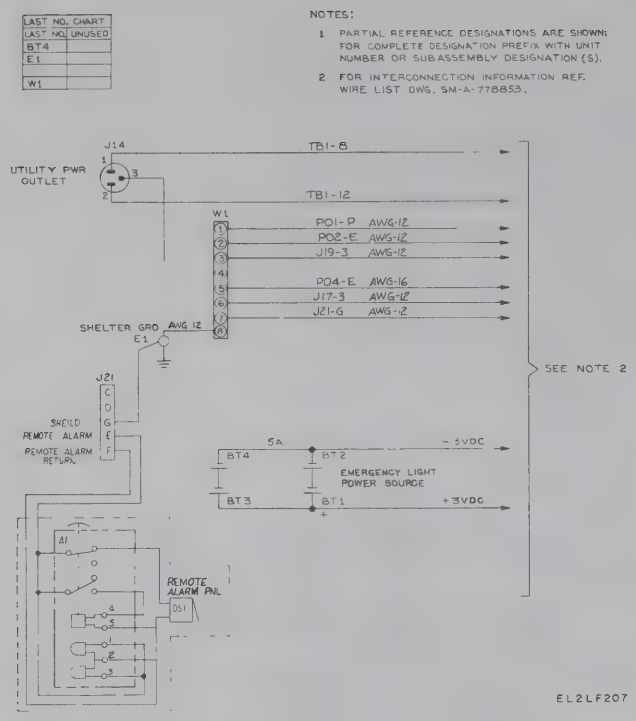


Figure 3-95. External dc power distribution box 1A14, schematic diagram.

3-31. Primary Power Distribution Panel 1A15, Circuit Analysis

(fig. FO 3-50)

The primary power distribution panel provides a distribution point for 115 vac, 3-phase power for the equipment shelter. The 3-phase power is applied to the panel at J1-A through J1-C from power distribution panel 1A12. Note also that neutral and ground are tied to J1-D and J1-E, respectively. All of the inputs are applied to terminal board TB1. From the terminal board the 115 vac is applied through circuit breakers to the output. Thermostat S1 controls shelter heat if switch S2 is OFF. When S2 is ON, the thermostat is bypassed and the shelter heater remains on regardless of the status of the thermostat.

3-32. Primary Power Monitor Panel 1A16, Circuit Analysis

(fig. 3-96)

The primary power monitor panel provides a monitor point for the frequency and voltage of the system power. The panel consists of voltage meter M1, frequency meter M2 and phase switch S1. The 3-phase primary power is applied through phase switch S1 which controls the input to voltage meter M1. Phase A is fed directly to meter M2 which provides an indication of input frequency.

3-33. Shelter Heater 1A17, Circuit Analysis

(fig. FO 3-51)

Shelter heater 1A17 provides heat for personnel comfort and equipment requirements. Heater circuit breaker CB1 on the primary distribution panel 1A15 applies 115 vac, 400 Hz, 3-phase power to thermostat S1 through relay K1 and heaters HR1 through HR6. Thermostat S1 opens at 300° F to protect the heater assembly in the event of failure and closes after opening at 270° F. Switch S2 on the primary power distribution panel bypasses the thermostat when S2 is ON. Primary power reaches fans B1 and B2 through relay K2. Redundant switches S2 and S3 provide a return path for relay K1 if the air flow is interrupted.

NOTE :

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUB-ASSEMBLY DESIGNATION (S).

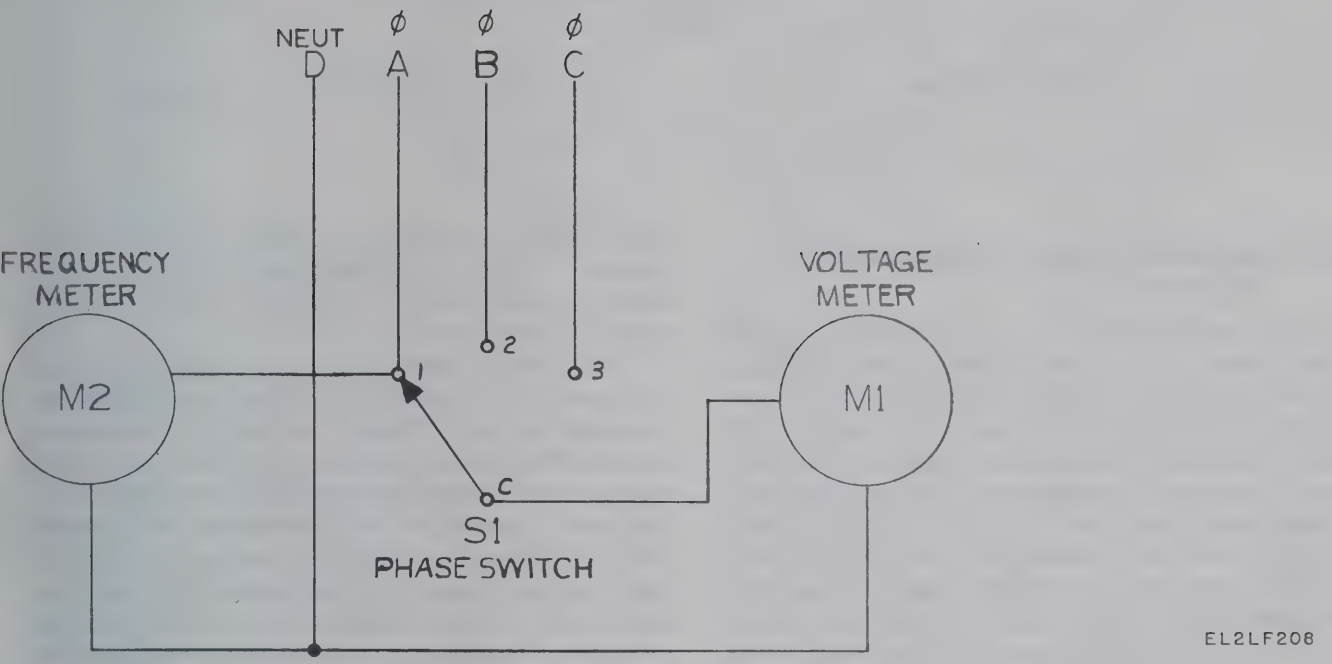


Figure 3-96. Primary power monitor panel 1A16, schematic diagram.

Section II. ANTENNA GROUP COMPONENTS

3-34. Power Supply PS1, Circuit Analysis
(fig. 3-97)

Power supply PS1 furnishes the high voltage required for operation of the AN/TSC-54 transmitter. The circuit consists of a three-phase full-wave bridge rectifier for the high voltage circuit and a single-phase full-wave bridge rectifier for a lower voltage output. Transformer T1 is a multitapped delta wound primary; wye round secondary. Bridge rectifier A1 rectifies the secondary voltage of transformer T1 and filtering of the output is provided by the two-section LC filter comprised of coil L1 and capacitor C1 and coil L2 and capacitor C2. The 13 KV high voltage output is applied to output terminals A and C through surge resistor R1. Resistors R3 and R4 form a voltage divider to provide an output to the beam voltmeter. The low voltage supply transformer T2 is energized through terminals E and F and the related bridge rectifier provides the necessary dc output which is filtered by the LC section consisting of capacitor C3 and inductor L3. The output is taken from terminals C and D. The link connections shown on the schematic diagram are for the 13 KV output requirement. For other output voltages the input link links can be connected to tape #4 for 12.3 KV, to #3 for 11.6 KV and to #2 for 10 KV.

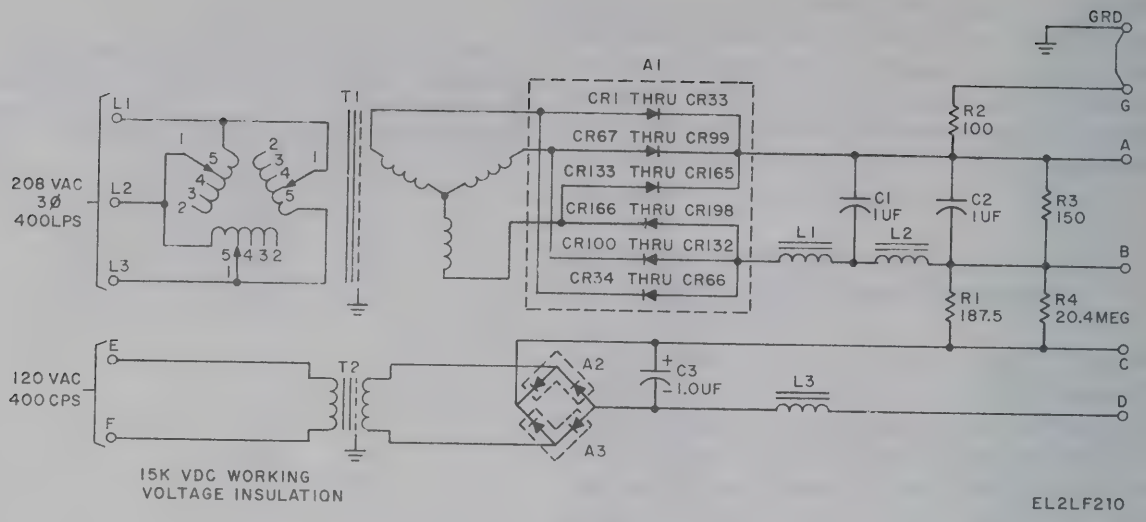


Figure 3-97. Power supply PS1, schematic diagram.

3-35. Transmitter Liquid Cooler 2A3A3

(fig. 3-98)

a. The transmitter liquid cooler 2A3A3 consists of heat transfer assembly 2A3A3A2 and rfi filter 2A3A3A1, and it is a liquid-to-air type heat transfer system utilizing an ethylene glycol and water coolant. The coolant mixture consists of 60 percent uninhibited ethylene glycol and 40 percent distilled water and is supplied at a minimum pump outlet pressure of 40 pounds-per-square-inch (psi). Coolant is pumped at a rate of 10 gallons per minute (gpm) and at a temperature of 63° C to 70° C (145° F to 158° F) while operating in ambient temperatures up to 49° C (120° F). The capacity of the system is approximately 3 gallons. Coolant carrying heat from the transmitter equipment is returned to the reservoir. The reservoir contains an air-space to allow for liquid expansion and a radiator-type pressure fill cap with a relief setting of 15 psi and the reservoir coolant level is monitored by two differential pressure switches.

b. Low liquid warning switch S1 opens, and low liquid interlock switch S2 closes when the coolant is at the proper level. Switch S1 closes when the coolant level drops below the minimum acceptable level of 5 inches, and as a result, +28 vdc unregulated power is applied through pins J2-C and J2-B, filter FL1A1, and pin Z of connector W1P26 (fig. FO2-4, sheet 5) to LOW LIQUID WARNING indicator DS1 (amber) on the transmitter control panel. Indicator DS1 illuminates and remains illuminated until equipment power is shut down or the coolant is replenished. When the coolant level drops 3-1/2 inches, switch S2 opens (fig. FO2-4, sheet 3) and deenergizes low liquid interlock relay K17 which removes the transmitter and beam power. Closed contacts A2 and A3 of relay K17 apply firing current to an SCR in latch circuit number 4 (fig. FO2-4, sheet 6 and 3-100), which in turn, applies power to illuminate LOW LIQUID indicator DS20 (red).

c. The system centrifugal pump takes coolant by suction from the reservoir and discharges it under pressure to one of three flow paths. One path is through the full flow three micron filter assembly through a particle filter coolant flow switch S3 to the heat exchanger and temperature control valve. Switch S3 remains open as long as satisfactory flow of coolant is maintained through the three micron filter. When the coolant flow decreases to 7.5 gpm due to clogging of the particle filter or any other faulty condition, switch S3 closes and applies +28 vdc unregulated power through filter FL1C1 and pin P26-NN (fig. FO 1-4, sheet 5) to illuminate LOW PARTICLE FIL COOL FLOW indicator DS2 (amber). Indicator DS2 remains illuminated until equipment power is shut down. This indicated fault is normally corrected by replacement of the three micron filter. Another path is through the filter bypass valve to the heat exchanger and the temperature control valve. The last path is through the backflush valve to the temperature control valve and outlet of the heat exchanger. Thus, hot coolant is supplied direct from the pump to the temperature control valve and cold coolant is applied from the heat exchanger to the valve.

d. Cooling is achieved in the heat exchanger by the fan drawing ambient air through the heat exchanger and exhausting it out through the fan orifice. The temperature control valve senses the output coolant temperature and automatically mixes hot and cold coolant to provide a constant flow of fluid between 63° C and 70° C (145° F and 158° F) to the transmitter equipment. The coolant tem-

perature and pressure are sensed at the output of the temperature control valve, and the values are displayed on gages located on the heat transfer system panel.

e. A portion of coolant (1/6 gallon per minute) from the pump is directed through a conductivity cell and a flow meter to the deionizer. The deionizer removes ions, minerals and oxygen from the coolant. The treated coolant is returned to the reservoir through a 0.35 micron filter, a second conducting cell and a flow control orifice.

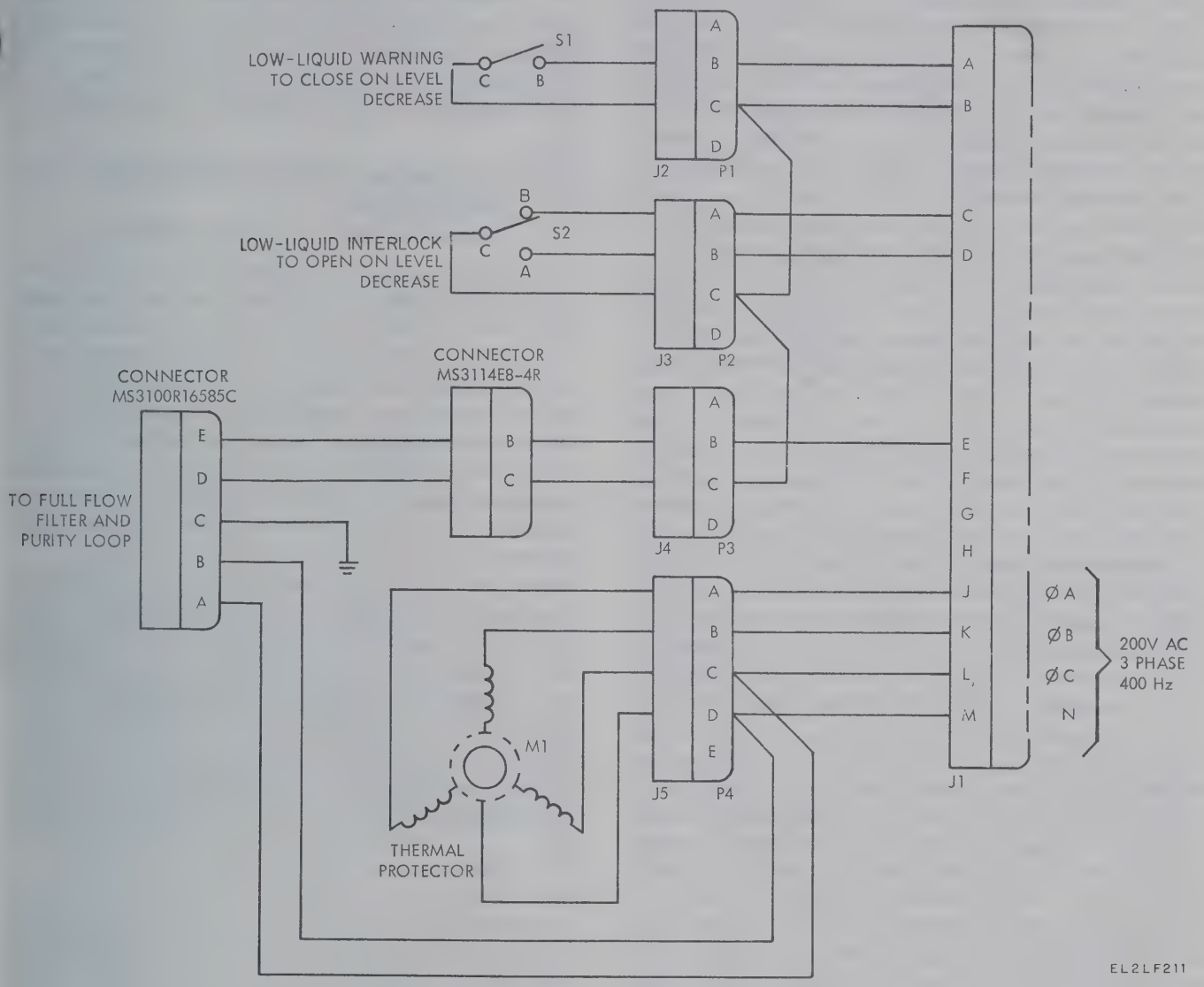


Figure 3-98. Heat transfer system, wiring diagram.

f. The coolant from the temperature control valve is applied to a manifold for distribution to the transmitter equipment. The coolant temperature is monitored by thermostatic switches S1 and S2 (fig. FO 2-4, sheet 3). If the coolant temperature is below 68° ±3° C (154° ±5° F), high coolant temperature switch S1 is closed and system coolant high temperature relay K21 is energized. When coolant reaches an abnormally high temperature of 73° ±2° (163.5° ±3.5° F), switch S1 opens and relay K21 deenergizes. Closed contacts A2 and A3 of relay K21 apply firing current to an scr in latch circuit number 4 (fig. FO 2-4, sheet 6) which in turn applies power to illuminate HIGH COOL TEMP indicator DS21 (red).

g. If the coolant temperature is above 1° ±2° C (34° ±4° F), low coolant temperature switch S2 is open. When the coolant temperature drops below −4.5° ±2° C (24° ±2° F), switch S2 closes and initiates two actions. First, +28 vdc unregulated power is applied through diode CR5 (fig. FO 2-4, sheet 5) to illuminate LOW COOL TEMP indicator DS4 (amber) on transmitter control panel 2A3A7 and through filter FL13A2 in primary power distribution panel 2A3A14 to illuminate LOW COOLANT TEMPERATURE indicator DS7 (amber) on rf

power monitor and control panel 1A3A27 (fig. FO 2-4, sheet 3) in transmitter exciter 2A3A10. Relay K1 applies power to heater HR1 and the coolant from the manifold is heated to compensate for extreme cold ambient temperatures. A pressure relief valve on the heater is set to operate at 200 psi.

h. Coolant flow through the transmitter equipment is monitored by flow switches S3 through S6 (fig. FO 2-4, sheet 3). Fluid must flow through waveguide and dummy load switch S2 and body and magnet switches S3 and S6 at a rate in excess of 1 gallon per minute. Flow through collector switch S5 must exceed 5 gpm. When the coolant flow through switch S3 or S6 drops below .5 gpm, the switch opens and body and magnet flow relay K18 is deenergized. Closed contacts A2 and A3 of relay K18 apply –28 vdc regulated power to fire an scr in latch circuit number 4 (fig. FO 2-4, sheet 6) which in turn applies power to illuminate BODY AND MAG FLOW indicator DS22 (red) on transmitter control panel 2A3A7. Liquid flow rate switches S4 and S5 (fig. FO 2-4, sheet 3) are connected in series to the +28 vdc regulated power source. Either switch (but not both) can simultaneously illuminate an associated fault indicator and denergize flow switches relay K19. Relay K19 is energized if satisfactory coolant flow is maintained through the waveguide components, dummy load and klystron collector coolant jackets. Under normal coolant flow conditions, flow switch S4 applies +28 vdc regulated power through switch S5 to energize relay K19. If the waveguide and dummy load coolant flow drops below 1 gpm, switch S4 operates to remove +28 vdc power from collector flow switch S5 which inhibits the collector flow indicator function, deenergize flow switches relay K19 and illuminate WG AND DUMMY LOAD FLOW indicator DS23 (red) on the transmitter control panel 2A3A7 through latch circuit number 1 (fig. FO 2-4, sheet 6). If the collector coolant flow rate drops below 5 gpm, flow switch S5 (fig. FO 2-4, sheet 3) operates to deenergize flow switches relay K19 and illuminate COLLECTOR FLOW indicator (red) on transmitter control panel 2A3A7 through latch circuit number 1 (fig. FO 2-4, sheet 6). Either indicator remains illuminated until a momentary interruption of the +28 vdc power by means of fault reset switches, resets latch circuit number 1.

3-36. Transmitter Control Panel 2A3A7, Circuit Analysis

(fig. 3-99 through 3-105 and FO 3-52)

The transmitter control panel of the AN/TSC-54 centralizes transmit function controls and indicators at antenna pedestal 2A3. The panel consists of metering circuits for selective monitoring of power, voltages and currents; switches for turn-on and control of power; and circuits for the display of actual and simulated faults. Operational theory discussions of the latch circuit, power sensing, power comparator, and diode switch modules of the transmitter control panel are given in *a* through *g* below.

a. Latch circuit No. 1 (fig. 3-99) has three identical silicon-controlled rectifier (scr) circuits individually capable of being switched to a continuous "on" state by a fault signal. Once turned "on", the circuit conducts, driving an indiciator lamp or relay, until the current path is externally interrupted by means of a reset switch. The following discussion is limited to the scr CR3 circuit which is typical of the three circuits contained in the module.

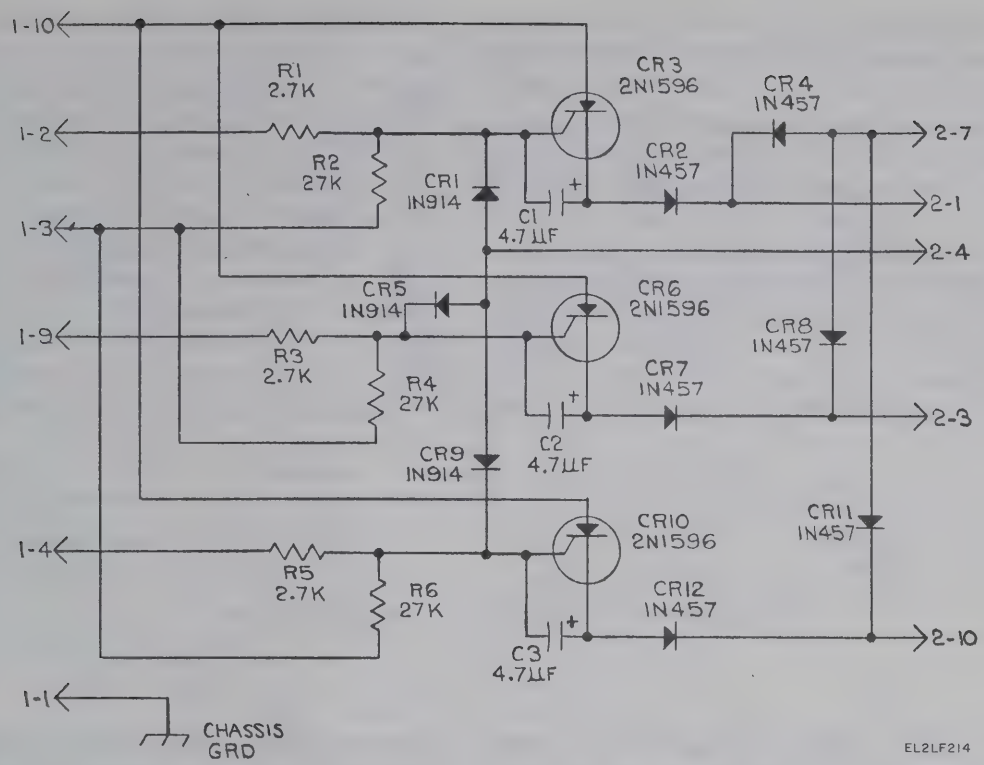


Figure 3-99. Latch circuit No. 1, schematic diagram.

(1) Resistor R1 is a current limiter. It provides a 10 mA gate current when a +28 vdc fault signal appears at pin 1-2. Upon application of a fault signal at pin 1-2, 10 mA flows into the gate of scr CR3 and fires the scr into full conduction. This action closes a current path from pin 2-1 through diode CR2 and scr CR3 to +28 vdc at pin 1-10. The device (lamp or relay) connected between pin 2-1 and the 28 vdc return line is thus operated and continues operating until the +28 vdc power applied to pin 1-10 is interrupted.

(2) During quiescent periods (no faults present), current flows from pin 1-3 (−28 vdc) through resistor R2 and diode CR1 to pin 2-4 (28 vdc) and maintains the gate of scr CR3 at a negative potential equivalent to the voltage drop across the junction of diode CR1. Capacitor C1 acts as a filter to prevent scr CR3 from firing on transients. Diode CR2 isolates scr CR3 from the lamp test circuit during lamp tests. Diode CR4 isolates the lamp test circuit and prevents interaction with the other fault circuits when a fault is detected. Application of +28 vdc lamp test power to pin 2-7 draws current through three external devices by way of pin 2-10 and diode CR11, pin 2-3 and diode CR8, and pin 2-1 and diode CR4. Scr CR6 and CR10 circuits operate like the scr CR3 circuit described above.

b. Latch circuit No. 4 (fig. 3-100) has two scr circuits. With two exceptions, each of the scr circuits operates like the typical circuit described in *a* above. First, in latch circuit No. 4, additional current paths are provided between pin 2-5 and the cathode of scr CR9 and between pin 1-10 and the cathode of scr CR10. The additional outputs facilitate operation of remote fault indicators. Second, fault signals applied to module pin 1-2 or 1-4 are also passed through diode CR2 or CR5, respectively, to pin 2-9. Either fault signal input can thus initiate operation of an external alarm device. Diodes CR2 and CR5 restrict the fault signals to their respective latch circuits.

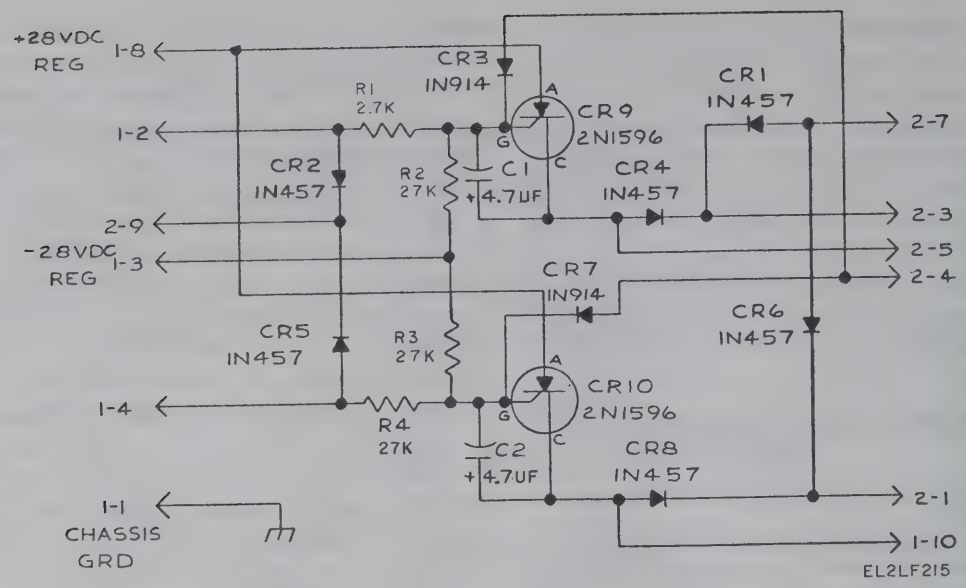


Figure 3-100. Latch circuit No. 4, schematic diagram.

c. Latch circuit No. 2 (fig. 3-101) has two scr latching circuits. Each circuit can be switched to its "on" state by a fault signal and continuously operate three external devices until the circuit power is interrupted by an external reset switch. Since both latching circuits are electrically and operationally indentical, only scr CR11 circuit is fully discussed as typical.

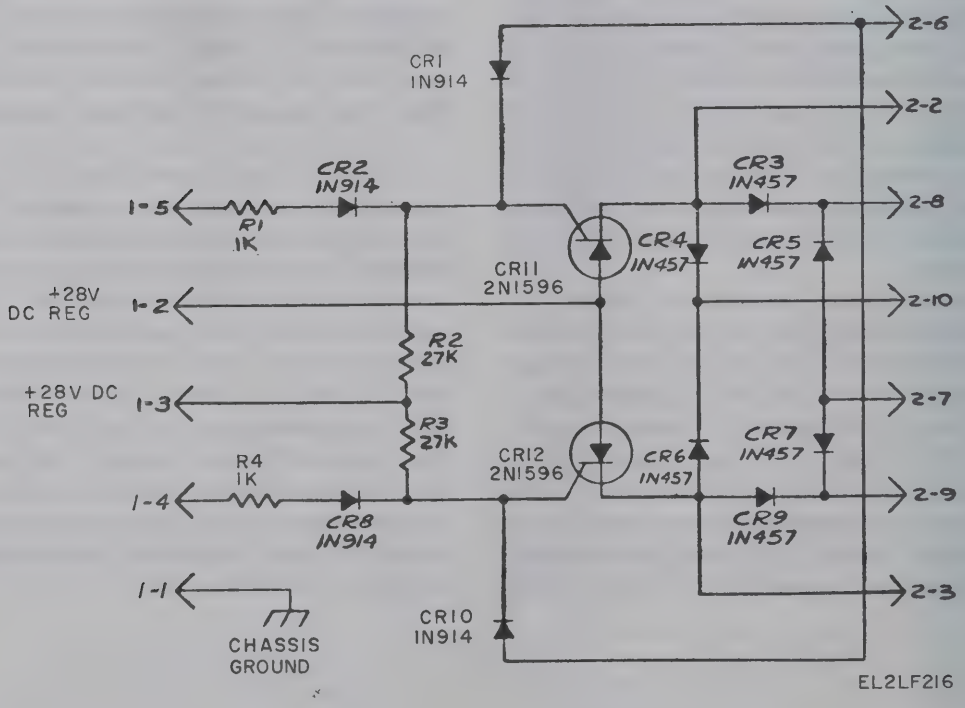


Figure 3-101. Latch circuit No. 2, schematic diagram.

(1) During quiescent periods (no fault present), current flow through module pin 1-3 (−28 vdc), resistor R2, diode CR1, and pin 2-6 (28 vdc return) maintains the gate of scr CR11 at a negative potential equal to the slight voltage drop across the junction of diode CR1. Upon application of a 15 vdc fault signal at pin 1-5, current flows through pin 1-3 and resistor R1 and provides about 12 mA of gate current to drive scr CR11 into conduction. This action simultaneously applies ±28 vdc power from

pin 1-2 through scr CR11 to three external devices. A direct output through pin 2-2 activates the diode switch driver module that fires the diode switch which removes rf drive from the system's klystron. A second output, applied through diode CR3 and pin 2-8, drives a fault indicator. A third output, applied through diode CR4 and pin 2-10, energizes a protective circuit relay that removes beam power from the system's klystron.

(2) Application of +28 vdc lamp test power through module pin 2-7 and diode CR5 and CR7, illuminates external fault lamps connected between a 28 vdc return line and pins 2-8 and 2-9, respectively. Diodes CR5 and CR7 isolate fault signals to their respective latching circuits. Diodes CR3 and CR9 isolate scr CR11 and CR12, respectively, from the lamp test circuit. Diodes CR4 and CR6 allow application of either fault signal to pin 2-10 without affecting the opposite latching circuit.

d. Low rf sensing circuit A6 (fig. 3-102) provides semiconductor device switch closure for illuminating power to external fault lamps when the system rf power decreases to a minimum acceptable level. The sensing circuit monitors a varying dc signal that corresponds with rf power level variations.

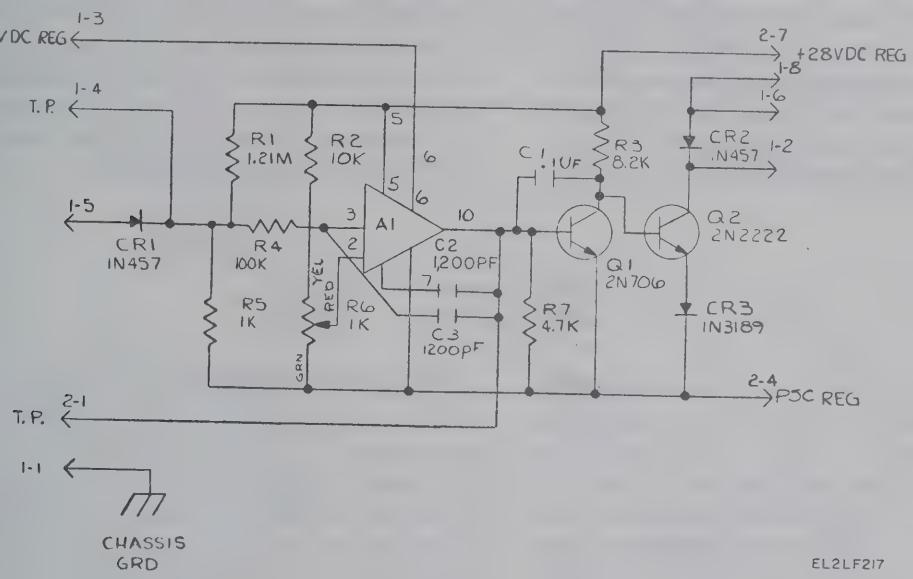


Figure 3-102. Low rf sensing circuit A6, schematic diagram.

(1) The varying dc signal is applied to module pin 1-5 of the sensing circuit by a detector amplifier. Level detector A1 of the low rf sensing circuit senses low rf power conditions by comparing the varying dc (rf power level input) signal with a preset reference level. The reference, obtained from a voltage divider consisting of resistor R2 and potentiometer R6, is set to a desired level between zero and +2.54 vdc and is applied to reference pin A1-2. Resistors R1 and R5 comprise a voltage divider that maintains approximately +0.023 vdc at signal input pin A1-3 during periods when the rf power is near zero. Diode CR1 in the rf power level signal input line blocks reverse current flow under very low rf power conditions.

(2) The rf power level signal input at module input pin 1-5 increases in a positive direction as the system rf power output increases. As soon as this input exceeds +0.023 vdc it is coupled to signal input pin A1-3 by resistor R4. However, no significant change occurs until the rf power level signal exceeds the present voltage level at reference input pin A1-2. As long as the rf power level signal remains less positive than the reference level, the output stage of level detector A1 remains in a nonconducting state and no current is present at output pin A1-10. This zero level holds transistor W1 in a cutoff state, and the ±28 vdc present at the collector of transistor Q1 forward biases transistor Q2 into full conduction. In this state, transistor Q2 completes a current path for fault lamp illuminating power. The current flows from the power supply common line at module pin 2-4 through diode CR3, transistor Q1 emitter-to-collector junction, to module pin 1-2 and also through diode CR2 to module pin 1-8. Externally, the current is further applied through two fault indicators to a ±28 vdc source, and the indicators illuminate.

(3) When the system rf output power increases above the minimum acceptable level, the rf power level signal applied at signal pin A1-3 becomes more positive than the present reference at pin A1-2, and the output stage of level detector A1 develops a 1 mA output. This current flow forward biases transistor Q1 into conduction, and a zero level applied from its collector to the emitter of transistor Q2 cuts off Q2. This action opens the current path for fault indicator illuminating power

and the indicators extinguish. The fault indicators remain extinguished while satifactory rf output power is maintained. Any decrease in rf power below the minimum acceptable level reverses conduction states within the rf sensing circuit, and thus causes the external fault indicator lamps to be illuminated. Capacitors C1, C2, and C3 filter stray rf and ac components from the signal routing line of the circuit. Module pin 1-6 provides an alternate current path through a lamp test switch for fault indicator testing.

e. Latch circuit No. 3 (fig. 3-103) has three identical latching circuits that can be individually switched to their "on" states by fault signals. When thus activated, the circuits continuously apply +28 vdc power to individual fault indicators or common protective devices until the power is interrupted by means of an external reset switch. Each latching circuit generally operates like the typical circuit described in *a* above. Notable differences include multiple outputs, higher voltage levels for gating the scrs, and additional diodes for isolation between circuits. Input signals to latch circuit No. 3 come from current source output level detectors (output $\simeq$ 1.0 mA). The 1.0 mA gate current is sufficient to fire the scr. Diode CR2 isolated the input to pin 1-4 when a fault signal is applied to either pin 1-2 or 1-5. The normal output, routed through diode CR3 and pin 2-5, illuminates a fault indicator. A direct output through pin 2-10 operates a vacuum switch that discharges high-voltage capacitors in beam power supply 2A2. An output applied through diode CR5 and pin 1-8 energizes a protective circuits relay that removes beam power from the system's klystron. Diode CR5 isolates scr CR4 circuit when either one of the other two latching circuits is activated by a fault signal. Pin 2-7 is the lamp test power input pin.

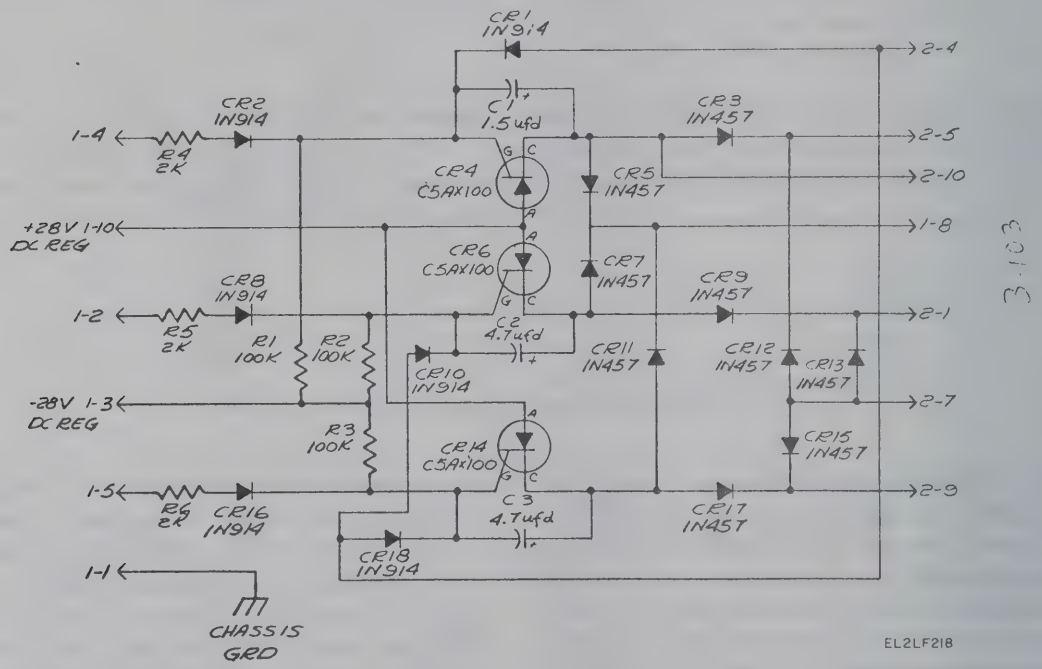


Figure 3-103. Latch circuit No. 3, schematic diagram.

f. The isolator arc sensing circuit (fig. 3-104) provides a gate signal to a latch circuit that illuminates a fault lamp to denote waveguide arcing and also initiates a fault lamp to denote waveguide arcing and also initiates a circuit-protect function. Dc amplifier AR1 is in the circuit monitors two dc levels that represent rf forward power at separate points in the high-power segment of the system's microwave circuit. One dc level is applied through module pin 1-4 to amplifier pin AR1-3; the other dc level is applied through module pin 2-9 and diode CR1 to amplifier pin AR1-2.

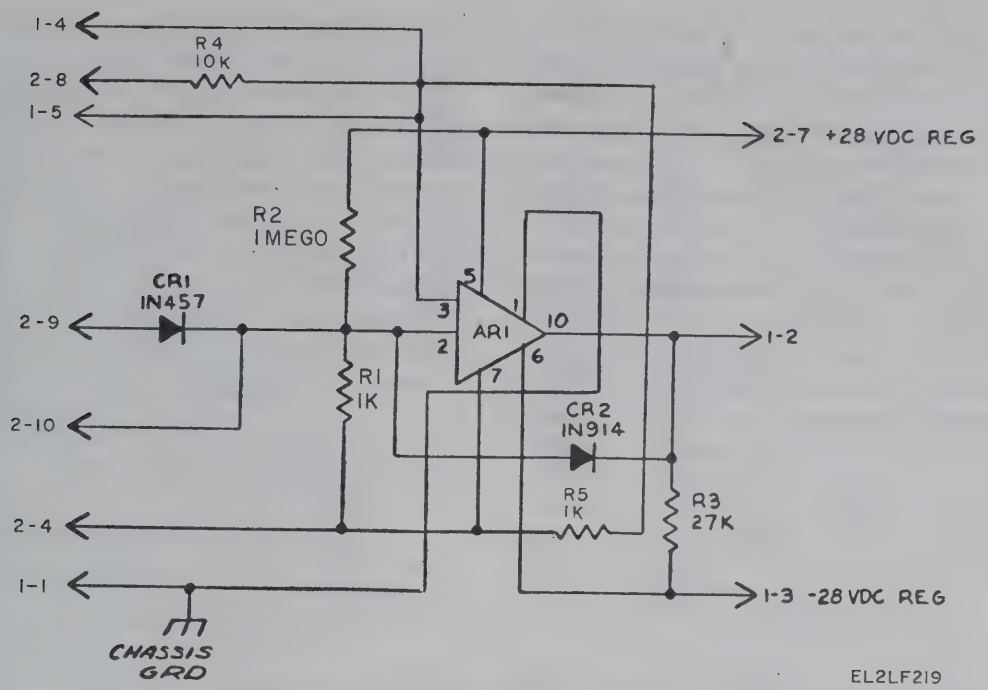


Figure 3-104. Isolator arc sensing circuit, schematic diagram.

(1) During normal transmit operations of the AN/TSC-54, the dc level at pin AR1-2 is more positive than the dc level at pin AR1-3. This normal relationship of the inputs results in a zero potential at amplifier output pin AR1-10 and module pin 1-2, and the external latch circuit is not affected. Occurrence of a waveguide arc reverses the relationship of the two dc level inputs, and thus causes conduction in the output stage of amplifier AR1 accompanied by a rise in pin AR1-10 voltage level at +15 vdc. This positive transistion is a gate signal to the latch circuit connected externally at module pin 1-2. The gate signal causes the latch circuit to apply operating power that initiates fault-indicate and circuit-protect functions. Resistors R2 and R1 comprise a voltage divider that maintains amplifier pin AR1-2 at a +0.023 vdc level during system standby periods when the two dc level inputs, that represent rf forward power, are at zero.

(2) This fixed-level difference between amplifier pins AR1-2 and AR1-3 ensures against inadvertent operation of the arc sensing circuit and initiation of the fault-indicate and circuit-protect functions. Resistors R4 and R5 comprise a voltage divider that develops a +2.55 vdc level that is applied to amplifier pin AR1-3 to simulate a waveguide arc condition. The +2.55 vdc level is applied in this manner when a +28 vdc arc test level is applied to module pin 2-8. The simulated rise in voltage level at pin AR1-3 affects amplifier AR1 in the same manner as an abnormal drop in the voltage level at pin AR1-2, thus a waveguide arc condition is artifically produced for testing the external fault-indicate and circuit-protect devices.

g. Diode switch trigger circuit A9 (fig. 3-105) provides a semi-conductor device switch closure that initiates an external circuit-protect function. Four electrically identical input circuits monitor operating conditions at two points in the high-power segment of the system microwave circuits. Satisfactory operating conditions are denoted by zero-level inputs while operational faults (high vswr or waveguide arcs) are denoted by +28 vdc level inputs to module pins 1-2, 1-4, 1-5, and 2-2. The diode switch trigger circuit remains quiescent while the system's transmiter circuits are functioning normally.

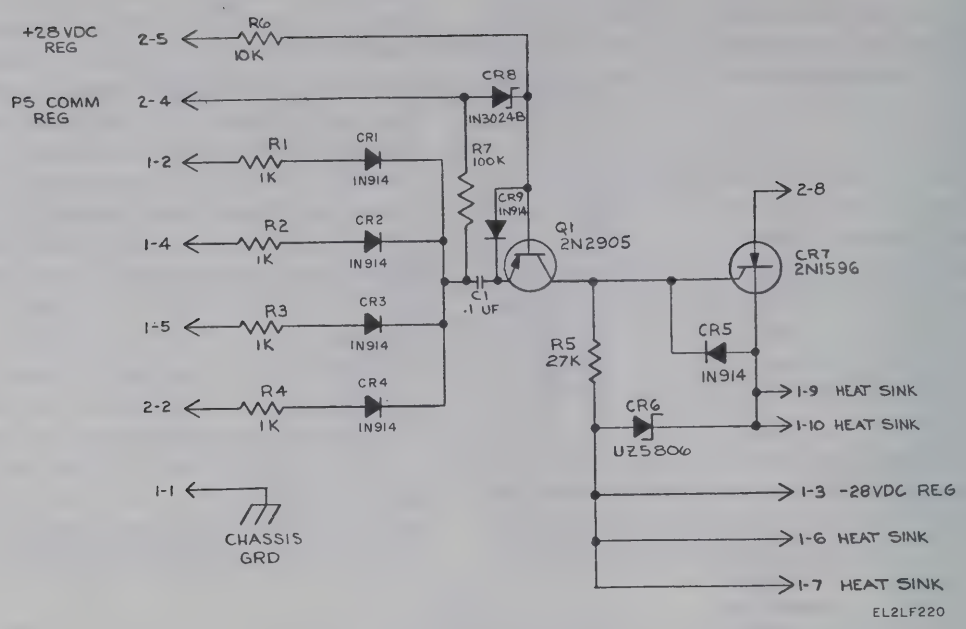


Figure 3-105. Diode switch trigger circuit A9, schematic diagram.

(1) Current flows from module pin 2-5 (28 vdc), through resistor R6 and Zener diode CR8 to modulepin 2-4 (+28 vdc return). Resistor R6 limits the current flow through diode CR8, and CR8 maintains a +15 vdc level at its anode and at the base of transistor Q1. A slight voltage drop across the diode CR9 junction results in a less positive voltage at the emitter of transistor Q1, and thus reverse biases A1 in a nonconduction state. Scr CR7 also remains in a nonconduction state until fired into full conduction by a positive trigger at its gate. When a fault occurs and a +28 vdc signal is applied to any one of the fault signal input pins, the diode switch trigger circuit is activated. For example, a klystron waveguide arc fault signal at pin 1-2 causes current flow from pin 1-2 through resistor R1, diode CR1, capacitor C1, and through the emitter of transistor Q1, causing Q1 to conduct briefly. This current pulse is applied to the gate of scr CR7. Resistor R7 provides a discharge path for capacitor C1 after a fault has been cleared.

(2) Once fired in this manner, scr CR7 continues conducting until the current path is externally interrupted by means of a reset switch. Current now flows through pin 1-3, Zener diode CR6, the cathode-to-anode junction of scr CR7 and output pin 2-8 to a diode switch. Zener diode CR6 drops 7 vdc, therefore a −21 vdc level is applied to the diode switch. The negative voltage biases the diode switch in an "off" stage, attenuating driving power to the system's klystron by 40 dB. Heat sink pins 1-6, 1-7, 1-9, and 1-10 are not connected externally in the AN/TSC-54 application of the diode switch trigger circuit module.

h. The relay box illustrated in figure FO 3-53 is a central housing for the relays necessary to complete the latching functions initiated on the transmitter control panel. It also completes interlock and fault functions originated by the transmitter liquid cooler sensing circuits.

3-37. Transmitter/Exciter 2A3A10, Circuit Analysis.

(fig. 3-106 through 3-113 and FO 3-53 through FO 3-55)

The frequency modulated (fm) send signals from the if patch panel are converted to discrete frequencies by three identical upconverters. Each upconverter converts a 70 MHz±20 MHz IF. signal into an RF signal in the frequency range between 7.9 to 8.4 GHz. Refer to COMTECH manual TM 11-5895-833-34-2 for the detailed theory of operation of the upconverter. Signal translation to a transmit frequency is followed by progressive power amplification within the transmitter exciter to a desired carrier level. An initial increase is provided by a traveling wave-tube (twt) rf amplifier and final amplification is achieved through a kylstron electron tube. The two-stage amplification produces an 8 kW power level; however, this level is diminished to a 5.25 kw carrier level after losses are incurred by subsequent isolator and bandpass limiting components. Transmitter exciter 2A3A10 contains detector amplifiers A9 through A12, arc detector amplifier A13, rf amplifiers A14 and A15, and rf heads A16 and A22. Figure FO 3-54 is the interconnecting diagram for the transmitter exciter.

a. Within detector amplifiers A9 through A12 (fig. 3-106), a power signal level is developed across the resistor network of R1, R2 and R6, and is coupled by resistor R4 to pin 3 of the dc amplifier. A reference voltage level of approximately −6.5 vdc is applied at pin 2 of the dc amplifier. The reference voltage is derived from a voltage divider network consisting of resistors R3 and R5, diode CR1 and CR3, and an external 1-kilohm resistor in isolator comparator module 2A3A7A1A8. The dc amplifier produces a positive output at pin 10 as long as the positive dc signal at pin 3 remains at or above a minimum acceptable level.

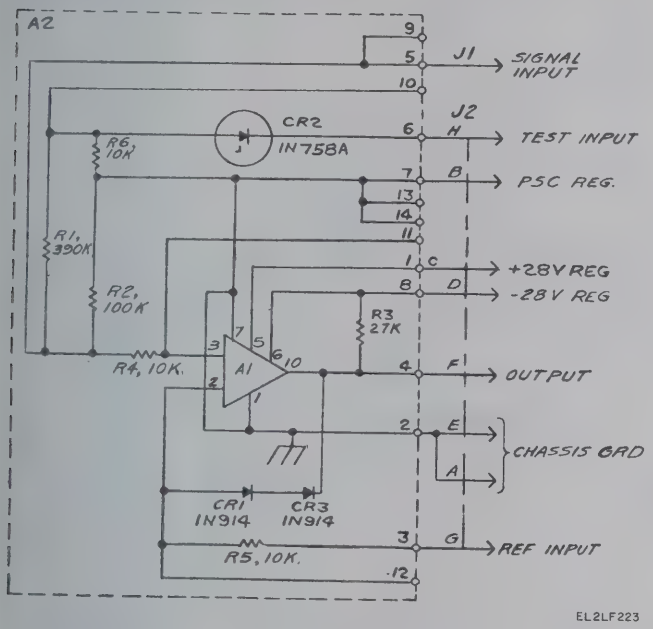


Figure 3-106. Detector amplifier, schematic diagram.

b. Arc detector amplifier A13 (fig. 3-107) consists of a photo-sensitive semiconductor element, a detector circuit, and a test lamp. In normal transmitting operations, the device detects arcing that may occur in either the klystron electron tube or its output port and waveguide by literally looking directly into the output of klystron and electromagnet assembly A19. The detector is physically oriented on waveguide adapter AT8 so that its photodiode CR2 is directly exposed to light from arcs in the klystrons output port by direct alignment through a 0.187-inch diameter drilled view passage in the adapter. Photodiode CR2 is a junction-barrier device used as a photo-voltaic cell. Connected in parallel across resistor R3, the photodiode is reverse-biased approximately 2 volts and only barrier leakage current flows in an insignificant amount under dark (no arc) conditions. When an arc occurs, the light striking the photodiode's reverse-biased junction produces an increase current flow across the junction. Effectively, the resistance decreases and the voltage at dc amplifier pin 3 rises. When the voltage at pin 3 rises sufficiently to overcome the effects of a reference voltage applied at pin 2, the dc amplifier produces a positive output at pin 10. An external voltage divider consisting of resistor R4 and potentiometer R5 in transmitter control panel 2A3A7 supplies the positive reference voltage to dc amplifier pin 2. Potentiometer R5 in the voltage divider network is the level-set adjustment control for the reference voltage. Test lamp DS1 can be illuminated to simulate an arc for fault test purposes; the lamp illuminates a drilled chamber and a milled passage which directs part of the light to the photodiode and triggers the detector circuit.

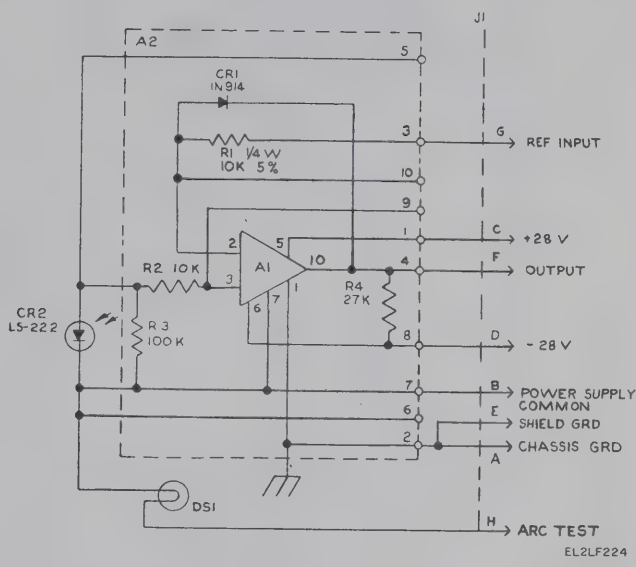


Figure 3-107. Arc detector amplifier, A13,schematic diagram.

c. Input/output signal characteristics for rf amplifier A14 are shown in figure 3-108. Rf amplifier A15 (fig. 3-109 and 3-110) contains a voltage regulator network ((1) below), dc amplifier ((2) below), comparator amplifier ((3) below), reference network ((4) below), and a feedback network ((5) below):

(1) The voltage regulating network consists of

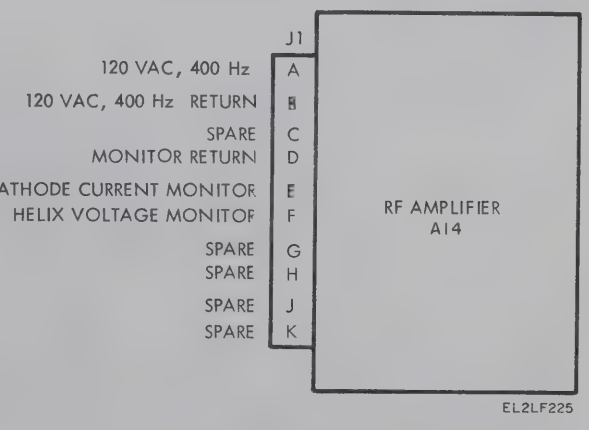


Figure 3-108. RF amplifier A14 input and output characteristics.

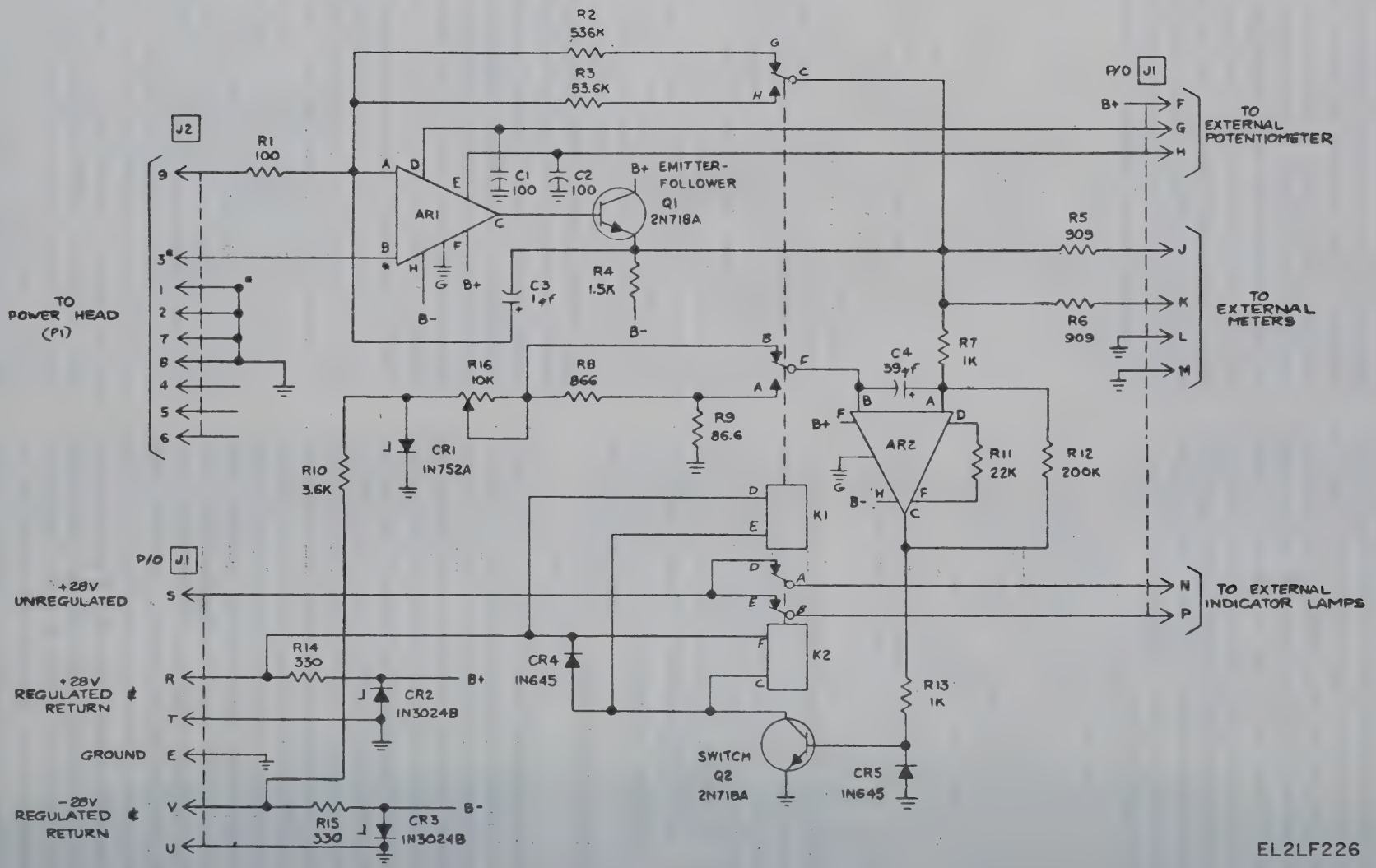


Figure 3-109. Rf amplifier A15, schematic diagram.

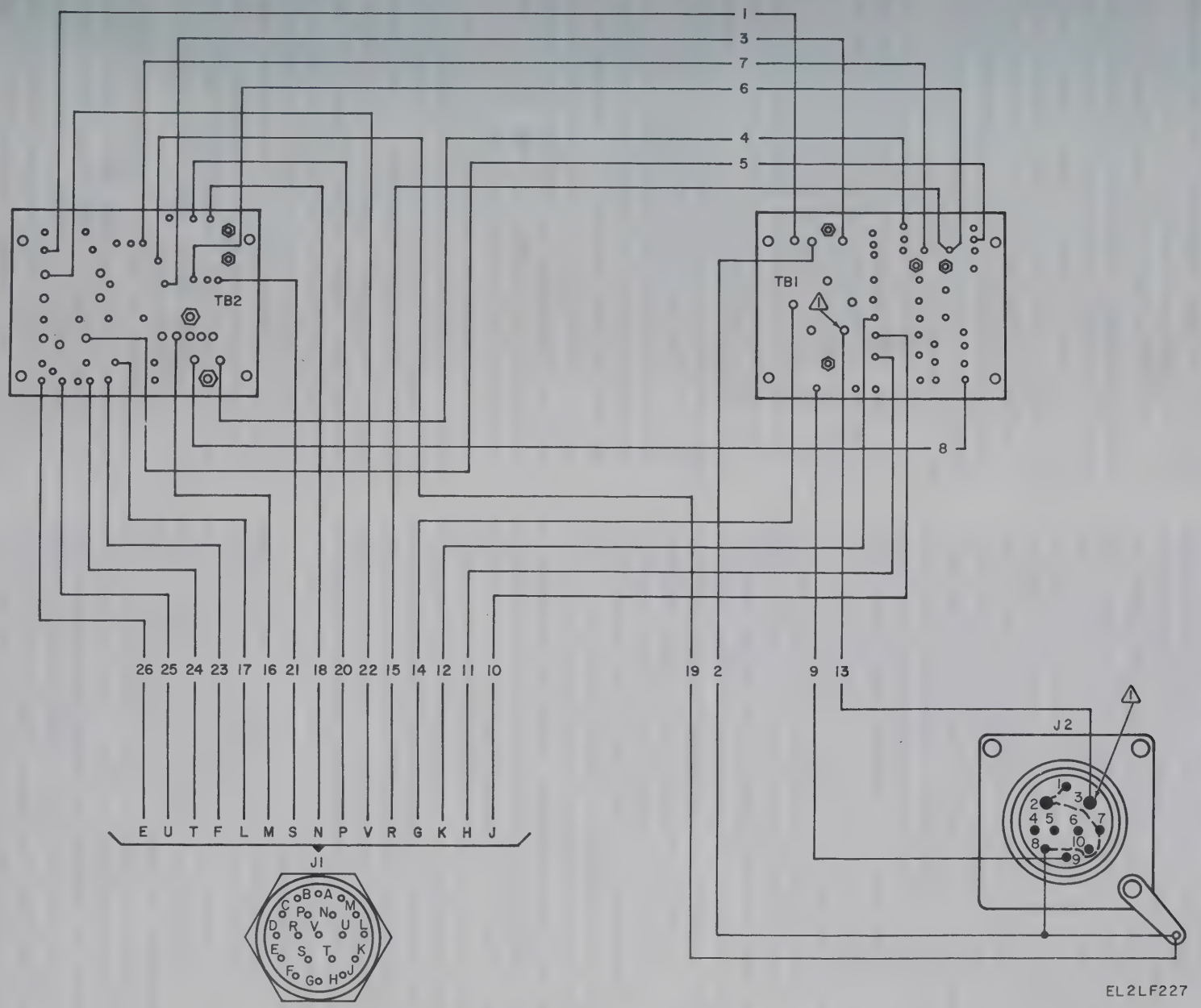


Figure 3-110. Rf amplifier A15, wiring diagram.

resistors R14 and R15 and Zener diodes CR2 and CR3. Resistors R14 and R15 drop the applied voltage down to the breakdown voltage level of CR2 and CR3. Regulated B+ and B- is developed across Zeners CR2 and CR3, respectively.

(2) The dc amplifier consists of amplifier AR1, capacitors C1, C2 and C3 and an external potentiometer. A dc input signal from the rf head is applied to pins A and B of amplifier AR1. The gain of AR1 is determined by the ratio of the feedback network resistance ((5) below) and the resistance value of the temperature compensated gain control network in the rf head. The output from amplifier AR1 is applied to the RF POWER meters on the transmitter control panel and rf power monitor control. Capacitors C1 and C2 filter out any noise on the output of amplifier AR1. The signal at the emitter of transistor Q1 is also applied to either feedback resistor R2 or R3 through relay contact K1C. This output is also applied to the RF POWER meter and comparator amplifier AR2.

(3) The inputs to comparator amplifier AR2 are from emitter follower Q1 and the reference network ((4) below). The gain of amplifier AR2 is determined by resistor R11. When the input from the reference network is more negative than the input from amplifier AR1, the output of comparator AR2 will be negative. Conversely, when the input from the dc amplifier is more negative than the input from the reference network, the output of comparator AR2 will be positive. When a negative voltage appears on the output of comparator AR2 it is felt on the base of transistor Q2. Transistor Q2 will stop conducting and deenergize relay K2. With relay K2 deenergized the +28 vdc will be applied to the LOW RANGE indicator (on the transmitter control panel) indicating that the RF POWER meter is in the LOW RANGE. When a positive voltage appears on the output of AR1, transistor Q2 will conduct, causing relay K2 to energize and extinguish the LOW RANGE indicator, indicating tha the RF POWER meter is in the high range. When relay K2 is energized, it also changes the feedback path around amplifier AR1 to lower its gain by a factor of 10.

(4) The input to the reference network, composed of resistors R8 through R11 and Zener diode CR1, is -28 vdc applied from jack J1-V. Potentiometer R10 drops the applied voltage down to the breakdown voltage of diode CR1. When the RF POWER meter is in the LOW RANGE, relay K1 will be deenergized and the output from the reference network will be across the series combination of resistors R8 and R9. When the RF POWER meter is in the high range, relay K1 will energize and the output from the reference network will be across resistor R9 only.

(5) When the RF POWER meter is in the LOW RANGE, relay K1 will be deenergized and feedback resistor R2 will be across amplifier AR1, increasing the gain of AR1. When the RF POWER meter is in the high range, relay K1 will energize and feedback resistor R3 will be across amplifier AR1, decreasing its gain to compensate for the larger input signal.

d. Input/output signal characteristics for dc amplifier AR1 are shown in figure 3-111 and the input/output signal characteristics for comparator amplifier AR2 are shown in figure 3-112.

e. The rf head (fig. 3-113) contains an rf network and a temperature compansating network. The rf network consists of capacitors C3, C4, and C5, resistor R1A/B and LC filters L1 and C1, and L2 and C2. The temperature compensating network consists of ballast resistor RT1 and resistors R2 and R3. The rf network contains a thin-film thermoelectric (tft) element which is represented by capacitors C4 and C5 and resistor R1A/B.

(1) The tft element, when placed in a transmission line, absorbs incident rf power. Some of the junctions of the tft are thermally bonded to the transmission line, while the remaining junctions are suspended in the air space inside the transmission line. The rf energy that is absorbed by the junctions located in the air space causes a temperature increase in the air space junctions relative to the thermally bonded junctions. The temperature difference between the two junctions creates a voltage across the junctions. This voltage is directly proportional to the temperature difference between the two junctions. By keeping the temperature differential between the two junctions low, the tft will sense an rms temperature change and produce a dc output voltage that is directly proportional to the abosrbed power.

(2) Rf power is coupled to the tft through capacitor C3. Capacitor C3 isolates the tft from any dc voltage that may be present in the rf signal. Since the rf is applied to the center point of resistor R1A/B, the resistor appears as two resistors in parallel. The parallel network formed by resistor R1A and R1B has an equivalent resistance which matches the input of the tft to the transmission line. The output of the tft is taken across resistor R1A/B which now may be considered as two resistors in series. The LC network of L1 and C1, and L2 and C2 are provided to filter out any stray rf appearing on the output.

(3) Since the tft is temperature sensitive, a temperature compensated gain control network, consisting of resistors R2, R3 and ballast resistor RT1 is provided. A change in temperature will cause a change in the resistance of ballast resistor RT1. The total resistance across RT1, R2 and R3 determines the gain of a dc amplifier that is part of rf amplifier A15 (*a* above).

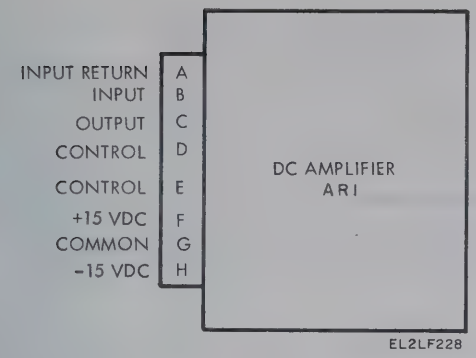


Figure 3-111. Dc amplifier AR1, input and output characteristics.

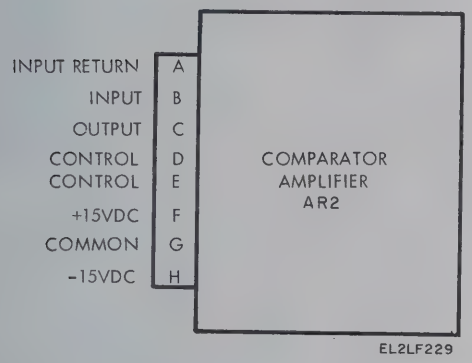


Figure 3-112. Comparator amplifier AR2, input and output characteristics.

3-38. Primary Power Distribution, Circuit Analysis.

(fig. 3-114 through 3-118 and FO 3-66 and FO 3-56)

a. The high voltage cage (2A3A11) circuitry is illustrated in figures 3-114 and FO 3-55; the wiring diagram of the primary power distribution panel (2A3A14) is shown in figure FO 3-56. The input and output signal characteristics for the various relays within the primary power distribution panel are shown in figures 3-115 through 3-117, respectively.

b. To simplify circuit analysis of input and output characteristics of relays within the primary power distribution panel, it is necessary to understand the operation of frequency sensing relay K3. Time delay control resistor R2 (fig. FO 3-56, sheet 4) is the major controlling factor in the sequential application of primary power to the AN/TSC-54. The resistance value of R2 determines the amount of time lapse before frequency sensing relay K3 will drop out, if the input line frequency to the equipment drifts outside the limits of 380 to 420 Hz.

c. The dropout time (*b* above) may be varied between 1.5 and 5.0 seconds. The resistance values given below will provide the delay periods as specified:

50K ohms = 1.6 seconds
300K ohms = 2.0 seconds
750K ohms = 3.0 seconds
1.2M ohms = 4.0 seconds
1.5M ohms = 5.0 seconds

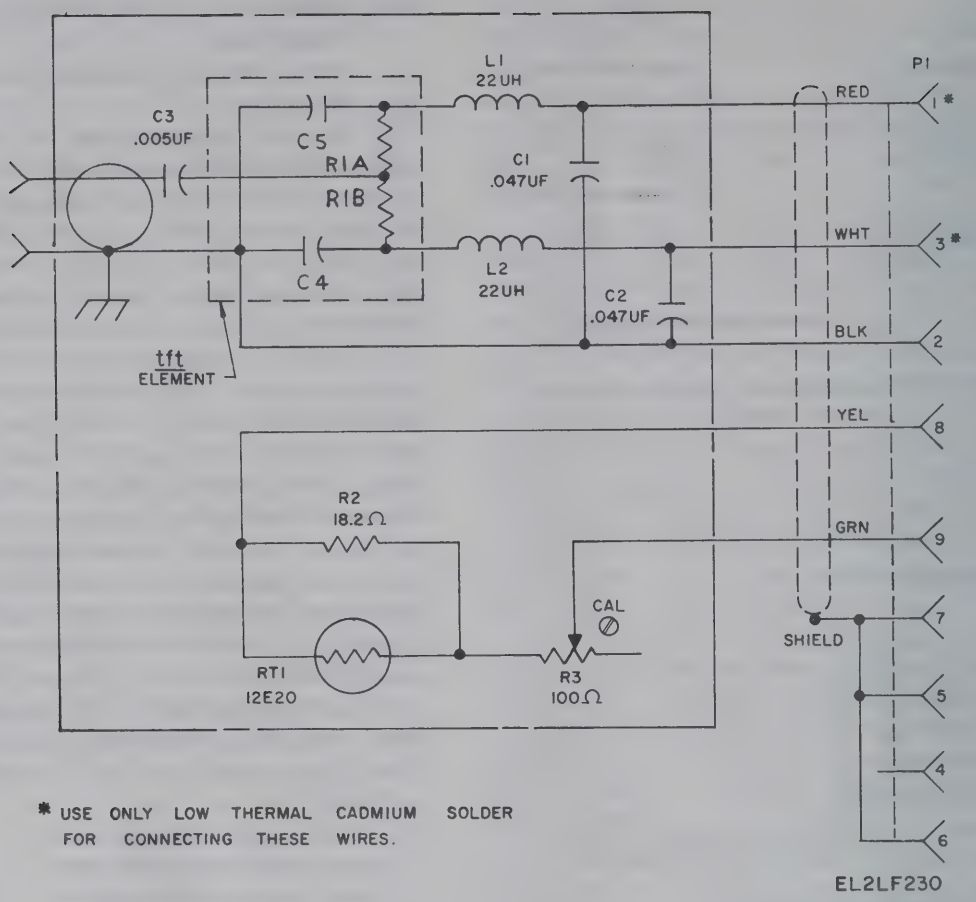


Figure 3-113. Rf head, schematic diagram.

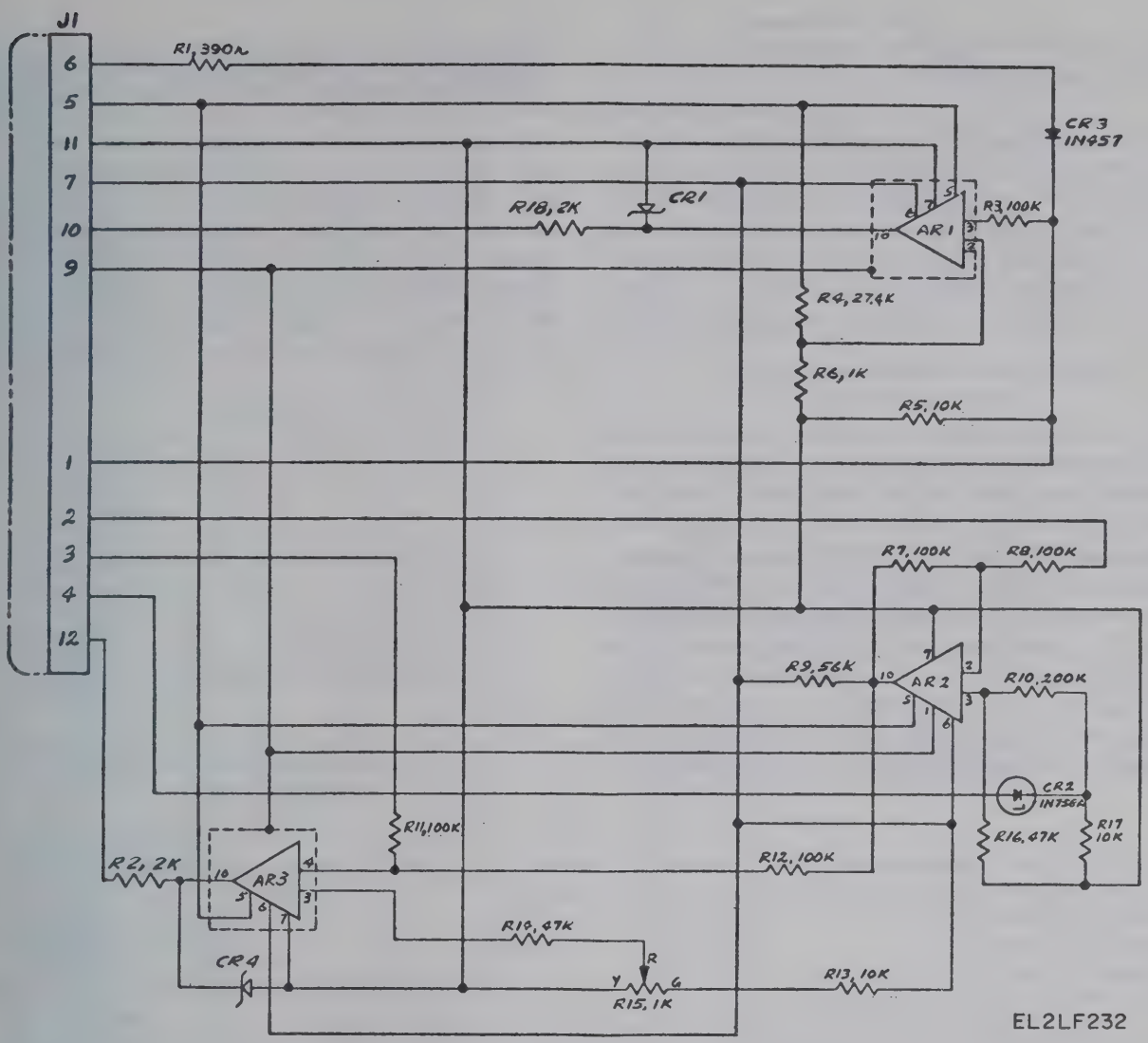


Figure 3-114. High voltage cage 2A3A11, component board, schematic diagram.

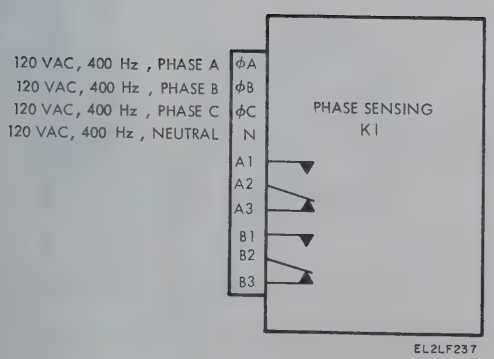


Figure 3-115. Phase sensing relay K1, signal characteristics.

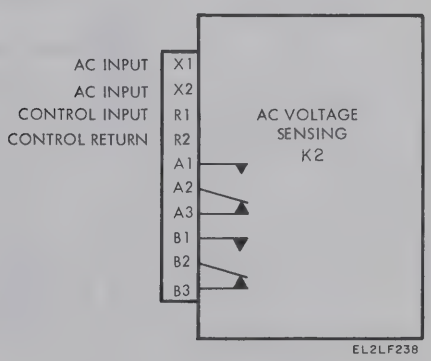


Figure 3-116. Ac voltage sensing relay K2, signal characteristics.

NOTE

Resistance values below 50K will give a time delay factor of 1.5 seconds.

d. The solid state contactor is a high-speed switch which operates 100 milliseconds faster than beam power supply contactor K1 (fig. 3-119), applying ac

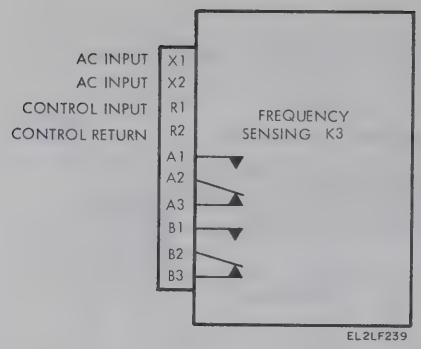


Figure 3-117. Frequency sensing relay K3, signal characteristics.

power through limiting resistors R11, R12 and R13. The limiting resistors prevent current surges. Ac power is applied to the solid state contactor through pins A and B where it is transformed, rectified and filtered to supply +10 vdc to the light coupled isolator U1. When the BEAM POWER ON switch is activated, +28 vdc is applied through pins D and E to the light source in the isolator. The isolator is activated by the light from the light source and fires Q1. When Q1 is on, current flows through the bridge rectifier and alternately turns on T1 and L1 closing the circuit, thus, allowing ac to flow between pins A and B. Removal of the 28 vdc control voltage will deactivate the contactor.

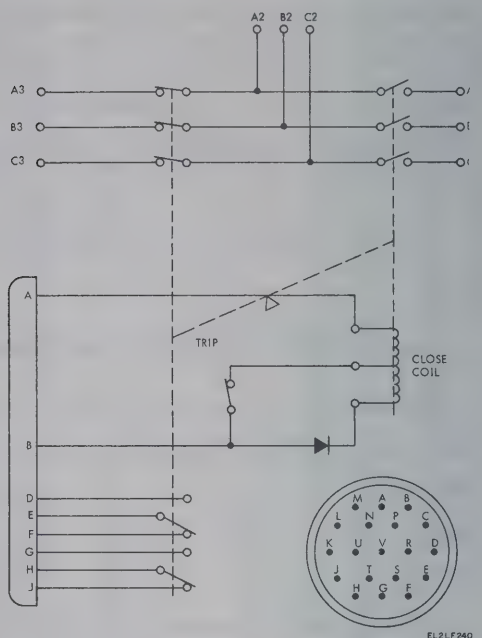


Figure 3-118. Primary power contactor K4, schematic diagram.

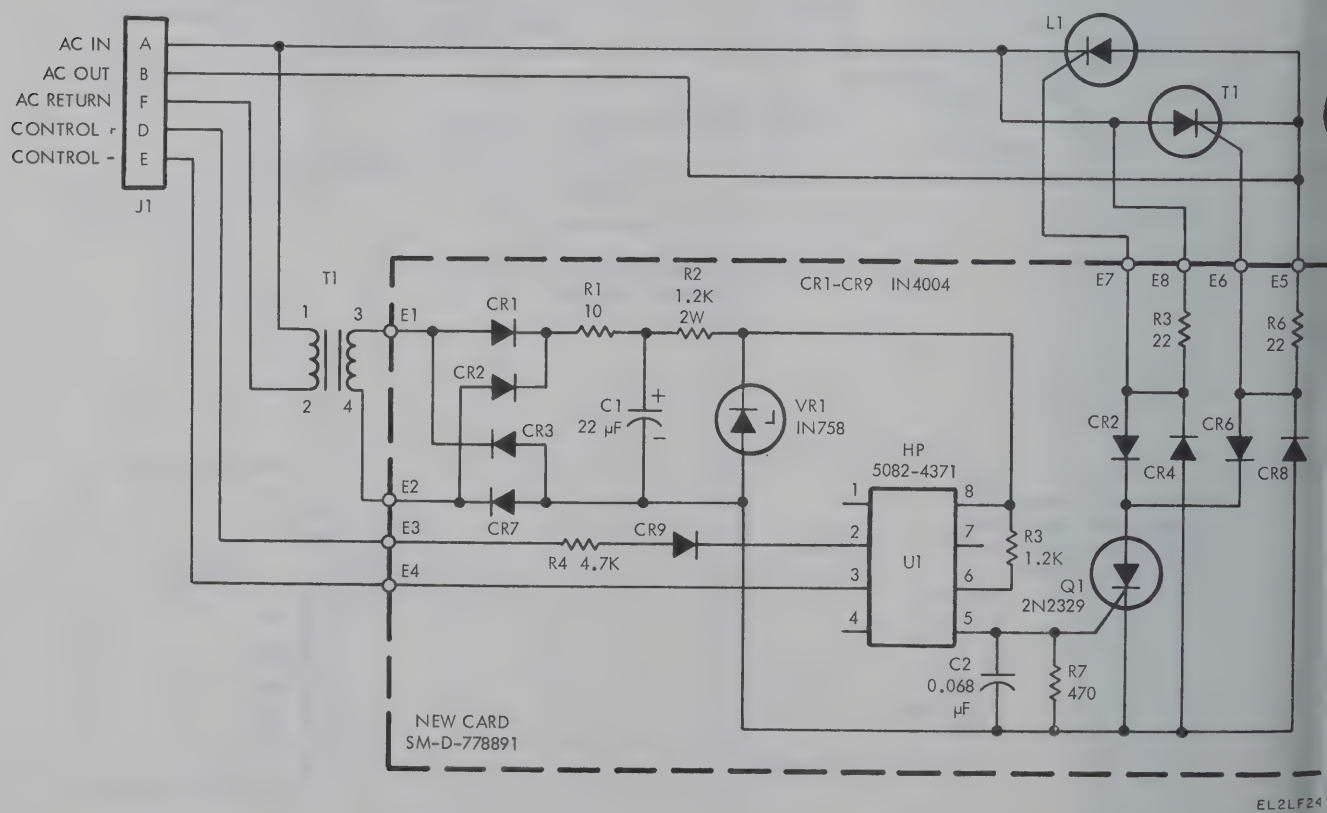


Figure 3-119. Solid state contactor, schematic diagram.

3-39. Servo Amplifier 2A3A17/A18, Circuit Analysis.

(fig. 3-120 through 3-126 and FO 3-57)

Servo amplifier A17/A18 (fig. 3-120) provides the necessary power to drive and control the azimuth and elevation drive motor assembly. The scr amplifier (*a* and *c* below) receives the input control signal from the associated azimuth or elevation position loop amplifiers. Two phase ac power is used to drive a bridge rectifier circuit consisting of diodes CR4 through CR7 which supplies the field

current for the drive motors of the antenna. The circuit for the magnetic field coils is completed through a relay (K5) which, when energized, completes the +28 vdc circuit to the amplifier output control relay (K1). Relay K2 is connected across the 120 vac input to the power amplifier and its contacts are connected in series with the system interlock contacts of relays K2 and K5. Relay K3, when energized by the standby command signal, applies power from the bridge rectifier to the antenna brake mechanism. The various modes of operation which relate to the switching and control functions of the servo amplifier are covered in the functional diagram analysis.

a. The dc power amplifier (fig. 3-121) consists of an input filter, a low voltage transformer, a dc amplifier with two banks of output transformers, a crossfire protection circuit, associated silicon-control rectifiers (scr) and two scr delta voltage/delta time (dv/dt) filters. The detailed circuit analysis for these circuits is covered in *b* and *c* below.

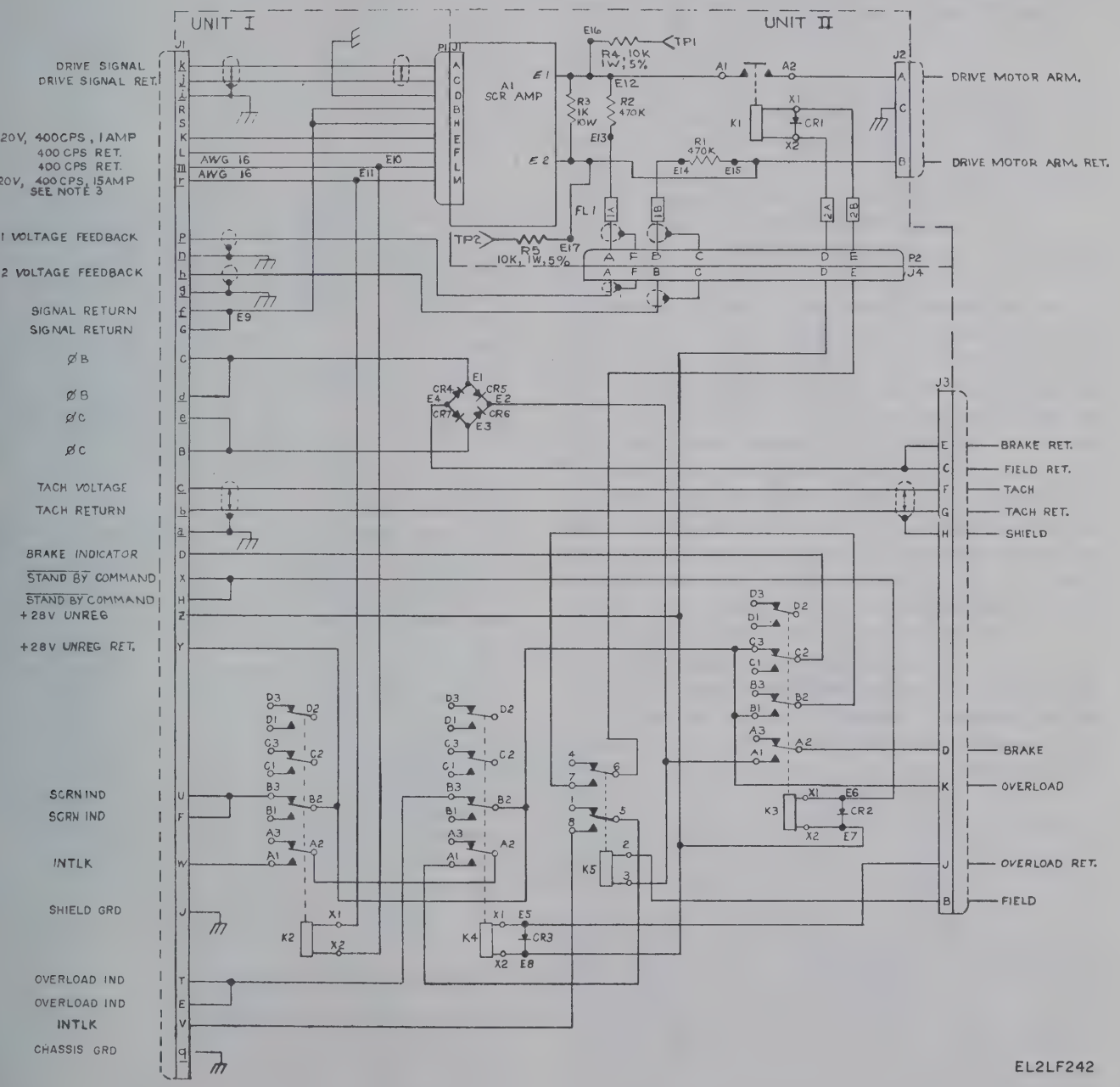


Figure 3-120. Servo amplifier A17/A18, schematic diagram.

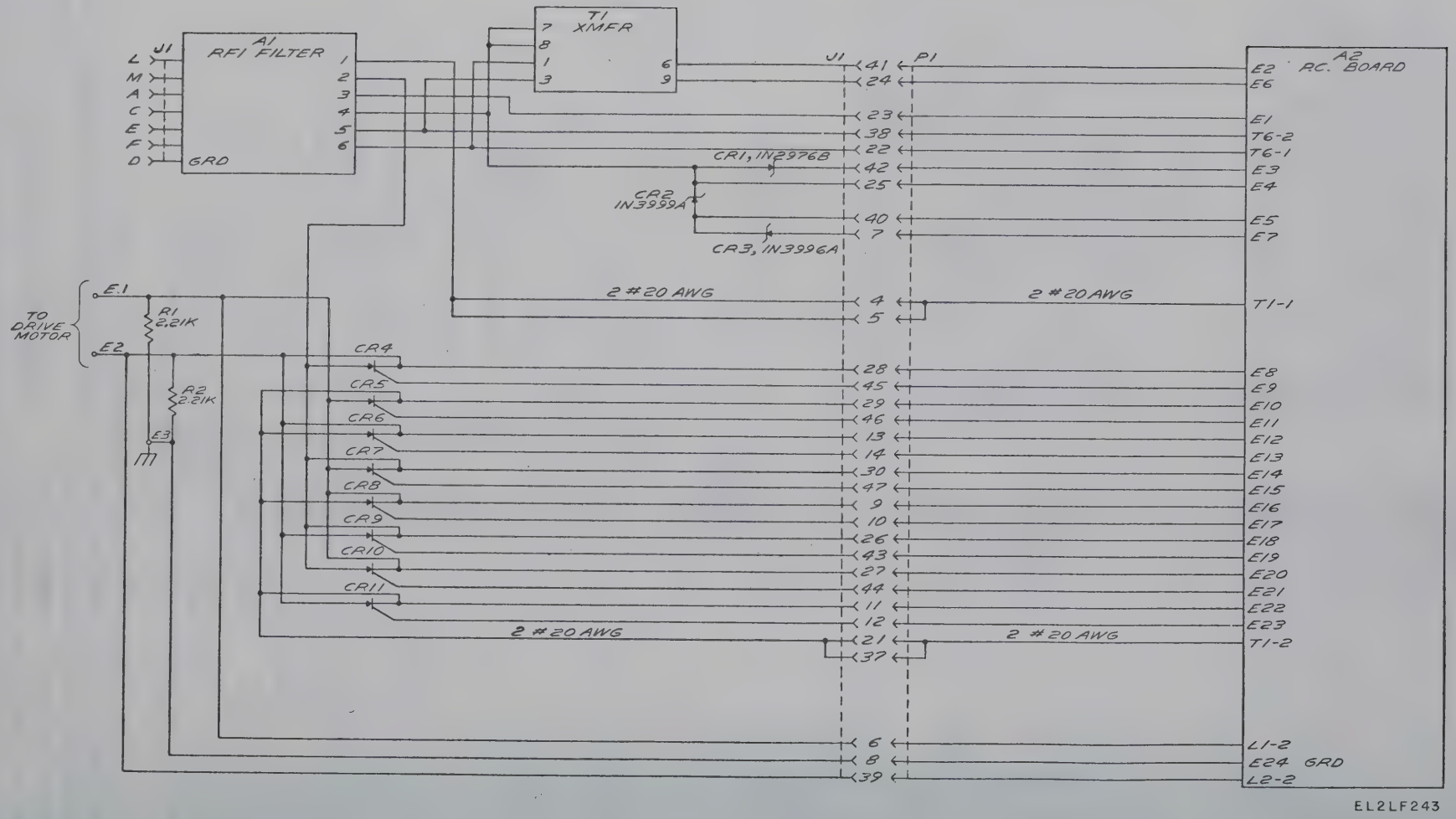


Figure 3-121. Dc power amplifier A1, schematic diagram.

b. Rfi filter A1 (fig. 3-122) consists of three filter sections which provide filtering for the 120 vac, 400 Hz input and the drive signal (+10 vdc) inputs to the dc amplifier. The 120 vac inputs are applied to the input pins L, M, E, and F of connector J1 with outputs at pins 2 and 5, respectively. Connector J1-L, J1-F, pins 1 and 5, are the filter return connections. The drive signal (±10 vdc) is applied through input pins A and C of connector J1 with the output at pins 3 and 4. Connector J1-C and pin 4 are the filter return leads.

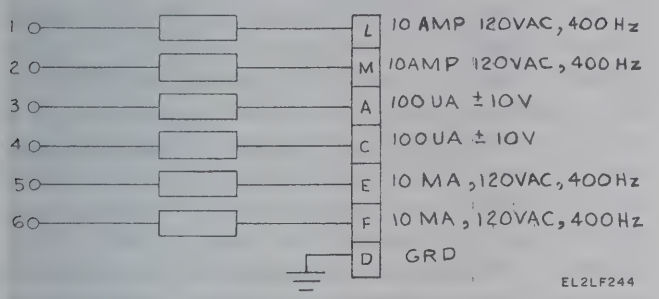


Figure 3-122. Rfi filter, schematic diagram.

c. Dc power amplifier A2 (fig. FO 3-57) receives, as an input, the drive signal from the antenna control circuits. It processes the drive signal to produce control pulses of current to the antenna drive motor. The circuit consists of an input differential amplifier module (*d* below), three double-ended constant current transistor stages, two banks of output transformers and associated silicon-controlled rectifier (*a* above), and an integrated logic synchronization circuit (*e* below).

(1) The control signal input is applied through resistors R3 and R4 to one of the inputs of the differential amplifier. Two back-to-back Zener diodes hold the input signal level from exceeding ±10 volts. The positive and negative voltages for operation of the differential amplifier and double-ended transistors are derived from the low voltage rectifier circuit which is connected through connector pins 41 and 24 to the secondary of the transformer. The outputs of the differential amplifier (pins 8 and 5) drive the bases of transistor Q1. Resistors R10 and R16 are the collector load resistors for Q1 and the output developed across them drives the bases of transistor Q2. The collector circuits of transistor Q2 are connected through switching networks to the bases of transistor Q3. The networks consist of switching diode CR8, capacitor C2, diode CR9 and capacitor C4.

(2) The collectors of transistor Q2 are connected through diodes CR12 and CR13 to the collector of transistor Q6. The base of transistor Q6 is driven by the collector of transistor Q7. The dc voltage that drives the base of transistor Q7 is derived by sensing the load current through the primary of transformer T1. The synchronizing signal is applied through double-ended transistor Q4 to the collectors of transistor Q2. Additional signals applied through connector pins 15 and 31 to the bases of Q4 are derived from the crossfire protection circuit. These signals reverse bias the proper base of Q4 to ensure proper phasing of the signals being applied to the collectors of Q2. The outputs of the switching networks drive the bases of transistor Q3. The collector load for one section of transistor Q3 consists of the primary windings of transformers T2 and T3 and the collector load for the other section of transistor Q3 consists of the primary windings of transformers T3 and T4. Diodes CR4 and CR5 in the collector circuits of transistors Q3 prevent the voltage at the collector from being driven excessively positive when magnetic fields in the primary winding of the transformer collapses.

(3) Silicon-controlled rectifiers are connected across each of the transformer secondary windings. The output connections of the silicon rectifiers are arranged so that a negative or positive voltage is applied through terminal E1 and E2 to the drive motor. These connections and the output load resistors are shown in figure 3-121. Depending upon the control voltage input polarity, the unbalance on the base of constant current transistor Q2 will cause one or other of the switching networks to drive the respective base of transistor Q3. The resultant pulse of current through the associated primary windings results in firing the scr's connected across the secondary windings. This results in the proper polarity corrective voltage being applied to the antenna drive motor. As soon as the pulse of current (representing the amount of corrective angular movement of the antenna) ceases, the gate current to the scr's also ceases. The functional interconnections for the servo amplifier circuitry are shown on the antenna control functional diagram.

d. Differential amplifier integrated circuit A1 receives the drive signal from the antenna control system as shown on the schematic diagram (fig. 3-122). The circuit consists of a five transistor configuration. Inputs are applied to pins 1 and 4 with outputs at the dual collector leads (pins 8 and 5). The positive supply voltage is connected to pin 7 and the negative supply voltage to pin 3. In this application, the drive signal is applied to input pin 1 with input pin 4 referenced through resistor R9 to the signal return line. Transistor Q3 provides a constant current which under quiescent conditions divides equally through the 50-ohm emitter resistors of the amplifiers. The base of the constant current source transistor Q3 is connected through resistor R1 and pin 2 to a reference potential to provide the constant bias required. When an input signal is present at pin 1, the current through transistor Q1 and collector resistor R2 increases or

decreases correspondingly. The outputs at pins 8 and 5 are therefore proportional to the swing of the input signal around the reference level. Offset voltages are fed back (in the overall circuit) through capacitors to maintain the desired level and stabilization. The outputs are fed to the servo amplifier circuit as discussed in *c* above.

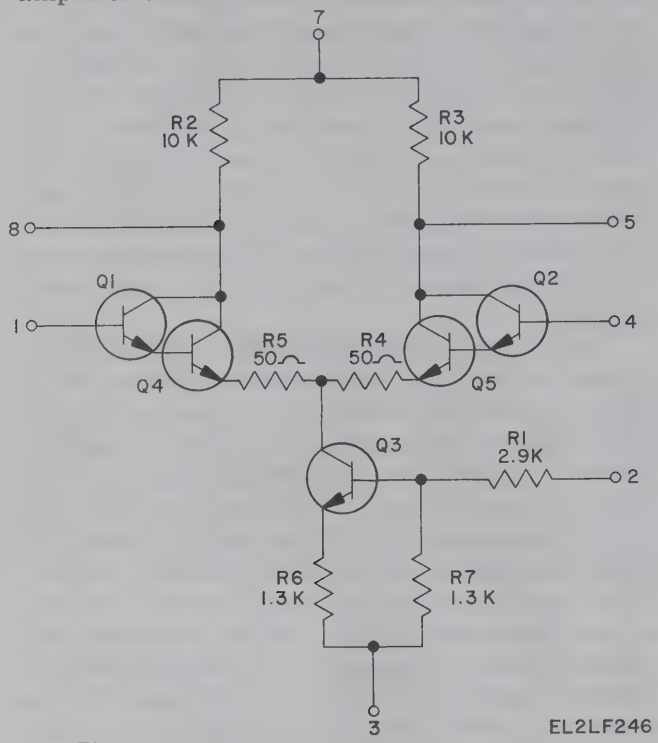


Figure 3-123. Differential amplifier integrated circuit, schematic diagram.

e. The diode transistor logic nand gate integrated circuit (fig. 3-124) is used in the scr amplifier. It provides the synchronization reference for the control transistors in that circuit. Two groups of four each of these gates are configured as shown on figure FO 3-57. A basic circuit of one of these gates is shown on the schematic diagram (fig. 3-124) and consists of two input steering diodes, two series-connected base bias diodes and an output npn transistor. With a high (positive voltage) at the inputs the steering diodes are reverse biased and the two base load diodes are forward biased from the positive supply voltage. Current flowing through the base bias resistor of the transistor forward biases the transistor and the collector output drops to ground reference or low. When a low (negative voltage) is applied to either of the steering diodes they are forward biased and current flowing through the resistor to the positive supply voltage, reverse biases the base diodes and the transistor is cut off. The output rises to the collector voltage. In the configuration used for the acr amplifier synchronization circuit, the voltages from the collector circuits of the associated transistors are applied as inputs to four of the gate circuits. Since the reference voltages are developed from the 120 vac input and scr amplifier synchronization circuit, the voltages from the collector circuits of the associated transistors are applied as inputs to four of the gate circuits. Since the reference voltages are developed from the 120 vac input and the scr outputs, the gating of the integrated circuit provides the timing sequence through the output transistor Q4.

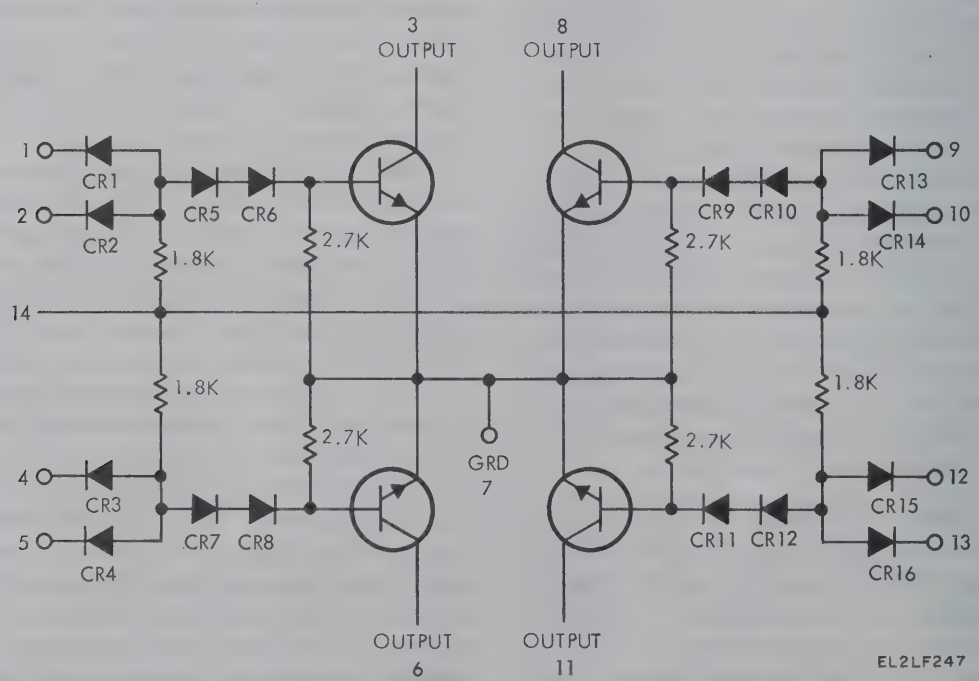


Figure 3-124. DTL NAND gate integrated circuit, schematic diagram.

f. The crossfire protection circuit (fig. 3-125) receives its input across diodes CR12 and CR13 to input E2 or across diodes CR14 and CR16 to input E5. The signal at E1 or E6 is applied to dc power amplifier A2 to ensure that the current pulses fire the proper scr's in the correct sequence.

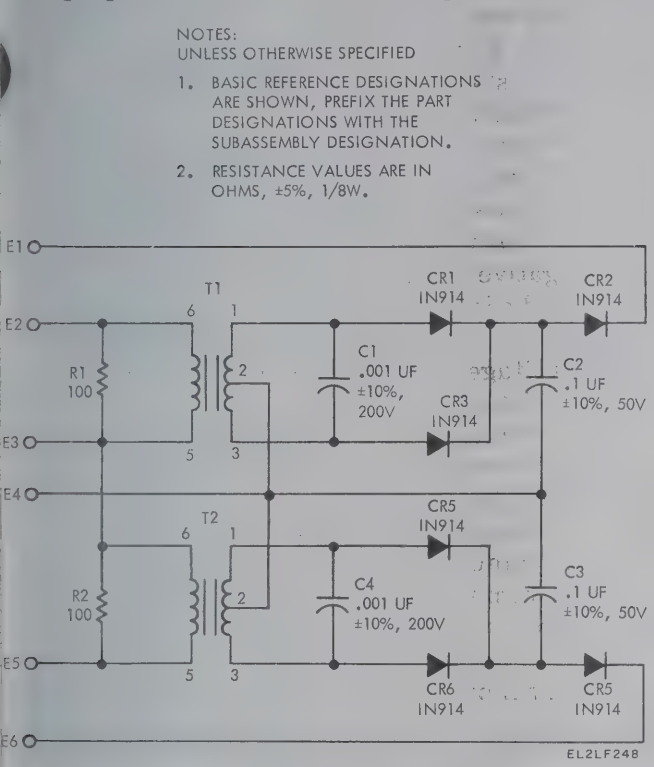


Figure 3-125. Crossfire protection circuit 2A3A18A1A3, schematic diagram.

(1) The protection circuit consist essentially of two identical sections, each containing a transformer T1 and T2, a half-wave rectifier composed of CR1 and CR3 or CR5 and CR6 along with filter capacitors C2 and C3. The resultant dc output voltage is present whenever current is flowing within scr bridge circuits. This voltage is applied to the bases of transistor Q4 located in the dc amplifier A2.

(2) The scr dv/dt filters A4 and A5 (fig. 3-126) provide isolation between the individual scr's. This circuit configuration prevents excessive current and subsequent damage to the scr's.

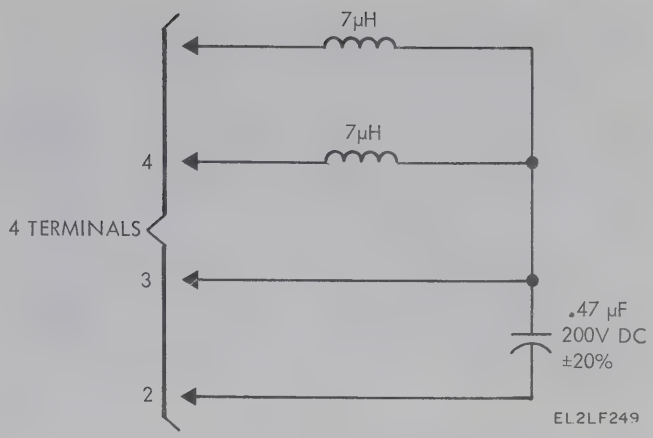


Figure 3-126. Scr dv/dt filter 2A3A18A1A5, schematic diagram.

3-40. High Voltage Plate 2A3A20, Circuit Analysis

(fig. 3-127 through 3-129)

The detailed circuit analysis for the components mounted on high voltage plate 2A3A20 are given in *a* through *c* below:

a. Magnet power supply A21 (fig. 3-127) furnishes the power for the electromagnet associated with the klystron power amplifier. Phase three power is applied to variable transformer T1. The output power is adjustable over a range from 95.5 volts rms to 114 volts rms by an adjustable dc voltage applied to terminal 4 of transformer T1. The output voltages are rectified by diodes CR1 through CR6. Electron flow is from terminal 4 of terminal board TB1, resistor R2, shunt resistor R3, pin B of connector J2, through the magnet and pin A of connector J2 to terminal board TB1-5. Breakdown diode CR7 prevents the voltage drop across resistor R2 from exceeding 5.6 volts. Resistor R3 is the shunt resistor for a current monitor connected across pins F and G of connector J3. Resistor R1 is connected across terminal board TB1. Component board assembly A1 monitors the magnet current and if the current flows below the proper amount, a low current output signal is applied through connector J3-E. Output voltage is 120 to 150 vdc as measured at test points TP4 and TP5.

Figure 3-127. Magnet power supply A21, schematic diagram.

b. The magnet power supply component board (fig. 3-128) consists of four resistors and a level detector assembly. Resistors R2 and R3 are connected between +28 volts and common pin 2. The 3-volt reference at the junction of resistors R2 and R3 is applied through resistor R4 to pin 3 of level detector assembly A1 and functions as the reference voltage. The signal input is applied across resistor R1 and biases pin 2 of level detector assembly A1. When the input signal is greater than 3 volts (magnet current greater than six amperes), the output at pin 4 is 0 volts. When the input signal falls below 3 volts, 1 mA is applied through pin 4. The input signal is generated across resistor R2, applied through the fault test switch on the transmitter control panel, and returned to the magnet power supply component board.

c. Variable power transformer T1 (fig. 3-129) provides a methof of adjusting the three-phase power. The transformer is a double wye with saturable reactors in each output leg. Three-phase, 208-volt, 400-Hz power is applied to the wye-connected primary windings. The primary is isolated from the secondary by shielding. The voltage from the primary is stepped down by the secondary and the voltage between each of the secondary legs is adjustable over a range between 95.5 volts rms and 114 volts rms. This is accomplished by applying an adjustable dc voltage across terminals 4 and 5 to vary the current through the three saturable reactors.

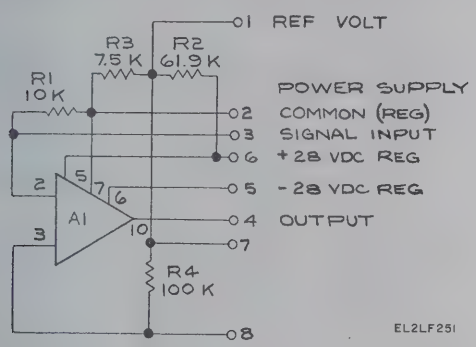


Figure 3-128. Magnet power supply component board, schematic diagram.

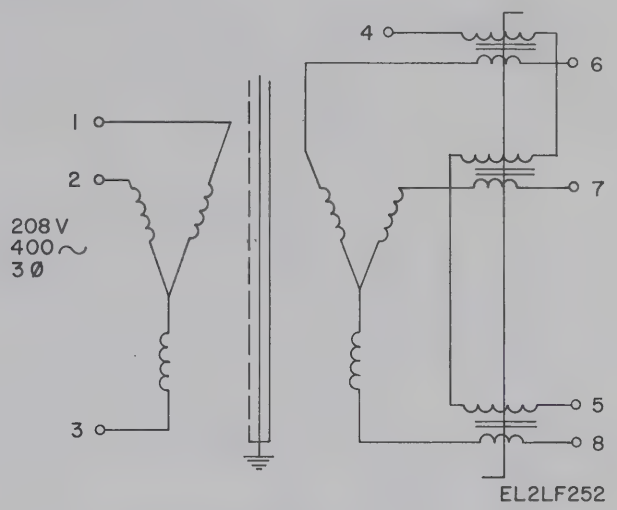


Figure 3-129. Variable power transformer T1, schematic diagram.

3-41. Azimuth Drive Assembly 2A3A22, Circuit Analysis

(fig. 3-130 through 3-135)

The azimuth and elevation synchro and limit switch assemblies are illustrated in figures 3-130 and 3-134, respectively. The azimuth and elevation resolver and gear box assemblies are shown in figures 3-131 and 3-135, respectively. The azimuth synchro and gear box assembly is illustrated in figure 3-132 and drive motor B1 is shown in figure 3-133.

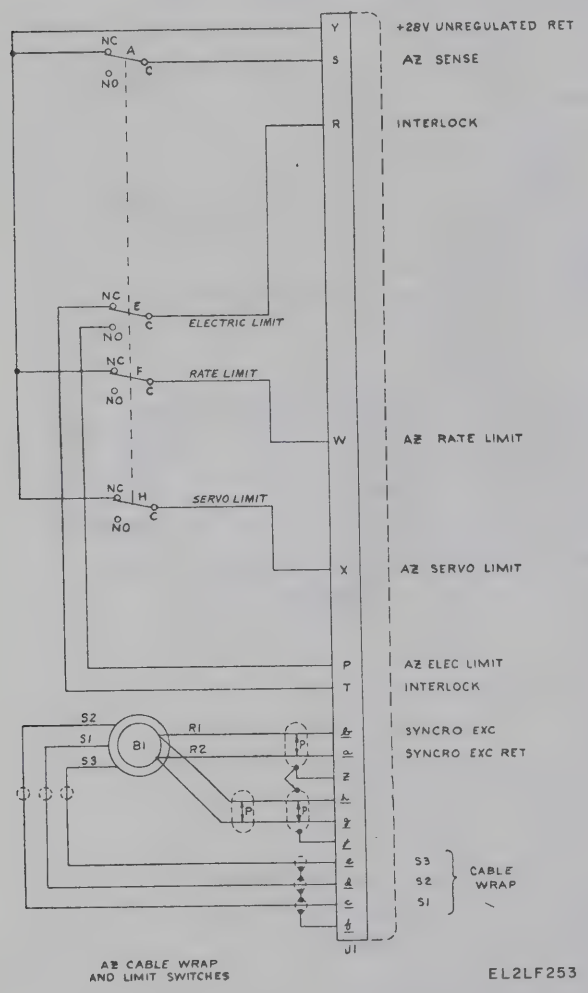


Figure 3-130. Azimuth synchro and limit switch assembly, schematic diagram.

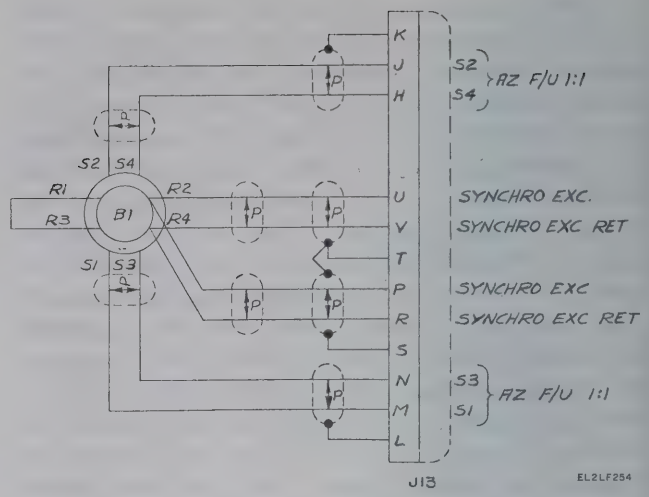


Figure 3-131. Azimuth resolver and gear box assembly, schematic diagram.

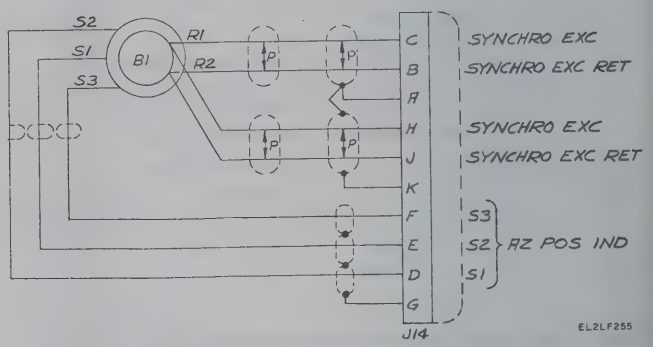


Figure 3-132. Azimuth synchro and gear box assembly, schematic diagram.

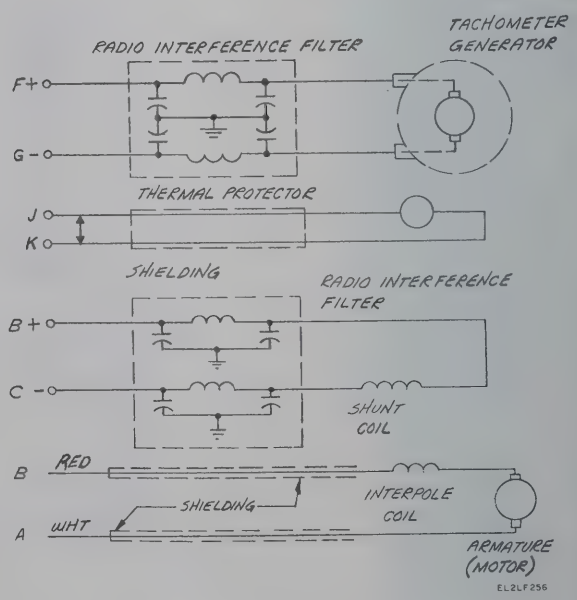


Figure 3-133. Drive motor B1, schematic diagram.

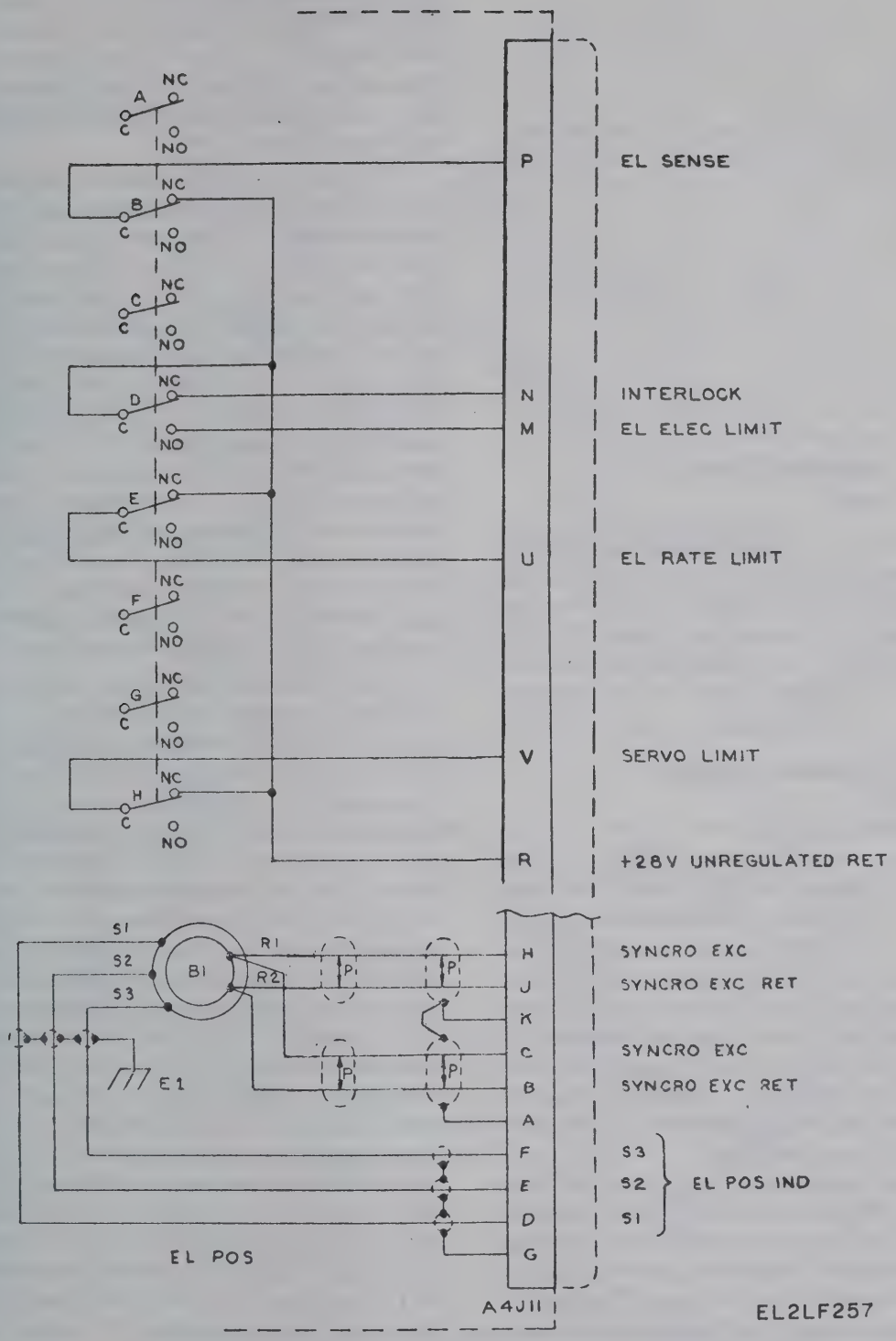


Figure 3-134. Elevation synchro and limit switch assembly, schematic diagram.

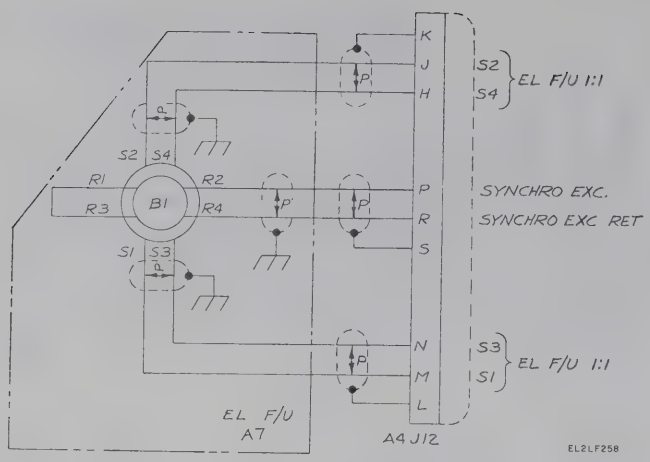


Figure 3-135. Elevation resolver and gear box assembly, schematic diagram.

3-42. Rf Box Assembly 2A9A1.

(fig. FO 3-58)

The rf box assembly contains the parametric amplifiers, twt amplifiers and associated waveguide switches. The relationship of rf box assembly components is shown on figure FO 2-1, sheets 1 through 4. For additional information on the parametric amplifiers, refer to TM 11-5820-819-30&P.

3-43. Azimuth-Elevation Scanner Assembly.

(fig. 3-136 and 3-137)

The azimuth/elevation scanner circuit receives the four timed scan pulses derived from the scan generator. These input timing pulses are amplified and are used to synchronize the tracking error signals with the modulation taking place in the microwave assembly. The circuit essentially consists of four transistor driver stages and associated phase shifting transformers and a temperature control circuit. The four driver stages of the scanner signals will be discussed prior to the discussion of the temperature control circuit.

a. The tuned driver signals consist of positive-going square wave pulses each of 10 milliseconds duration with 30 milliseconds between the leading edge and trailing edge. When the leading edge of the wave-train is applied to the base of transistor Q4, transistor Q4 conducts and a pulse of current flows through the lower winding of the primary of transformer T2. This induces a current flow in the secondary w'nding and in ferrite transformer assembly T3, tl ereby inducing a magnetic field in that assembly. After 10 milliseconds the pulse drops to zero and coincidently, the leading edge of the pulse at the input of transistor Q3 is turning that transistor on.

b. The pulse of current through the upper winding of the primary of transformer T2 indicates a magnetic field of opposite polarity in the ferrite transformer assembly. At the end of 10 milliseconds the pulse drops to zero and coincidently the leading edge of the pulse at the input of transistor Q2 is turning that transistor on. The pulse of current from the collector of transistor Q2 flows in the associated primary winding inducing a magnetic field in transformer T3. When the pulse is decaying, the pulse at the input of transistor Q1 causea a pulse of current in the upper winding of transformer T1 and a resultant magnetic field of opposite polarity. The cycle now repeats and the overall result is that the induced voltage causes two states of phase status; 0 degrees and 180 degrees in the microwave assembly.

c. The temperature control circuit consists of a balanced resistive bridge circuit, a unijunction transistor and an scr heater element. Thermistor R18 forms one arm of the bridge circuit and trsnsistor Q5 is the load across the bridge. When the temperature is normal, the bridge is balanced and transistor Q5 is cut off. Under this condition, the unijunction transistor Q6 is also cut off and the scr receives no gate voltage and remain off. When the temperature is below normal, the resistance of thermistor R18 changes and the bridge becomes unbalanced. This causes transistor Q5 to be forward biased and capacitor C6 is charged through resistor R23 and transistor Q5. Since this conduction path is present only when diode CR1 is forward biased by the positive cycle of the ac input, capacitor C6 does not charge to the firing potential required for unijunction transistor Q6. Eventually the charge on capacitor C6 is sufficient to turn transistor Q6 on and the resulting current through resistor R25 fires the scr and heater current flows. As the temperature returns to normal, transistor Q5 cuts off and capacitor C6 discharges through the unijunction transistor.

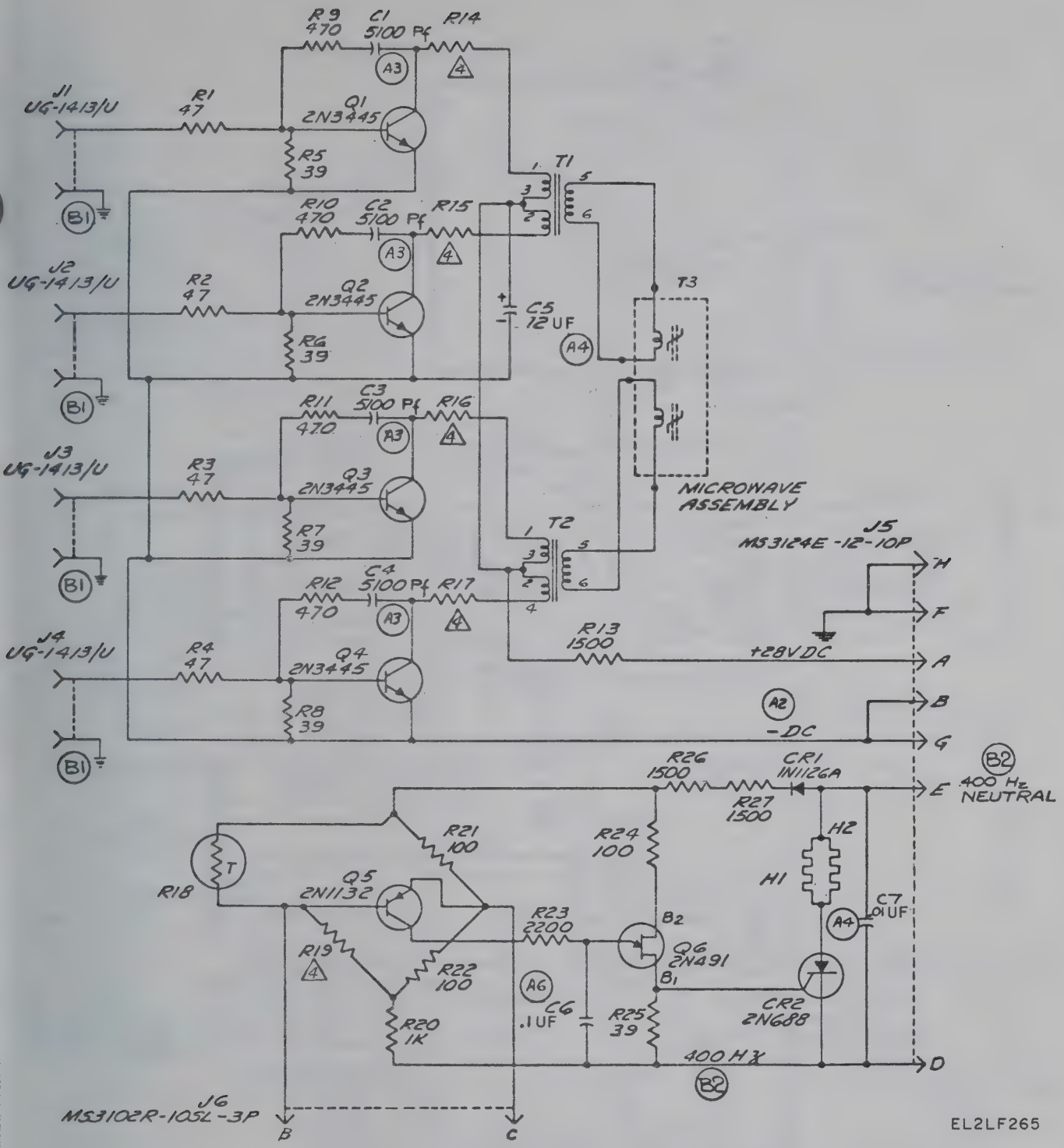


Figure 3-136. Azimuth/elevation scanner assembly, schematic diagram.

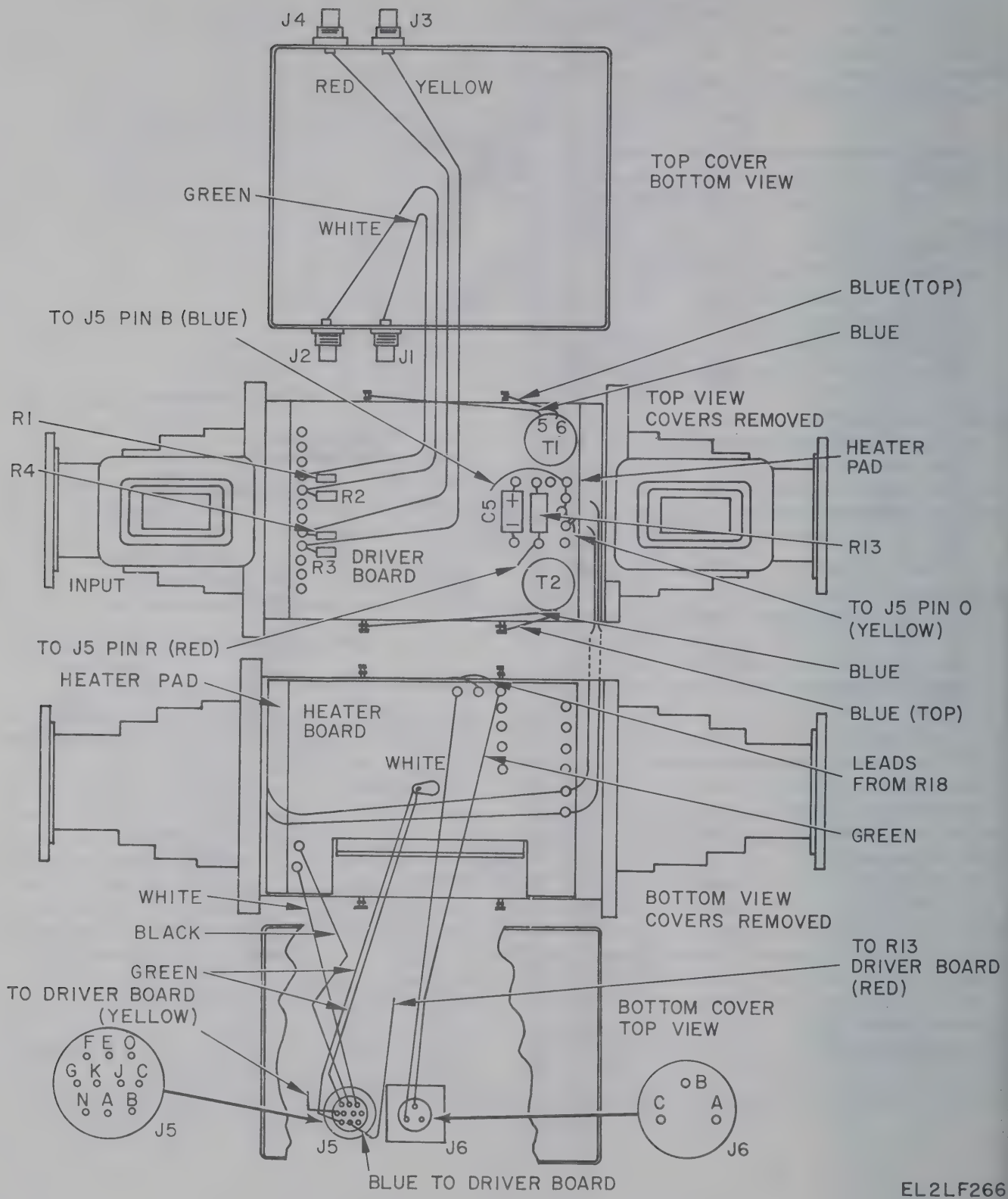


Figure 3-137 ①. Azimuth/elevation scanner assembly, wiring diagram (sheet 1 of 2).

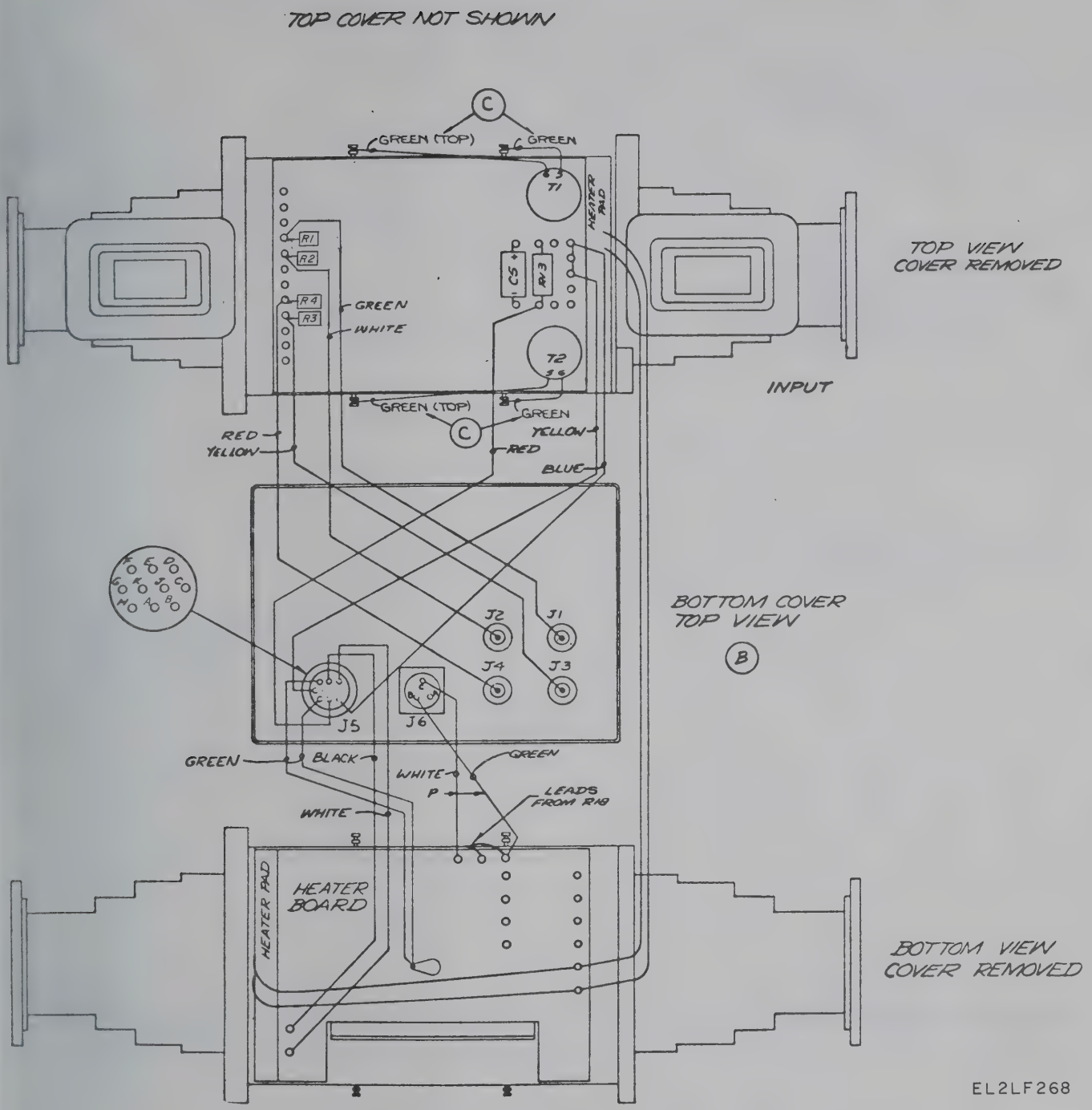


Figure 3-137. ②Azimuth/elevation scanner assembly, wiring diagram (sheet 2 of 2).

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TM 11-5840-340-12	23 Jan 74	Radar Set AN/PPC-76

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PAGE NO.	PARAGRAPH	FIGURE NO.	TABLE NO.	IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
2-25	2-28			Recommend that the installation antenna alignment procedure be changed throughout to specify a 2° IFF antenna lag rather than 1°. REASON: Experience has shown that with only a 1° lag, the antenna servo system is too sensitive to wind gusting in excess of 25 knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2° without degradation of operation.
3-10	3-3		3-1	Item 5, Function column. Change "2 db" to "3db." REASON: The adjustment procedure for the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.
5-6	5-8			Add new step f.1 to read, "Replace cover plate removed in step e.1, above." REASON: To replace the cover plate.
		F03		Zone C 3. On J1-2, change "+24 VDC to "+5 VDC." REASON: This is the output line of the 5 VDC power supply. + 24 VDC is the input voltage.

TYPED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER
SSG I. M. DeSpiritof 999-1776

SIGN HERE: SSG. I.M. DeSpiritof

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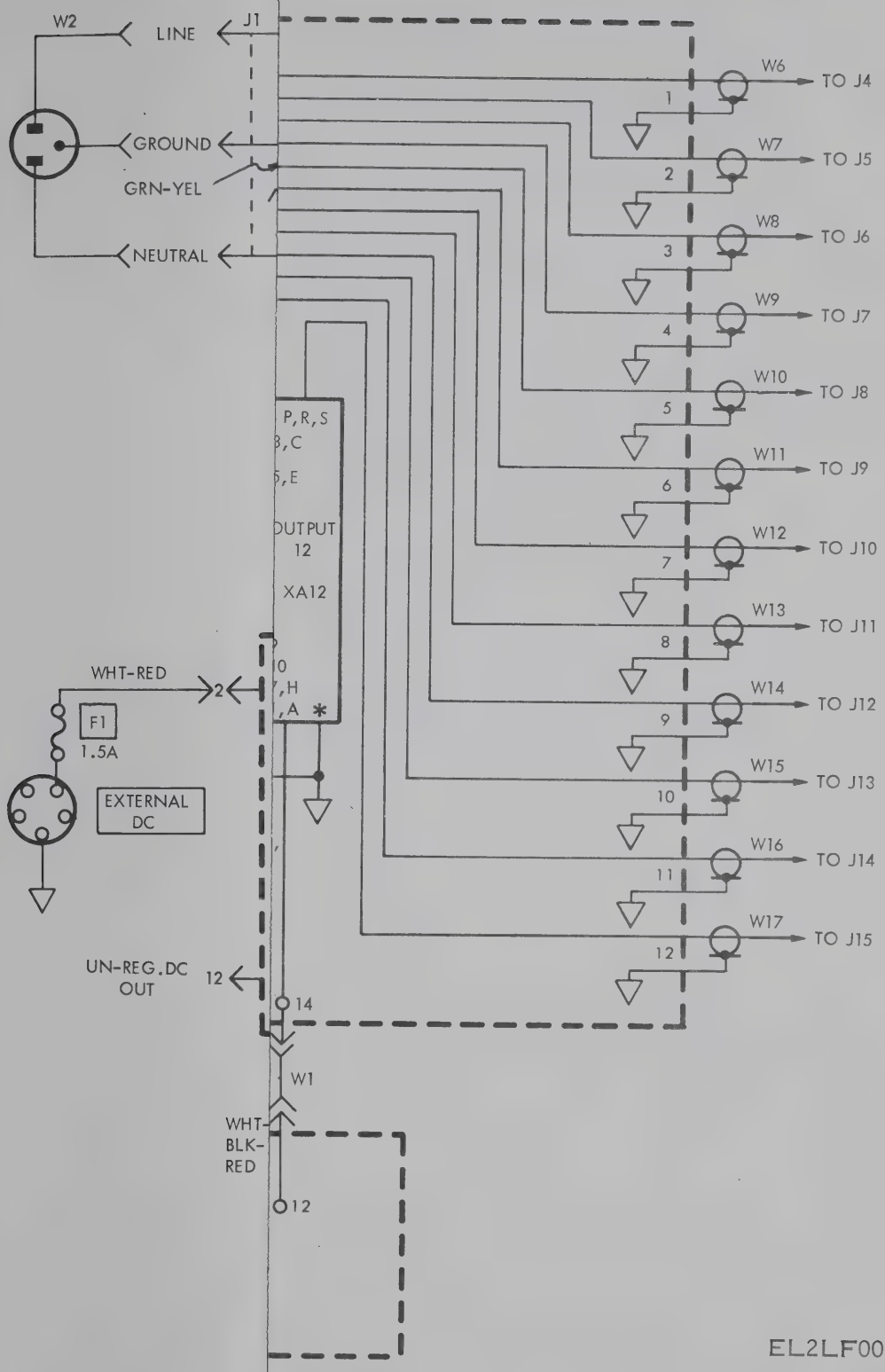
W2
LINE
J1
GROUND
GRN-YEL
NEUTRAL
W6
TO J4
W7
TO J5
W8
TO J6
W9
TO J7
W10
TO J8
W11
TO J9
W12
TO J10
W13
TO J11
W14
TO J12
W15
TO J13
W16
TO J14
W17
TO J15
P,R,S
,C
,E
UTPUT
12
XA12
WHT-RED
F1
1.5A
EXTERNAL
DC
UN-REG.DC
OUT
12
14
W1
WHT-
BLK-
RED
12
EL2LF006

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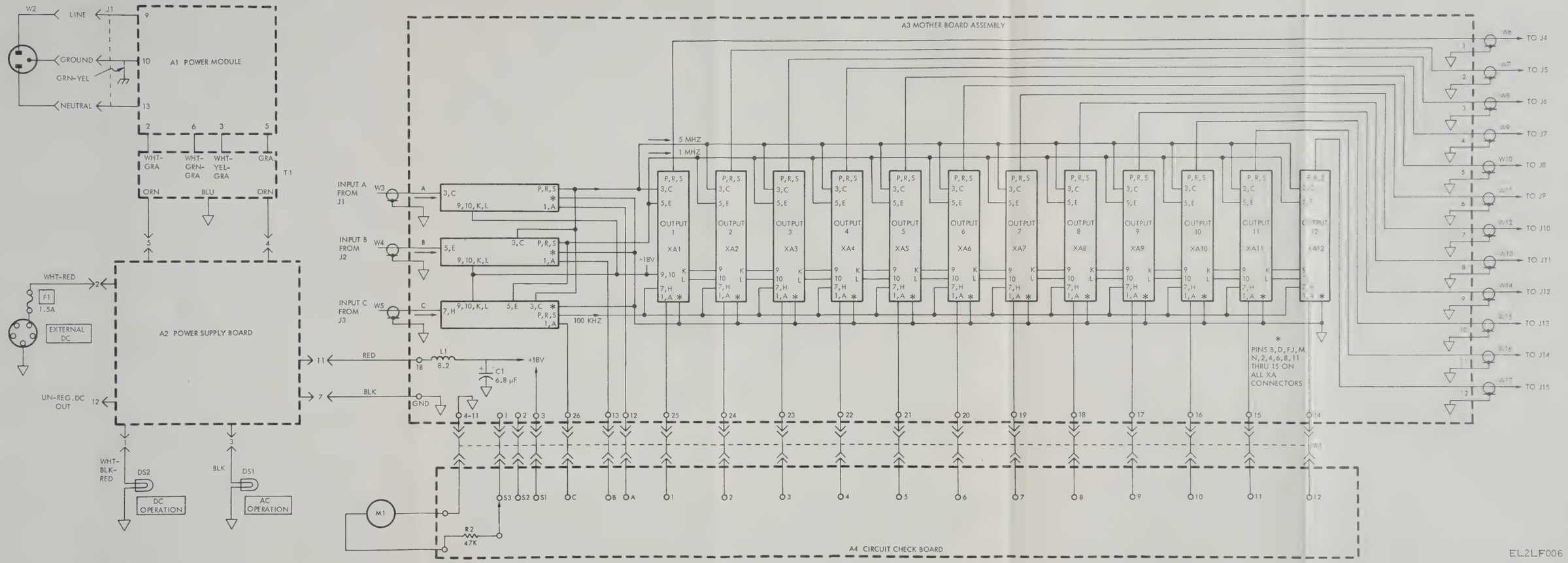
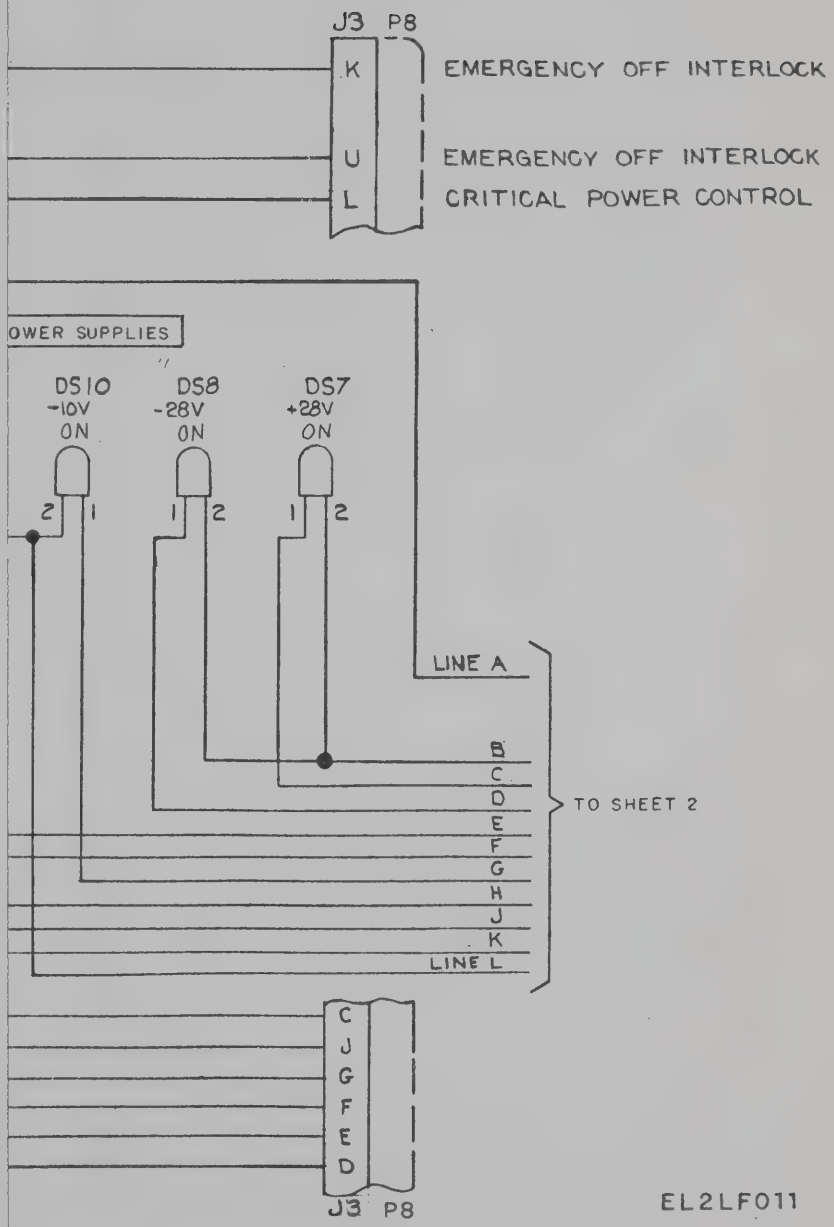


Figure FO 3-1. Distribution amplifier connection diagram.

'E DESIGNATION

OSITION.



EL2LF011

t 1 of 2).

NOTES:

1. PARTIAL REF DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION(S).
2. CIRCUIT BREAKERS ARE SHOWN IN CLOSED POSITION.
3. [ ] INDICATES EQUIPMENT MARKING.

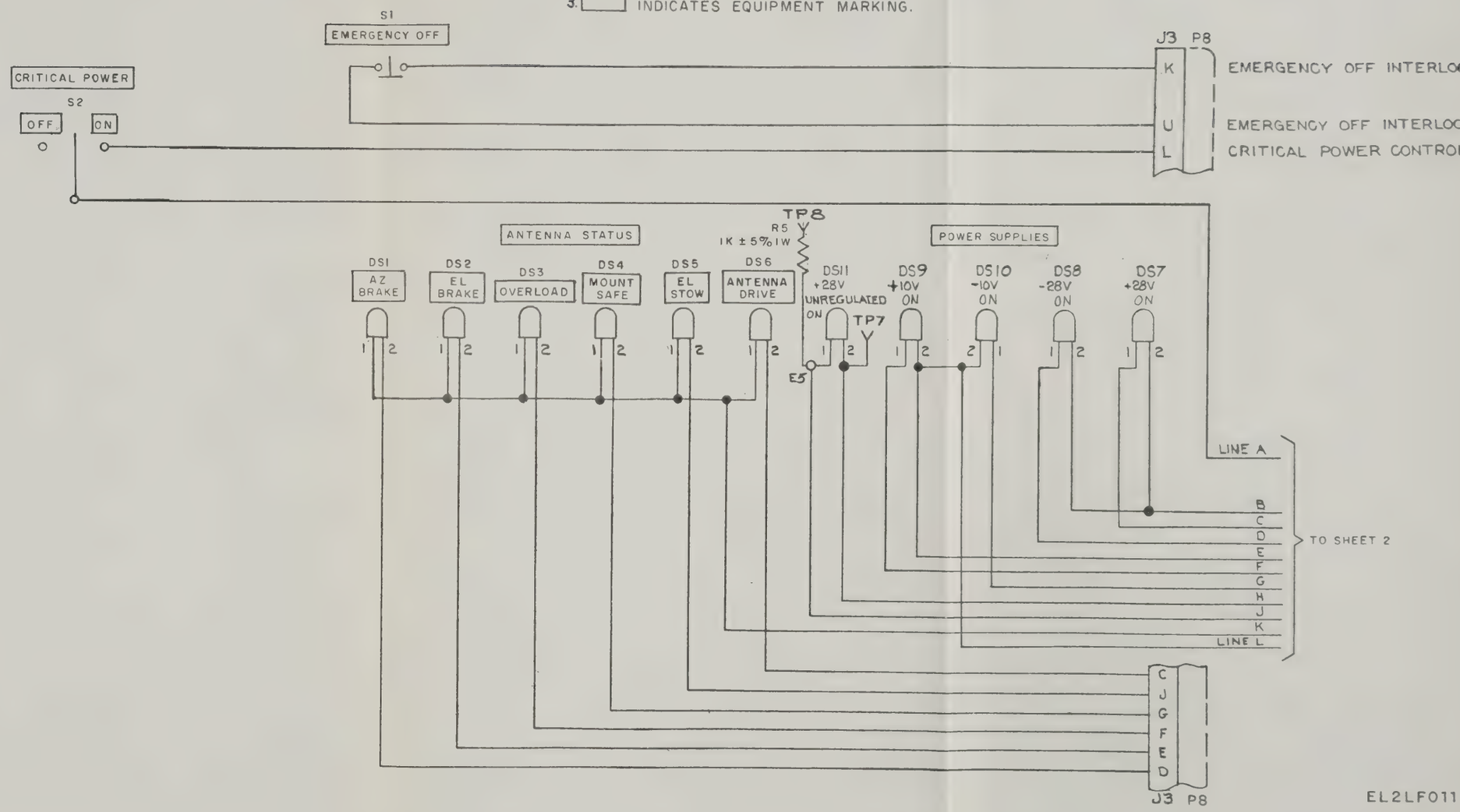
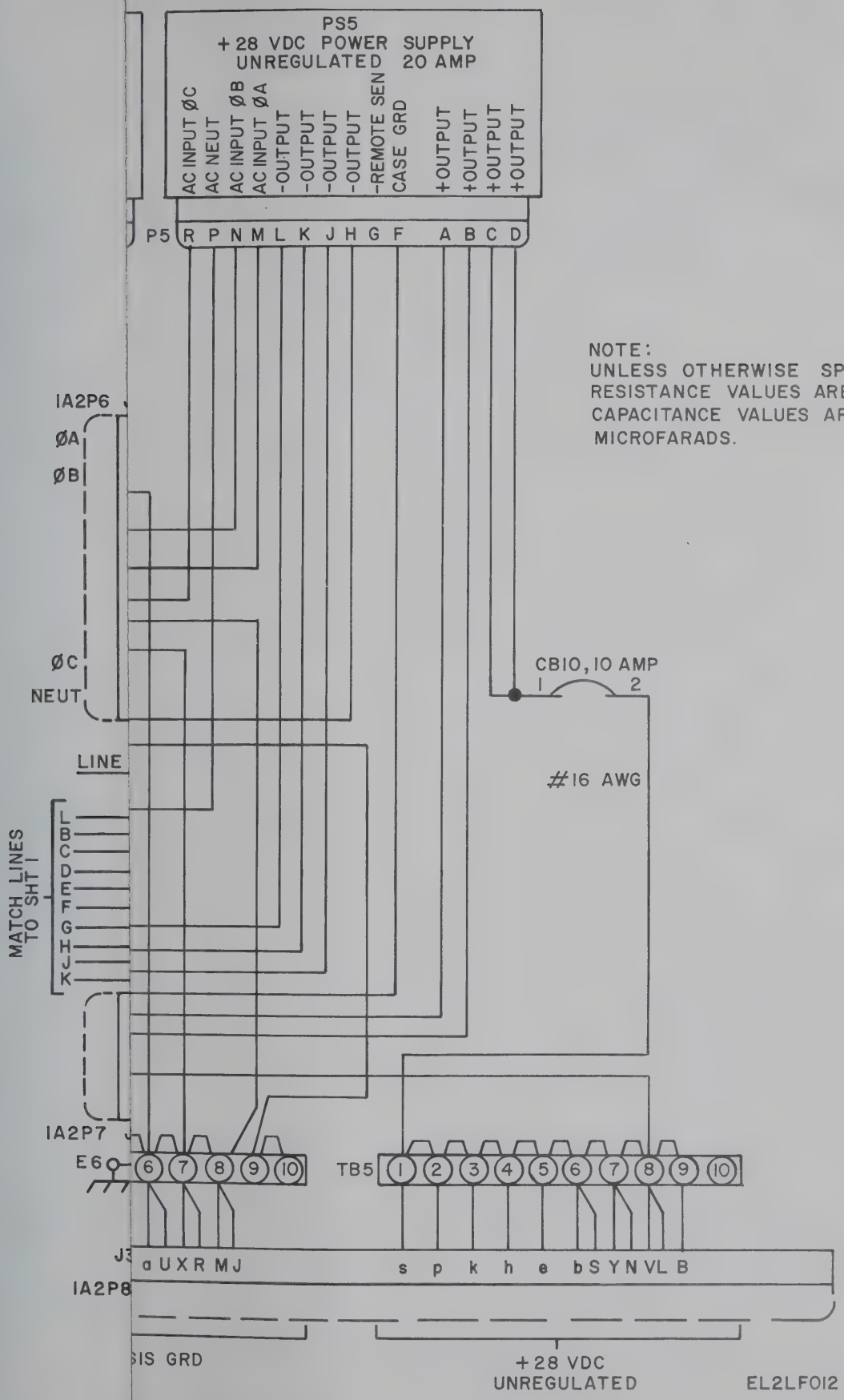
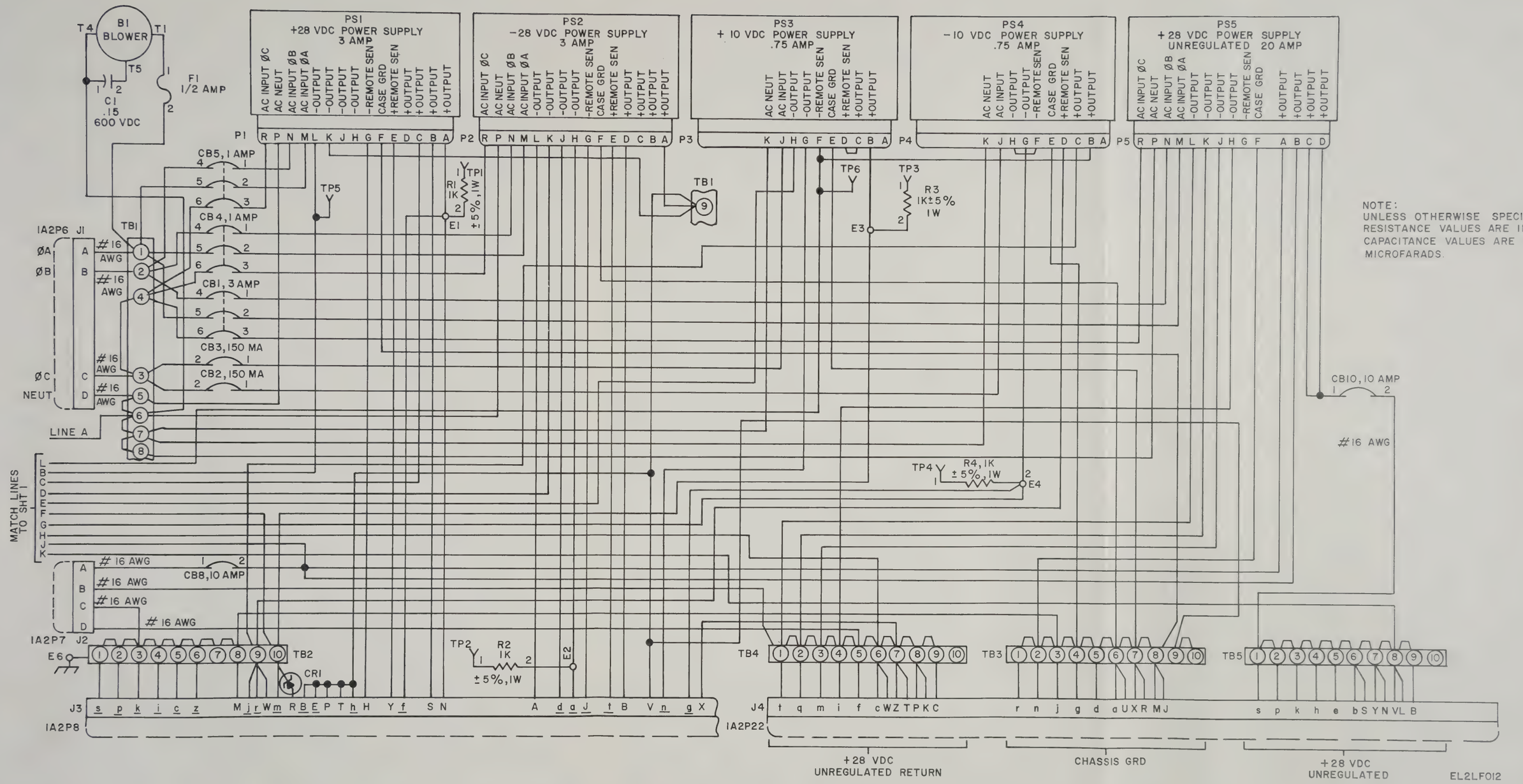


Figure FO 3-2. ① *Power distribution panel, schematic diagram (sheet 1 of 2).*


PS5
+28 VDC POWER SUPPLY
UNREGULATED 20 AMP
AC INPUT ØC
AC NEUT
AC INPUT ØB
AC INPUT ØA
-OUTPUT
-OUTPUT
-OUTPUT
-OUTPUT
-REMOTE SEN
CASE GRD
+OUTPUT
+OUTPUT
+OUTPUT
+OUTPUT
P5 R P N M L K J H G F A B C D
NOTE:
UNLESS OTHERWISE SPECIFIED;
RESISTANCE VALUES ARE IN OHMS,
CAPACITANCE VALUES ARE IN
MICROFARADS.
1A2P6
ØA
ØB
ØC
NEUT
LINE
CB10, 10 AMP
1
2
#16 AWG
MATCH LINES
TO SHT 1
B
C
D
E
F
G
H
J
K
1A2P7
E6
6 7 8 9 10
TB5
1 2 3 4 5 6 7 8 9 10
J3
a U X R M J
s p k h e b S Y N V L B
1A2P8
SIS GRD
+28 VDC
UNREGULATED
EL2LF012



NOTE:
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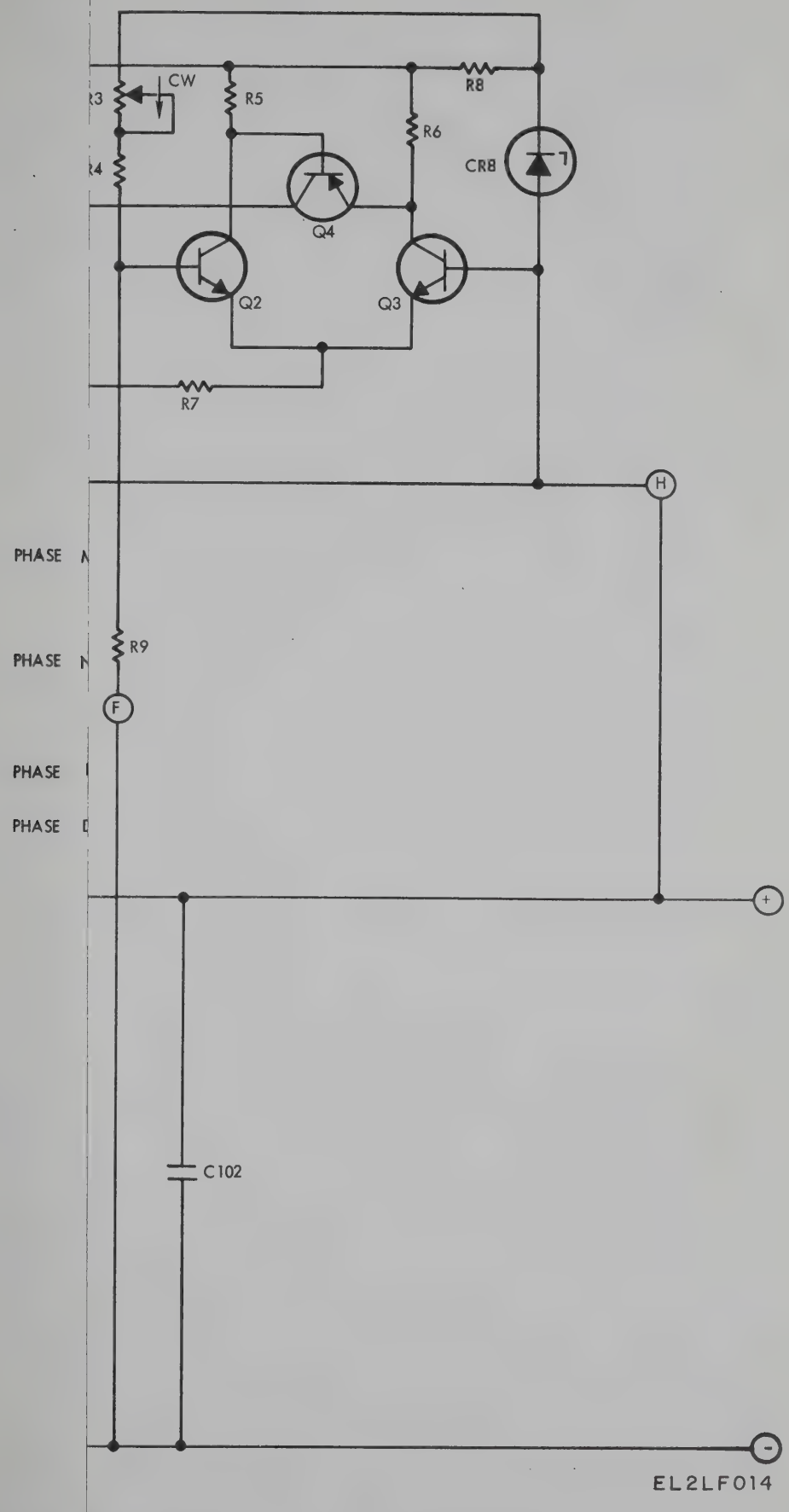
CAPACITANCE VALUES ARE IN
MICROFARADS.

Figure FO 3-2.③ Power distribution panel, schematic diagram (sheet 2 of 2).


CW
R5
R8
R6
CR8
Q4
Q2
Q3
R7
H
PHASE
PHASE
R9
F
PHASE
PHASE
C102
+
-
EL2LF014

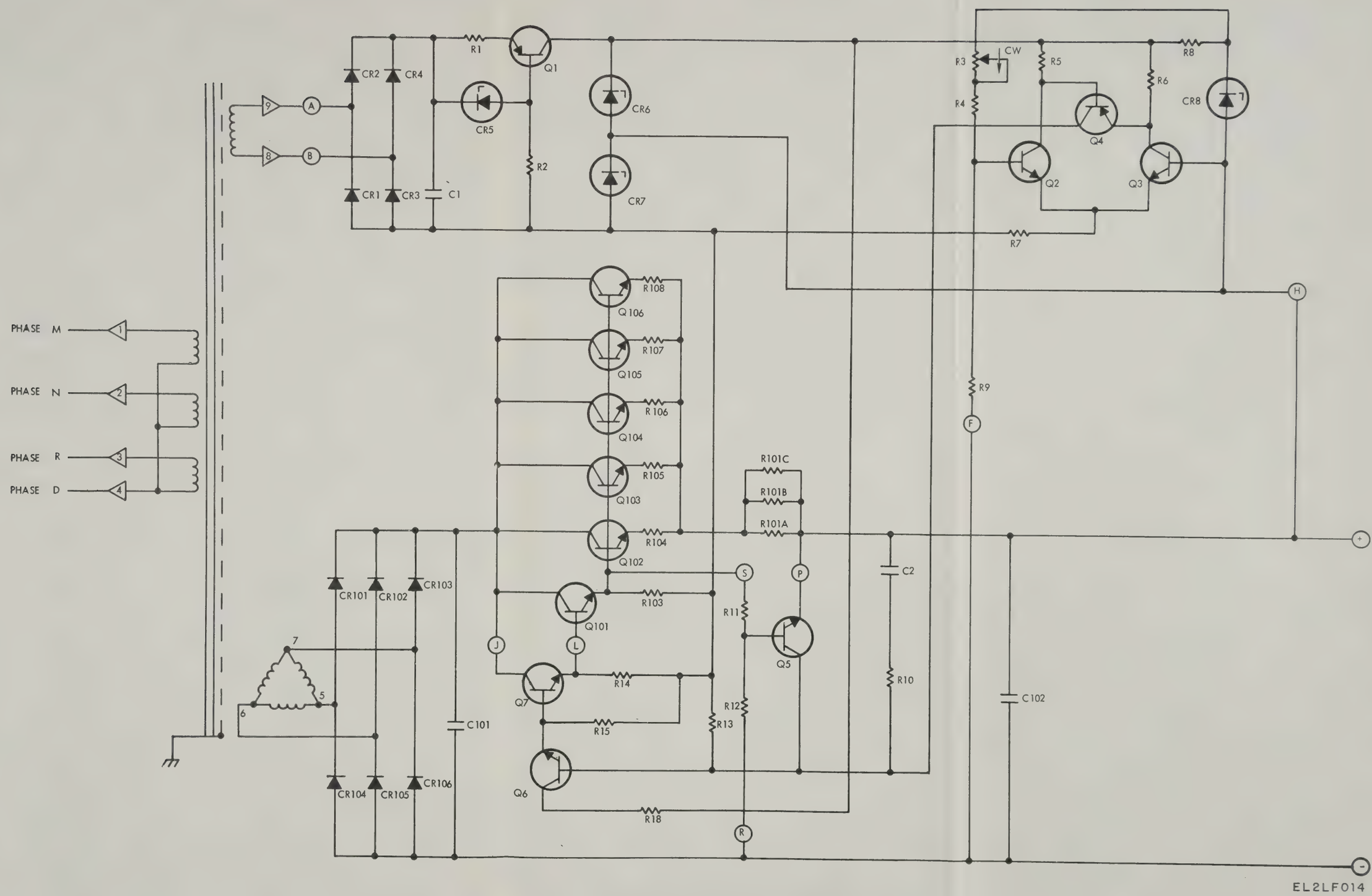
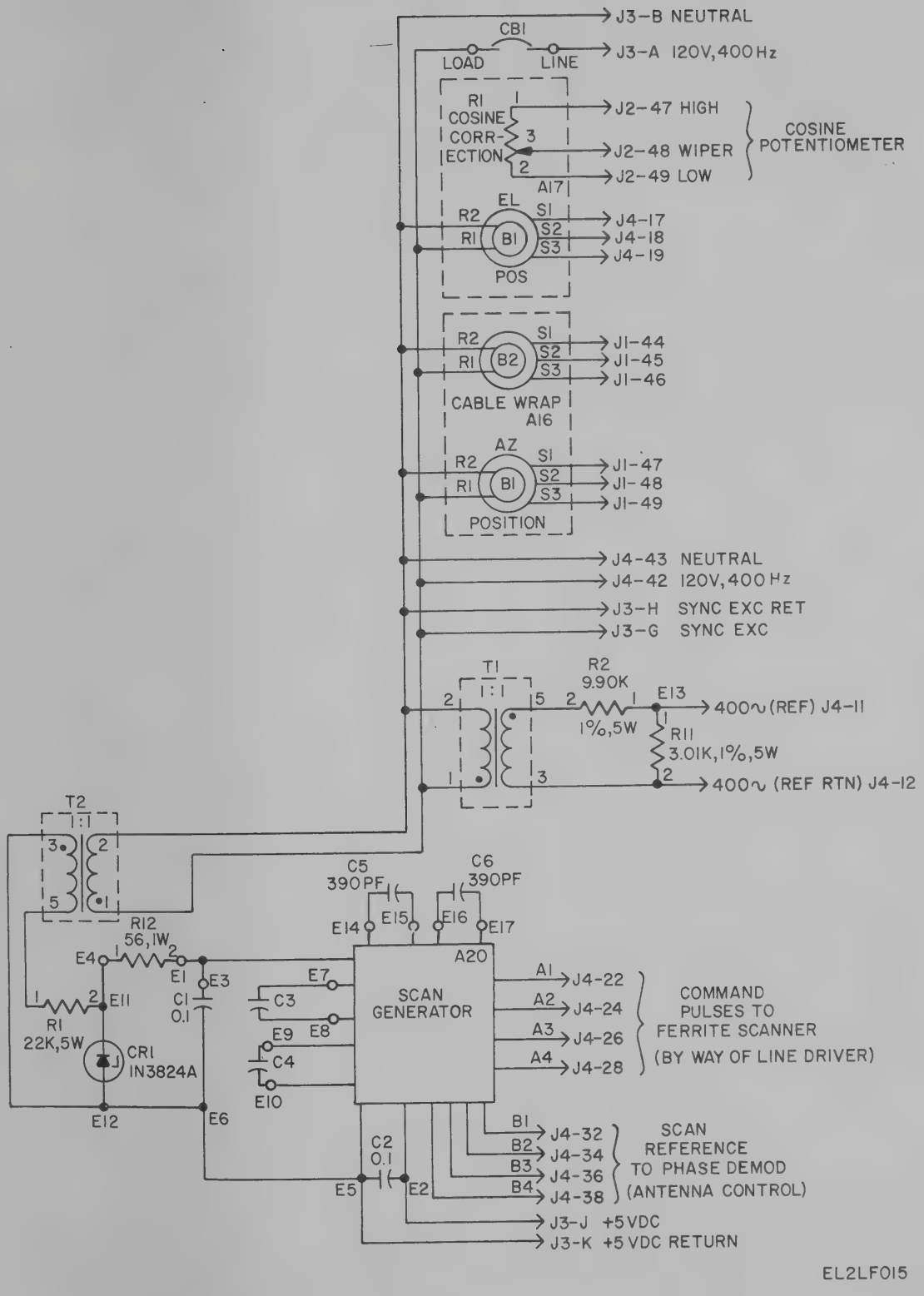


Figure FO 3-3. +28 vdc power supply PS5, schematic diagram.


J3-B NEUTRAL
CB1
LOAD
LINE
J3-A 120V,400Hz
R1
COSINE
CORR-
ECTION
3
2
J2-47 HIGH
J2-48 WIPER
J2-49 LOW
COSINE POTENTIOMETER
A17
EL
R2
R1
B1
POS
S1
S2
S3
J4-17
J4-18
J4-19
B2
CABLE WRAP
A16
J1-44
J1-45
J1-46
AZ
POSITION
J1-47
J1-48
J1-49
J4-43 NEUTRAL
J4-42 120V,400Hz
J3-H SYNC EXC RET
J3-G SYNC EXC
T1
1:1
R2
9.90K
1%,5W
E13
400∿ (REF) J4-11
R11
3.01K,1%,5W
400∿ (REF RTN) J4-12
T2
C5
390PF
C6
390PF
E14
E15
E16
E17
R12
56,1W
E4
E1
E3
E7
C1
0.1
C3
E9
E8
C4
E10
E11
R1
22K,5W
CR1
IN3824A
E12
E6
A20
SCAN
GENERATOR
A1
A2
A3
A4
J4-22
J4-24
J4-26
J4-28
COMMAND
PULSES TO
FERRITE SCANNER
(BY WAY OF LINE DRIVER)
B1
B2
B3
B4
J4-32
J4-34
J4-36
J4-38
SCAN
REFERENCE
TO PHASE DEMOD
(ANTENNA CONTROL)
C2
0.1
E5
E2
J3-J +5VDC
J3-K +5 VDC RETURN
EL2LF015

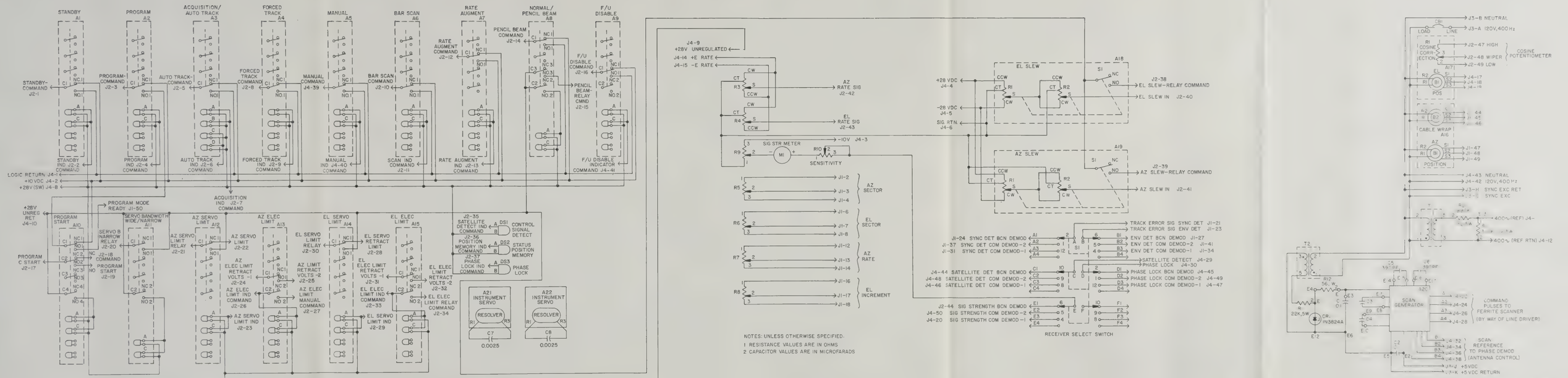
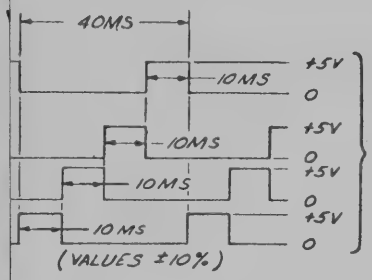
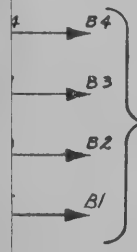


Figure FO 3-4. Antenna control panel, schematic diagram.

FROM A
PANEL,



PULSE GROUP TO LINE DRIVERS ON ANTENNA CONTROL PANEL



DELAYED PULSE GROUP TO TRACKING DEMODULATOR ON ANTENNA CONTROL PANEL

EL2LF016

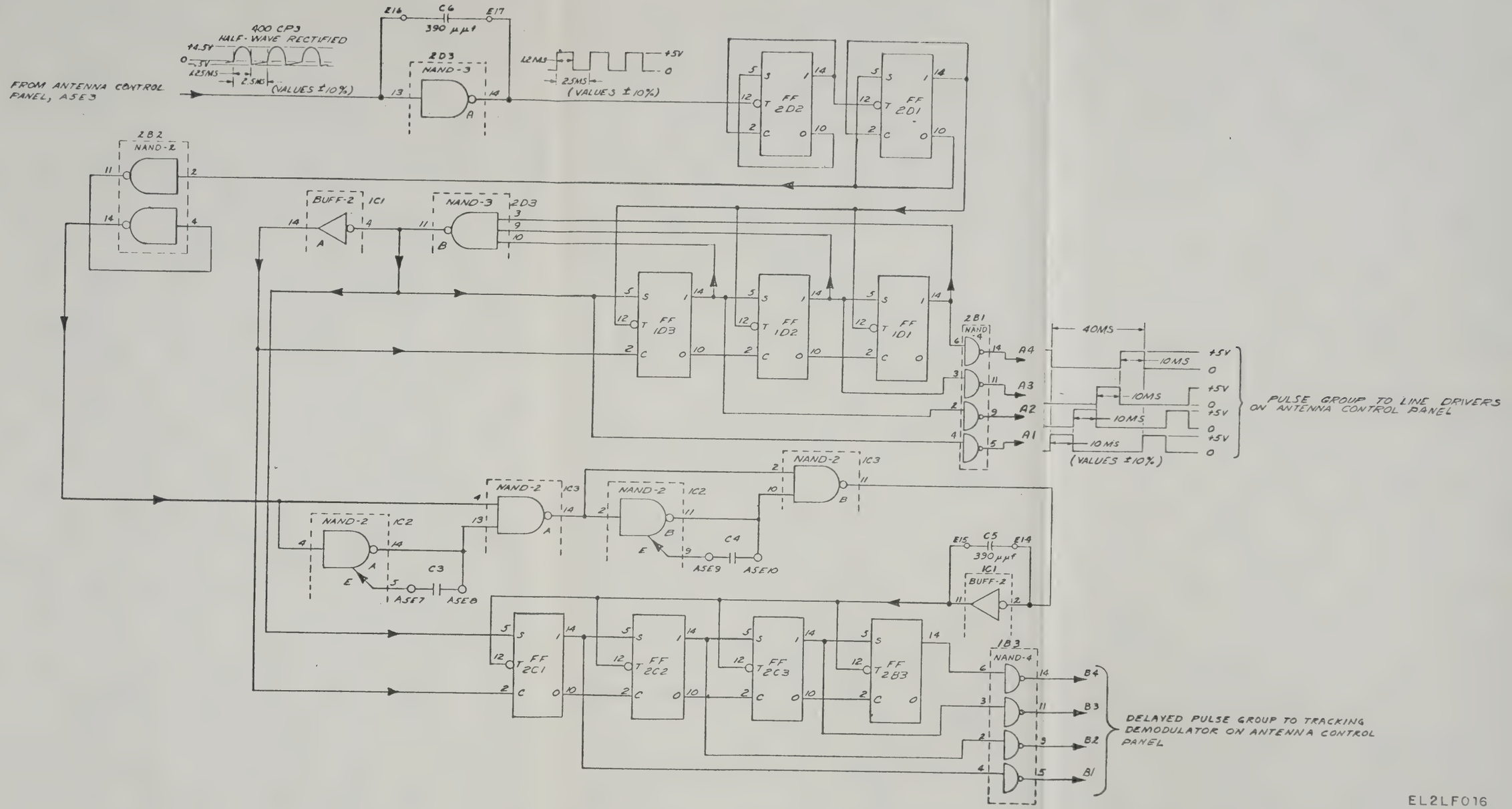
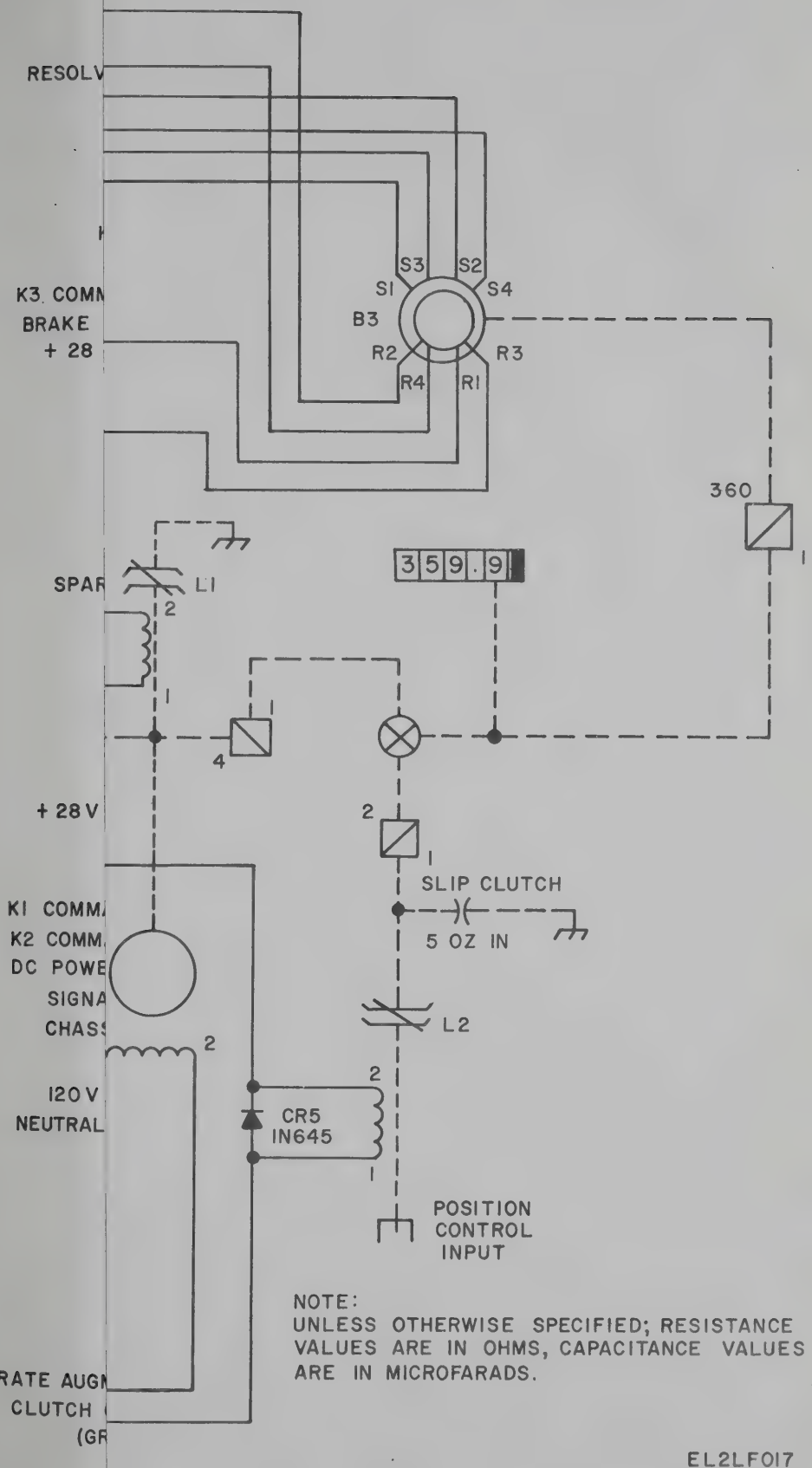


Figure FO 3-5. Scan generator A20, logic diagram.



NOTE:
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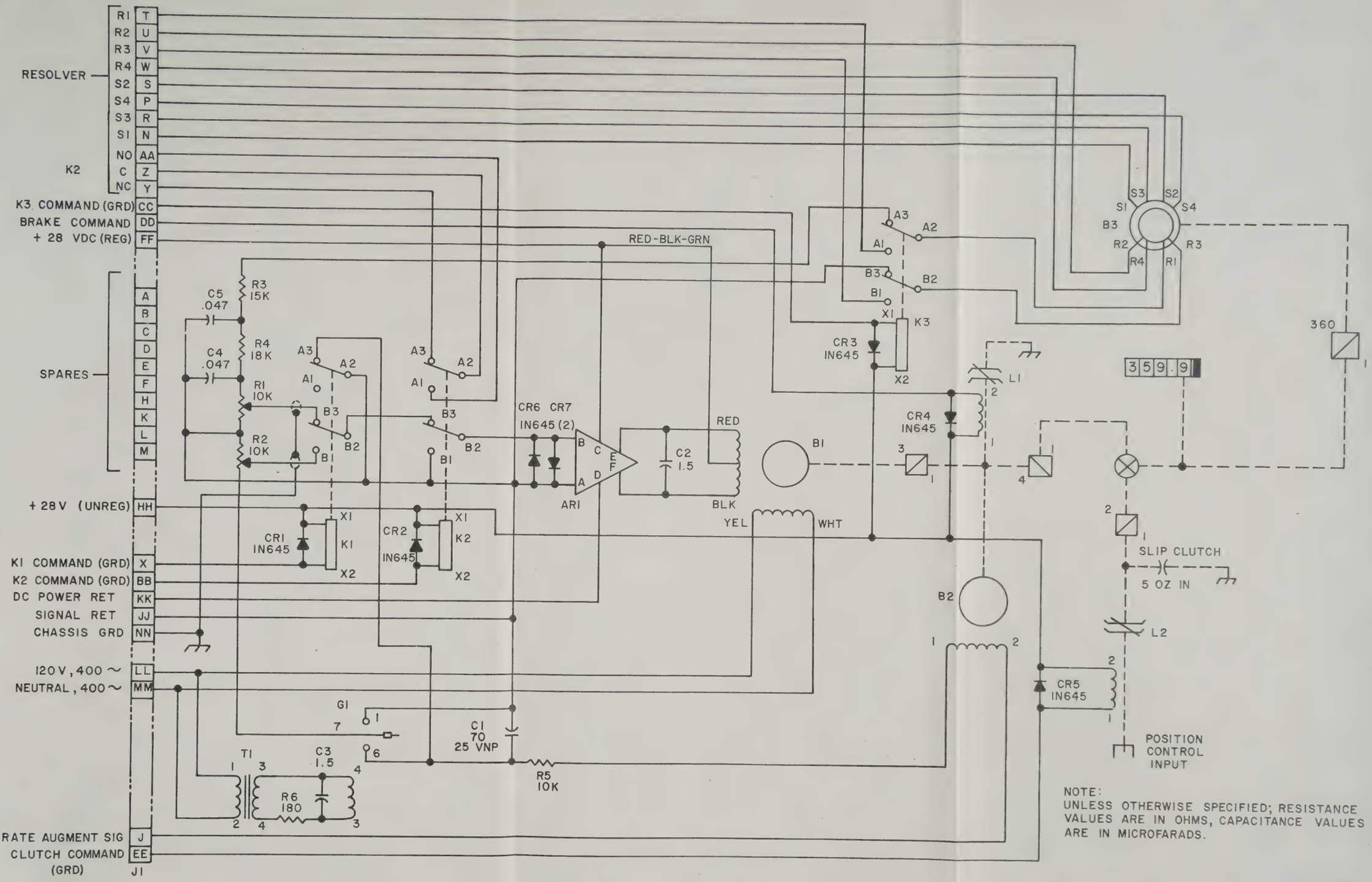
EL2LF017



NOTE:
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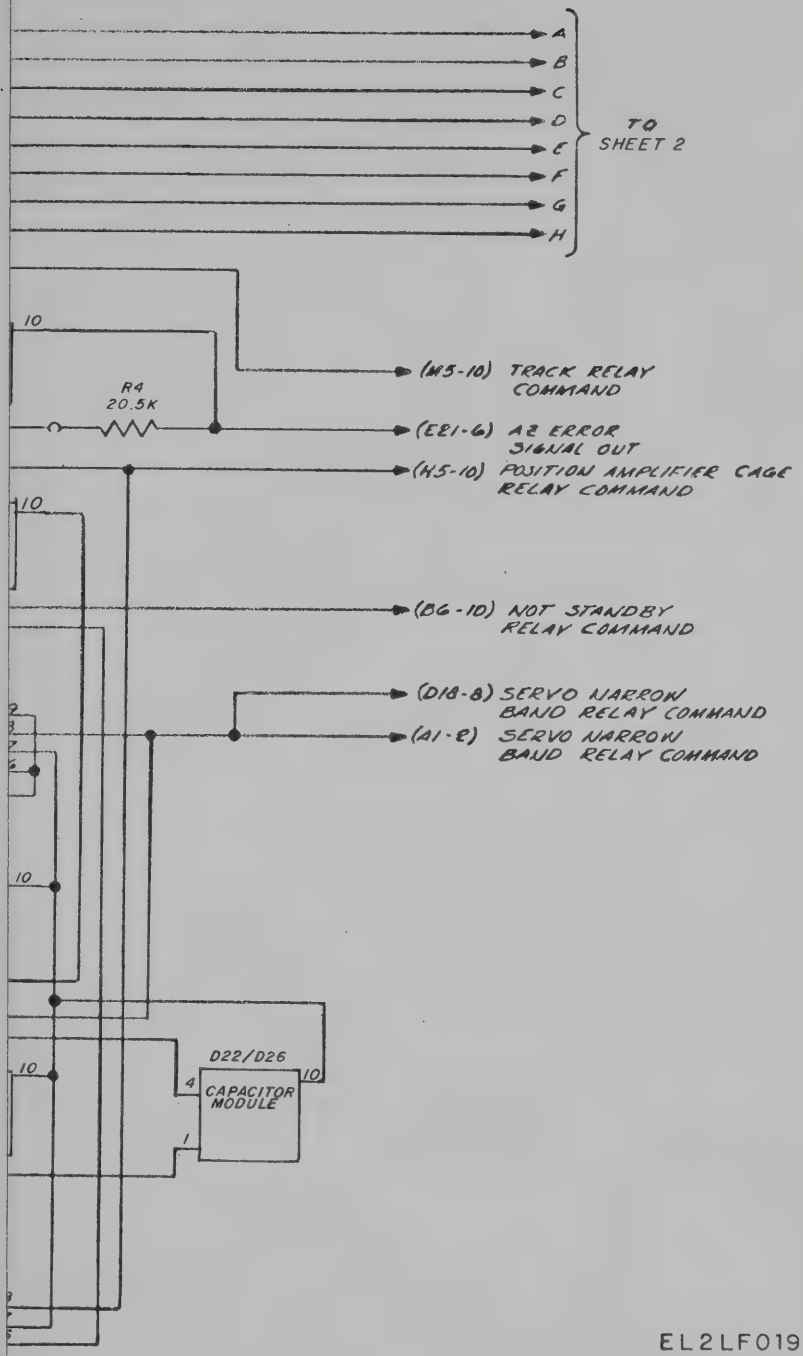
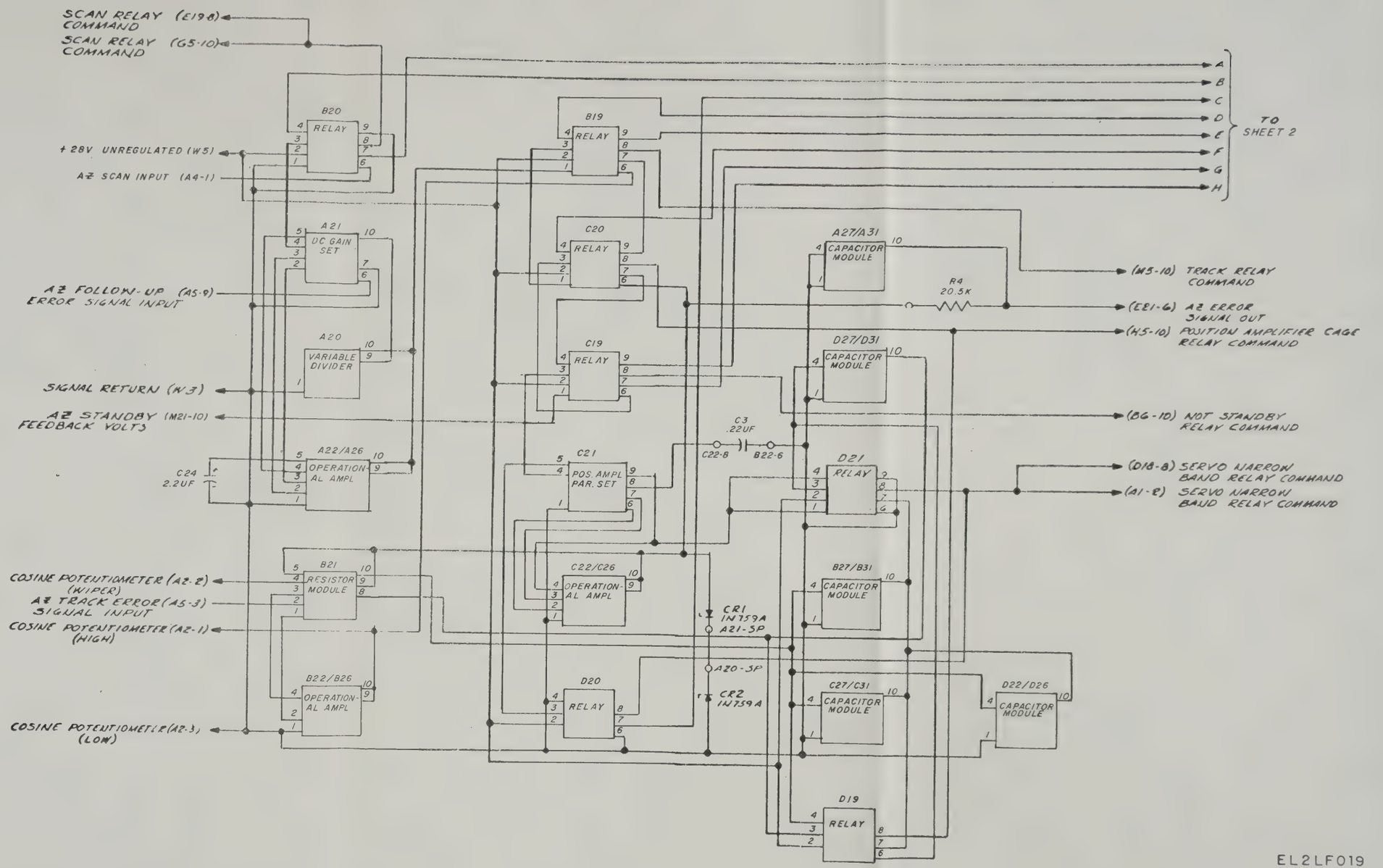
EL2LF017

Figure FO 3-6. Azimuth and elevation servo mechanism, schematic diagram.

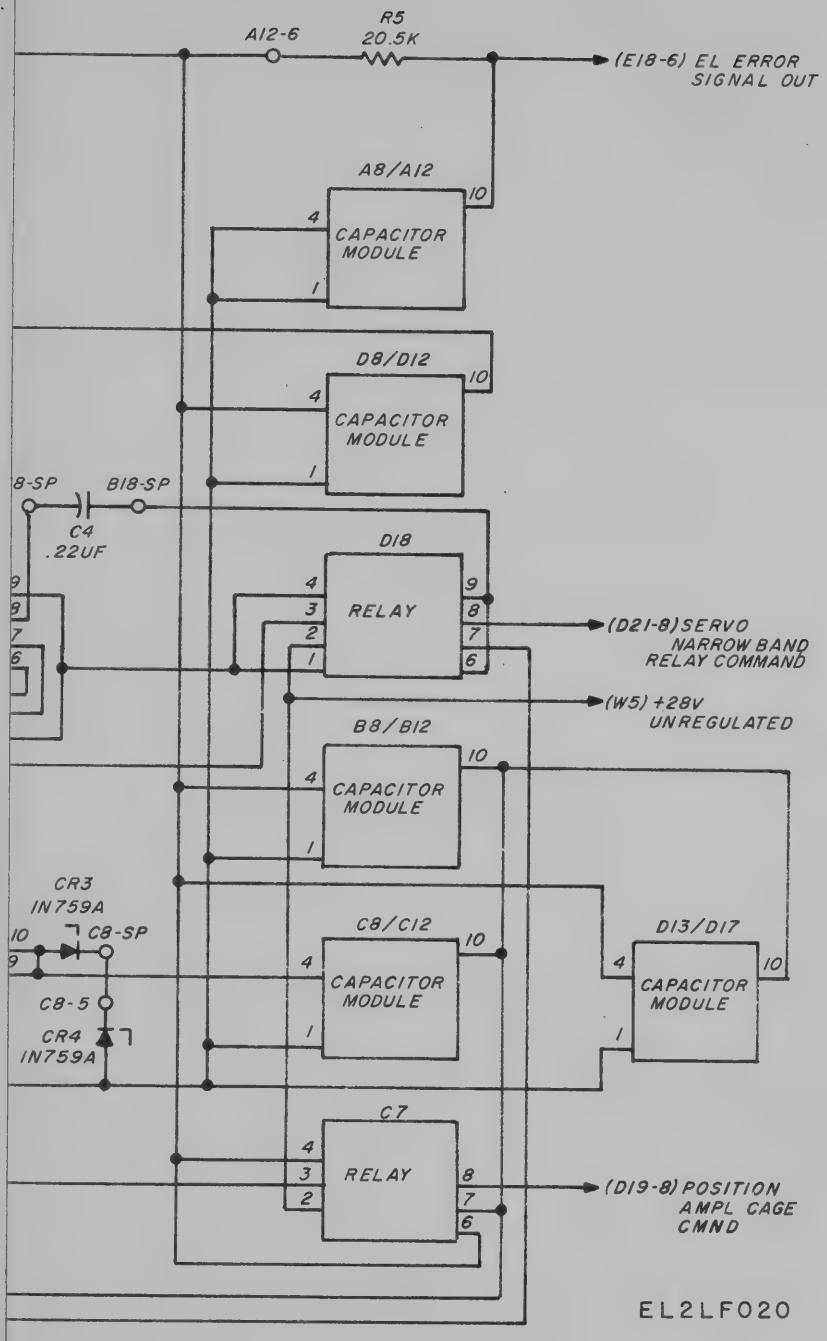

A
B
C
D
E
F
G
H
TO SHEET 2
10
R4
20.5K
(H3-10) TRACK RELAY COMMAND
(E21-6) AZ ERROR SIGNAL OUT
(H5-10) POSITION AMPLIFIER CAGE RELAY COMMAND
10
(B6-10) NOT STANDBY RELAY COMMAND
(D18-8) SERVO NARROW BAND RELAY COMMAND
(A1-8) SERVO NARROW BAND RELAY COMMAND
10
10
D22/D26
CAPACITOR MODULE
4
1
10

EL2LF019



EL2LF019

Figure FO 3-7. ① Upper module board, schematic diagram (sheet 1 of 7).



natic diagram (sheet 2 of 7).

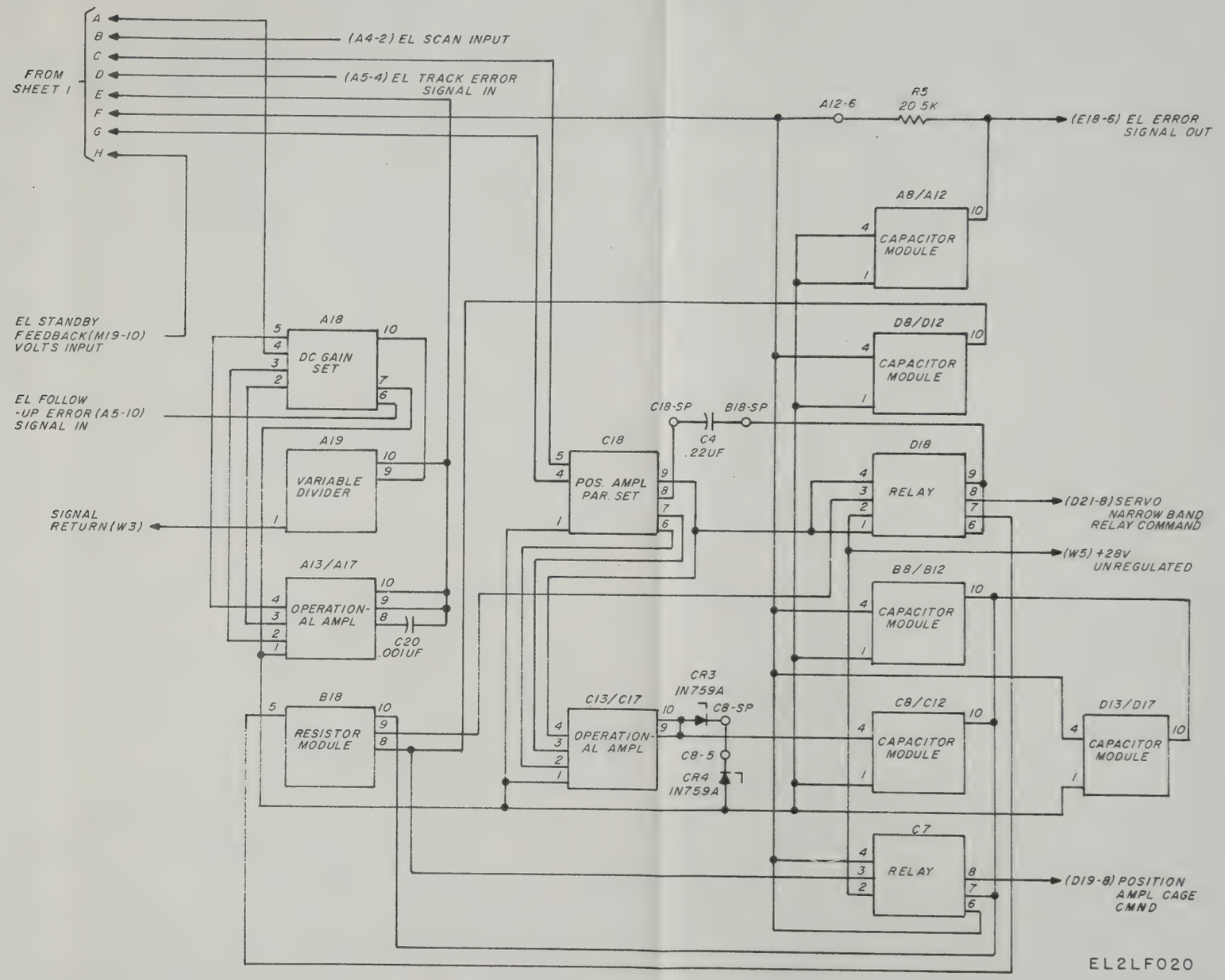
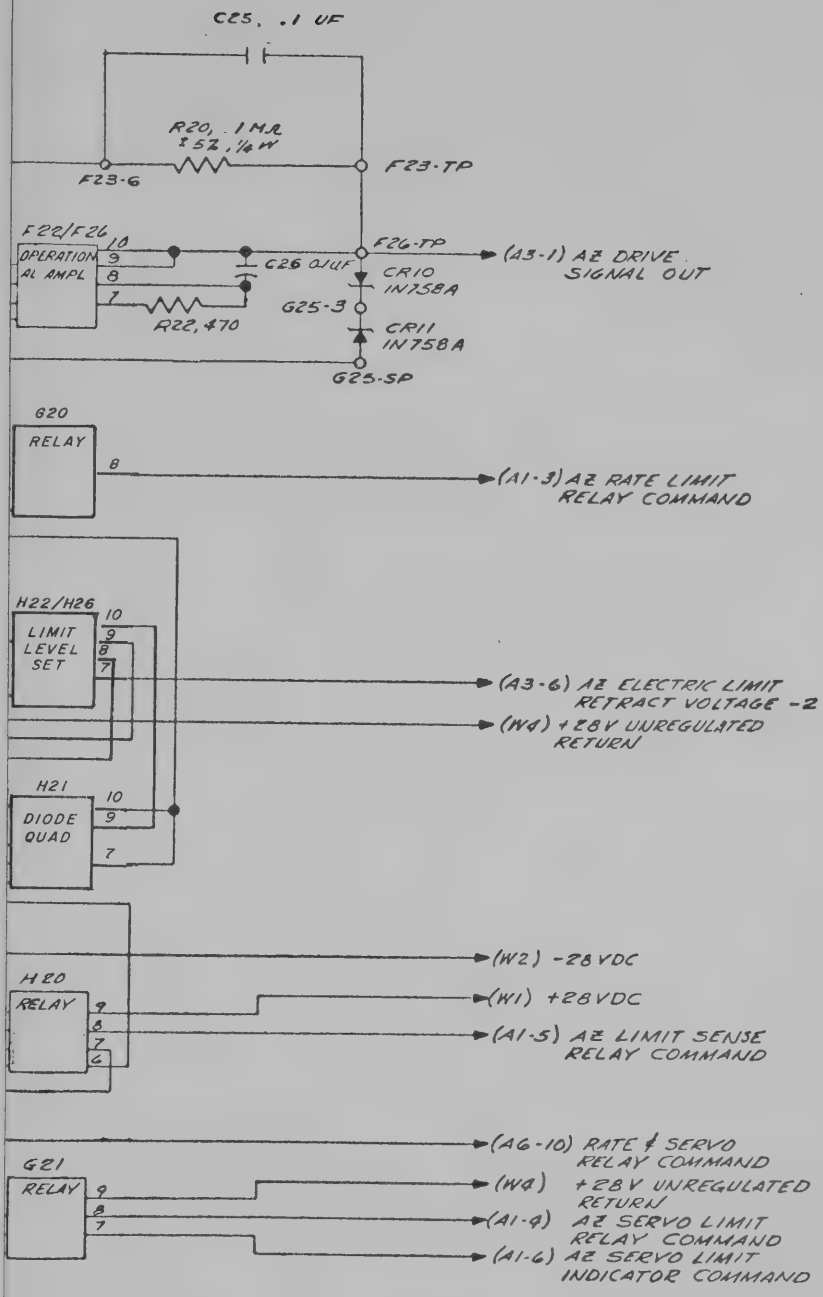


Figure FO 3-7. ③Upper module board, schematic diagram (sheet 2 of 7).



EL2LF021

eet 3 of 7).

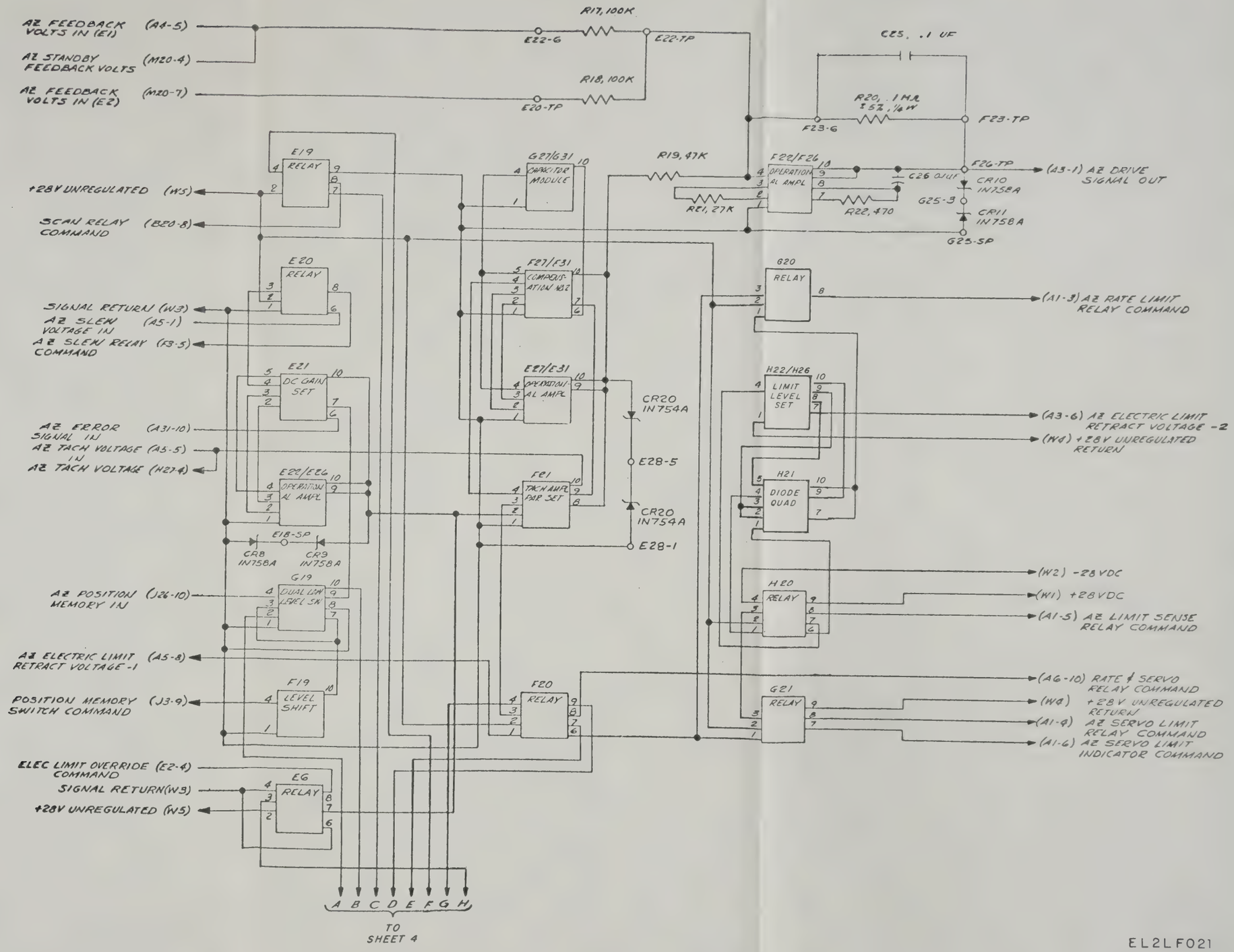
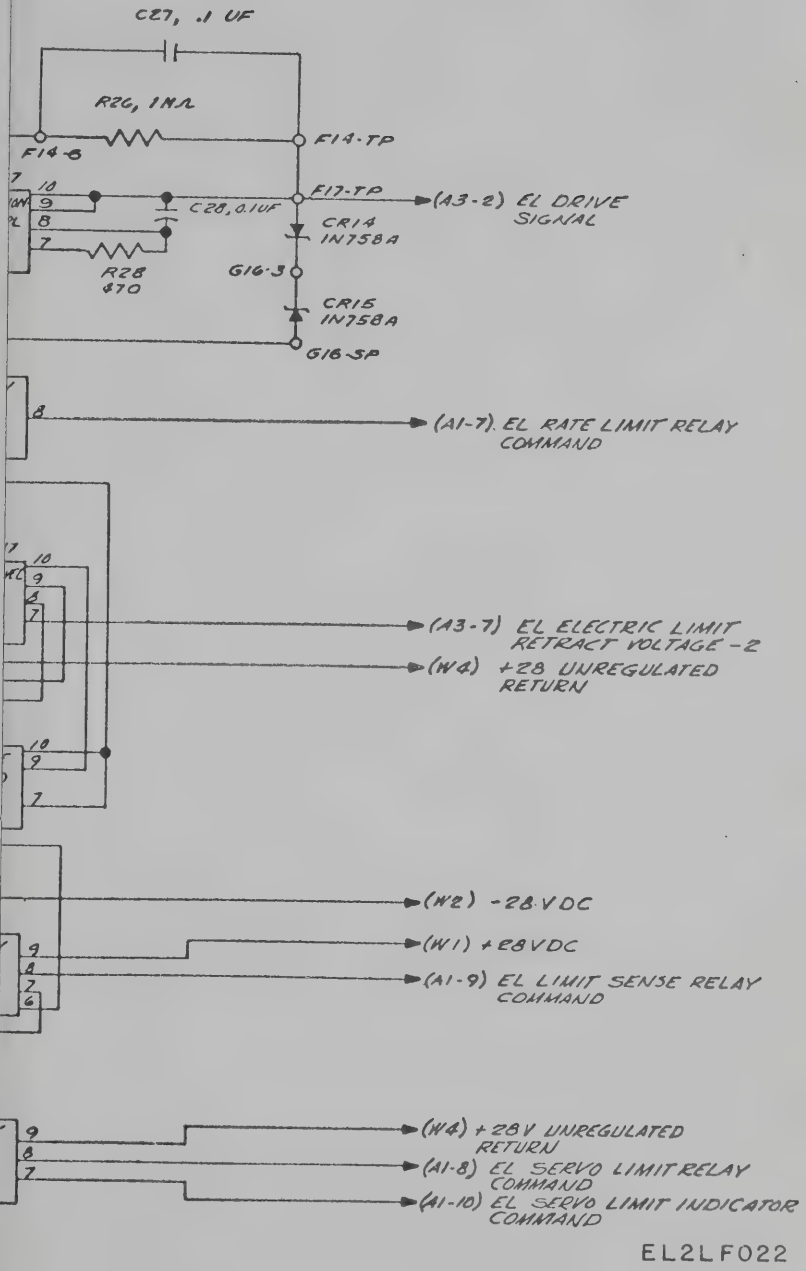


Figure FO 3-7.③Upper module board, schematic diagram (sheet 3 of 7).


C27, .1 UF
R26, 1 MΩ
F14-6
F14-TP
F17-TP
(A3-2) EL DRIVE SIGNAL
C28, 0.1UF
CR14 IN758A
R28 470
G16-3
CR15 IN758A
G16-SP
(A1-7) EL RATE LIMIT RELAY COMMAND
(A3-7) EL ELECTRIC LIMIT RETRACT VOLTAGE -2
(W4) +28 UNREGULATED RETURN
(W2) -28 VDC
(W1) +28 VDC
(A1-9) EL LIMIT SENSE RELAY COMMAND
(W4) +28 V UNREGULATED RETURN
(A1-8) EL SERVO LIMIT RELAY COMMAND
(A1-10) EL SERVO LIMIT INDICATOR COMMAND
EL2LF022

4 of 7).

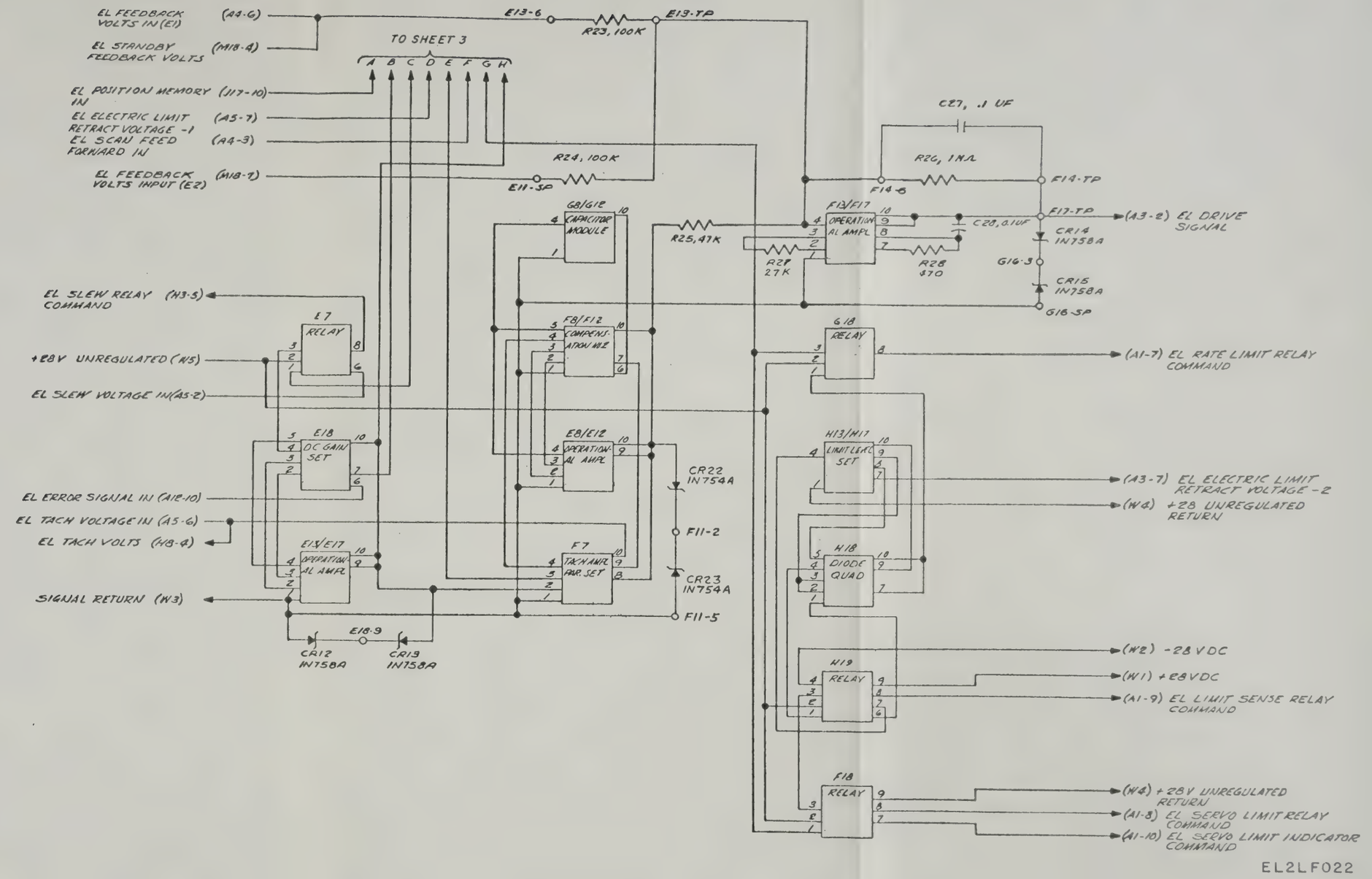
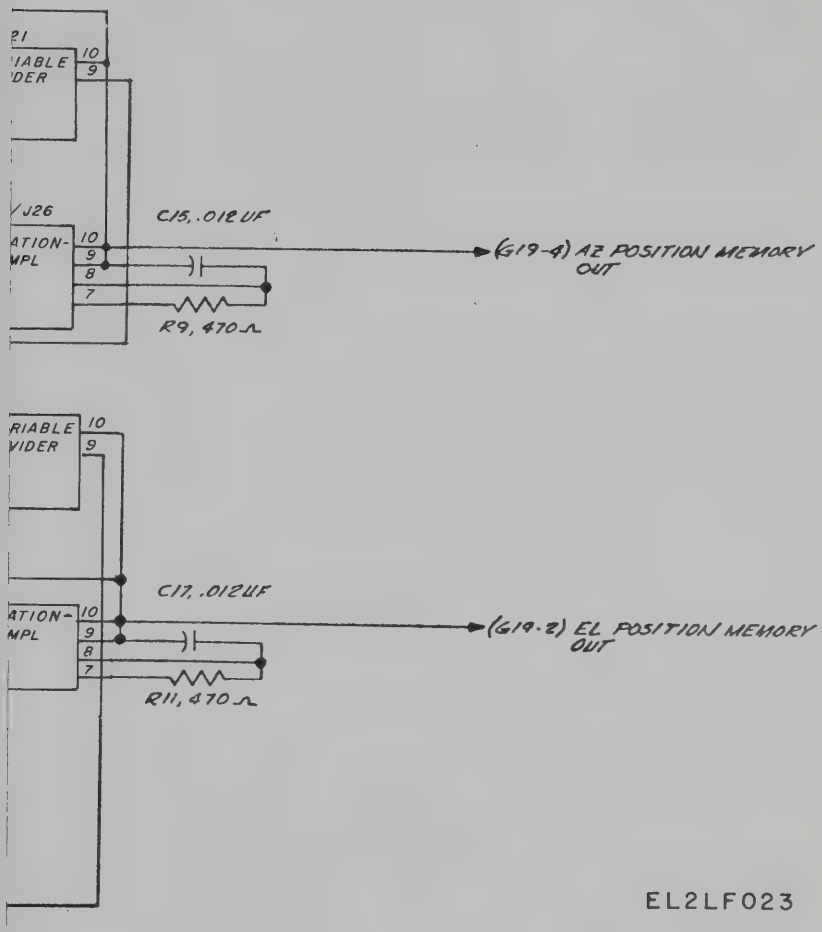


Figure FO 3-7.④ Upper module board, schematic diagram (sheet 4 of 7).


10
9
C15, .012 UF
(G19-4) AZ POSITION MEMORY OUT
8
7
R9, 470Ω
C17, .012 UF
(G19-2) EL POSITION MEMORY OUT
R11, 470Ω
EL2LF023

5 of 7).

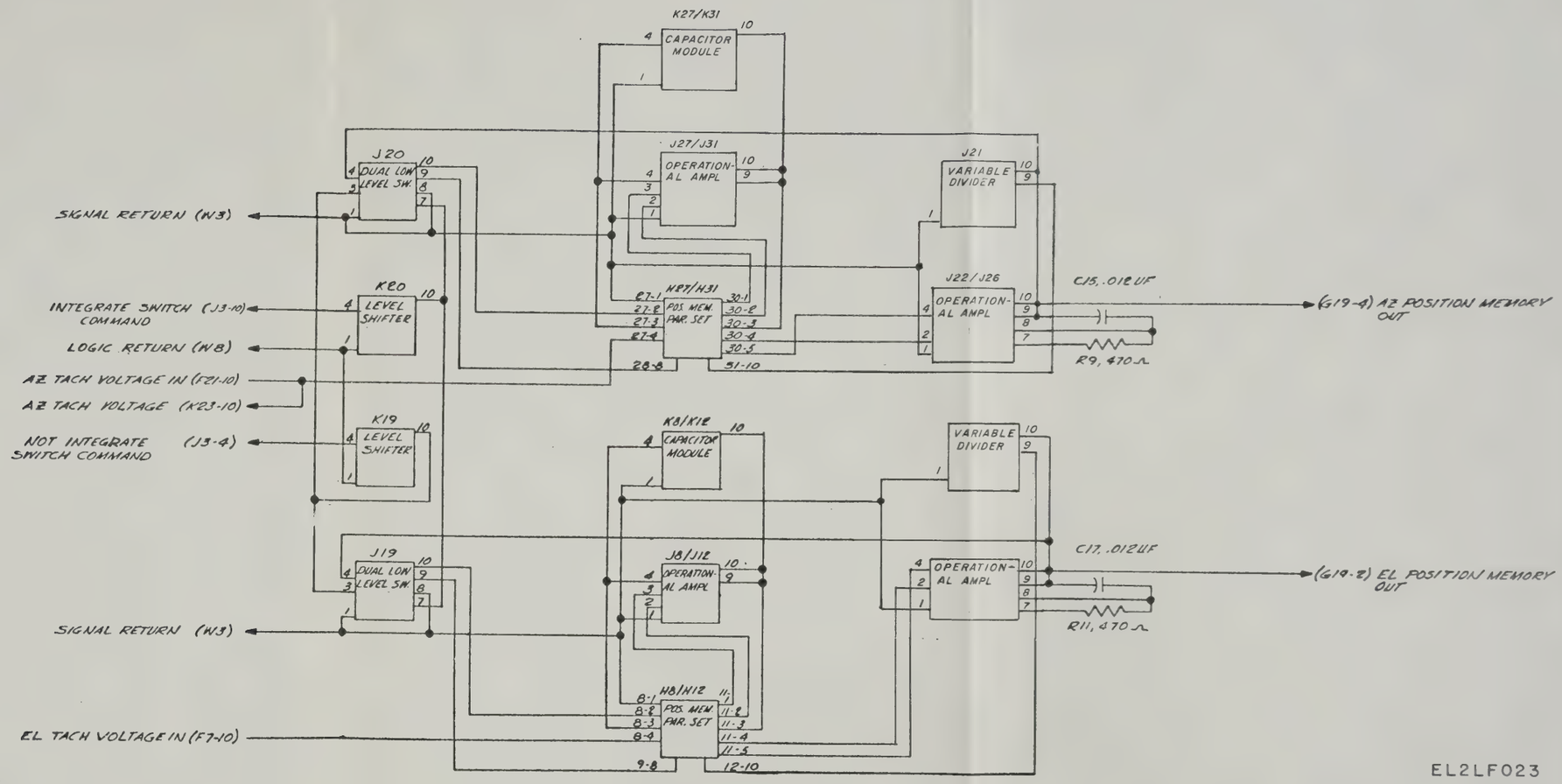
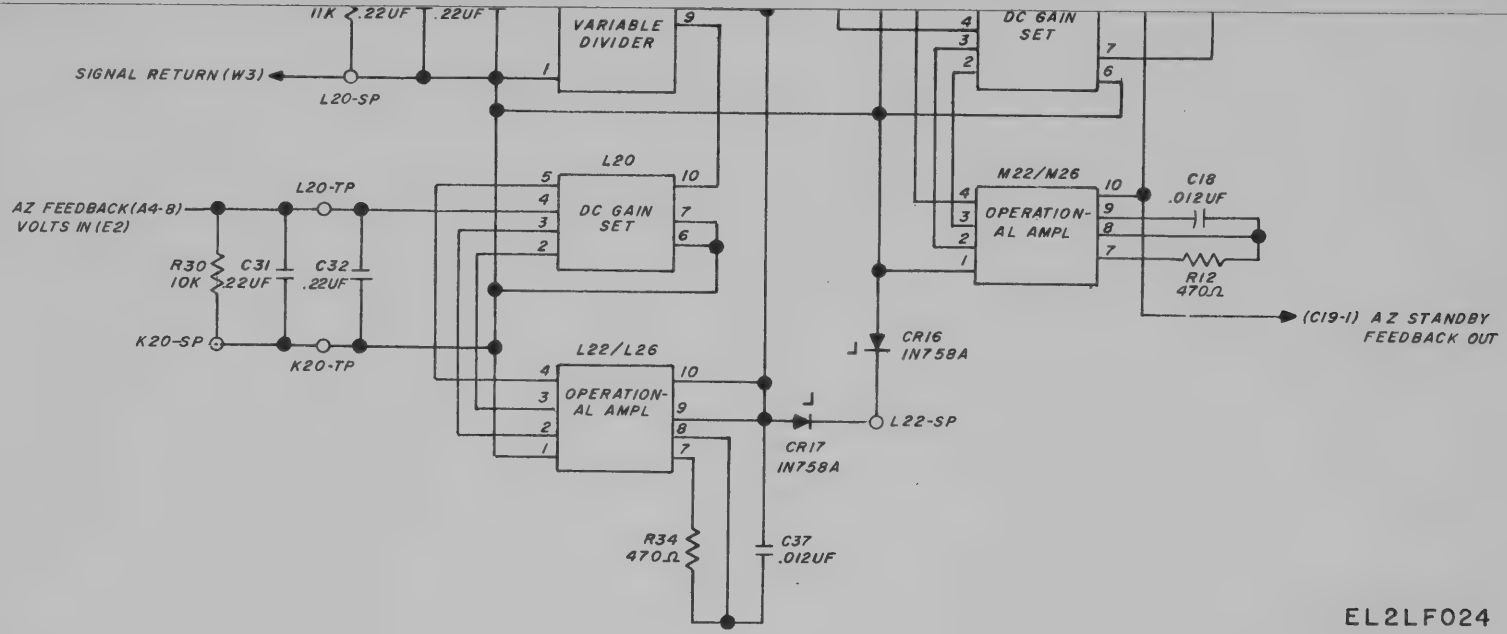
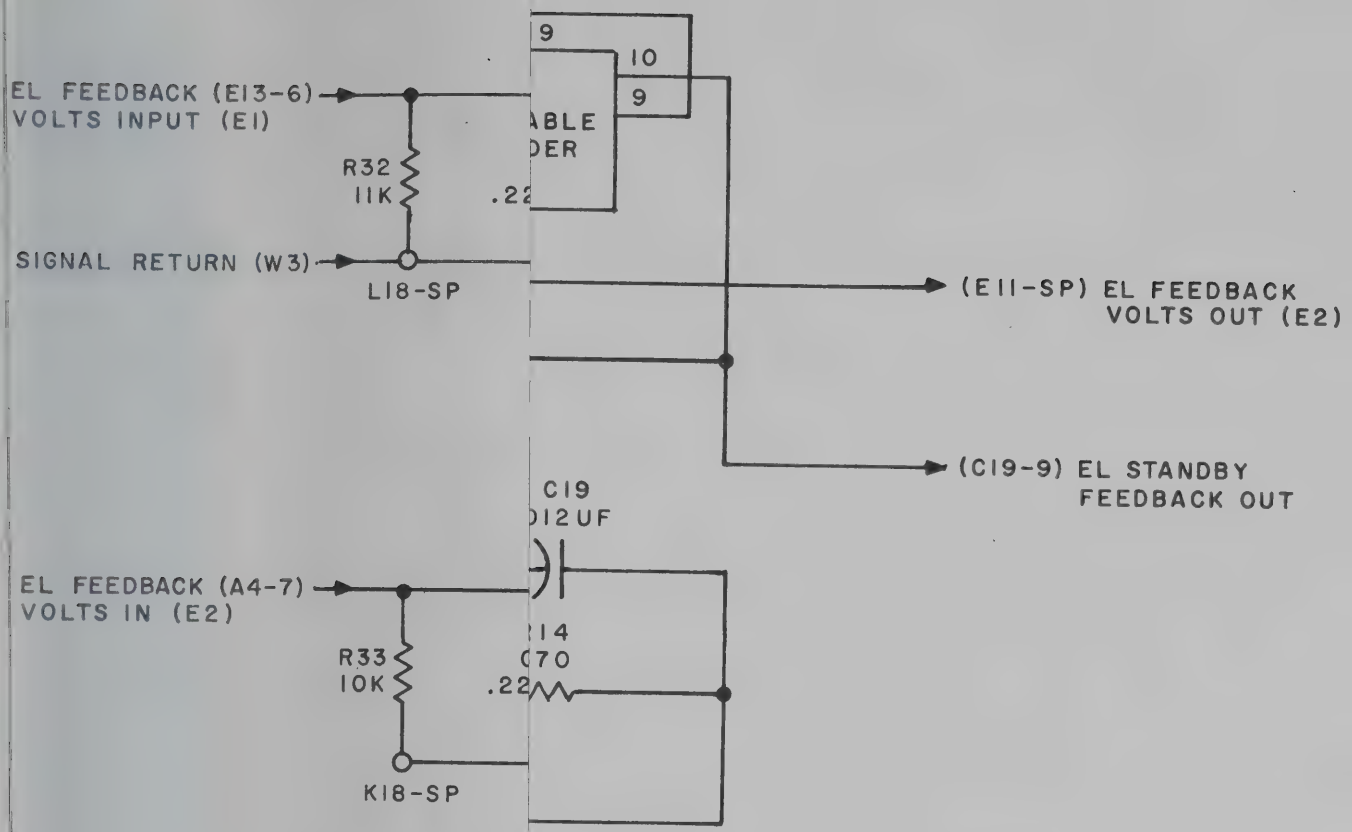


Figure FO 3-7.Ⓢ Upper module board, schematic diagram (sheet 5 of 7).



Upper module board, schematic diagram (sheet 6 of 7).

Figure FO 3-7.ⓔUpper module board, schematic diagram (sheet 6 of 7).


9
10
9
EL FEEDBACK (E13-6)
VOLTS INPUT (E1)
ABLE
DER
R32
11K
.22
SIGNAL RETURN (W3)
L18-SP
(E11-SP) EL FEEDBACK
VOLTS OUT (E2)
(C19-9) EL STANDBY
FEEDBACK OUT
C19
012UF
EL FEEDBACK (A4-7)
VOLTS IN (E2)
214
C70
R33
10K
.22
K18-SP

EL2LF025

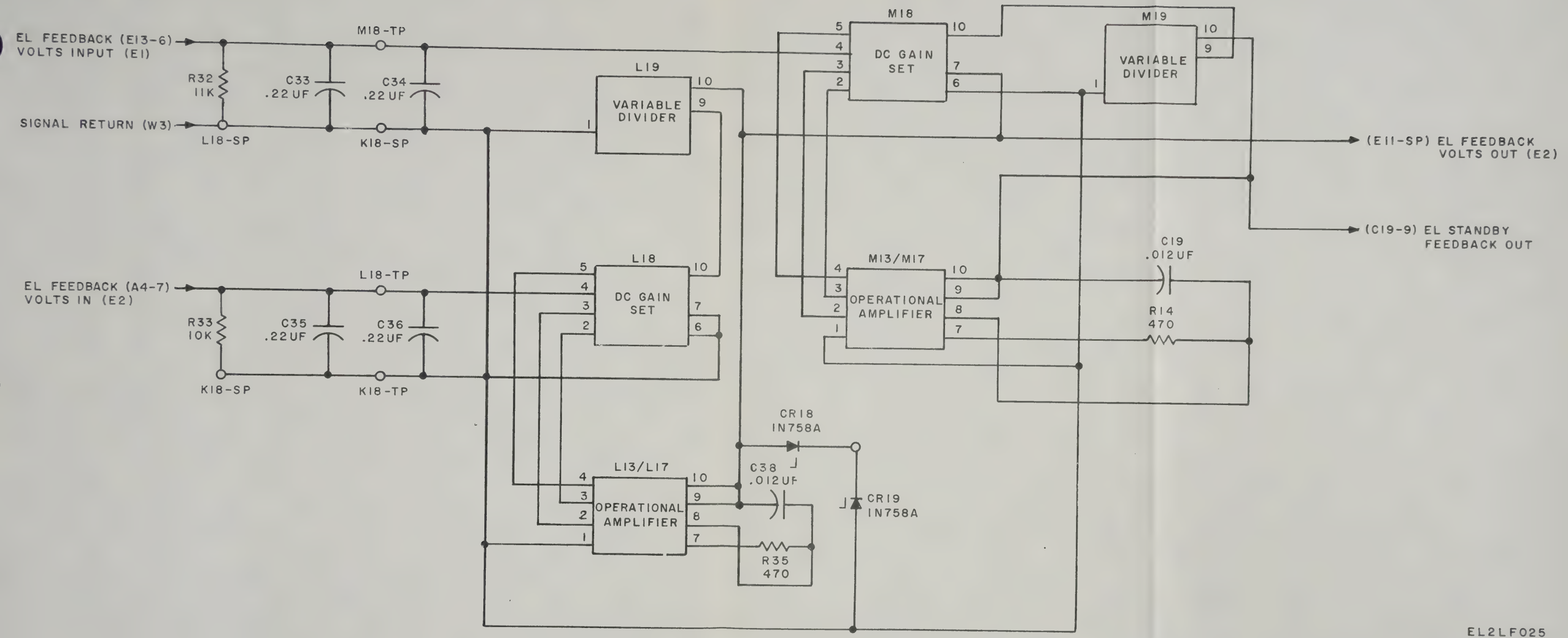
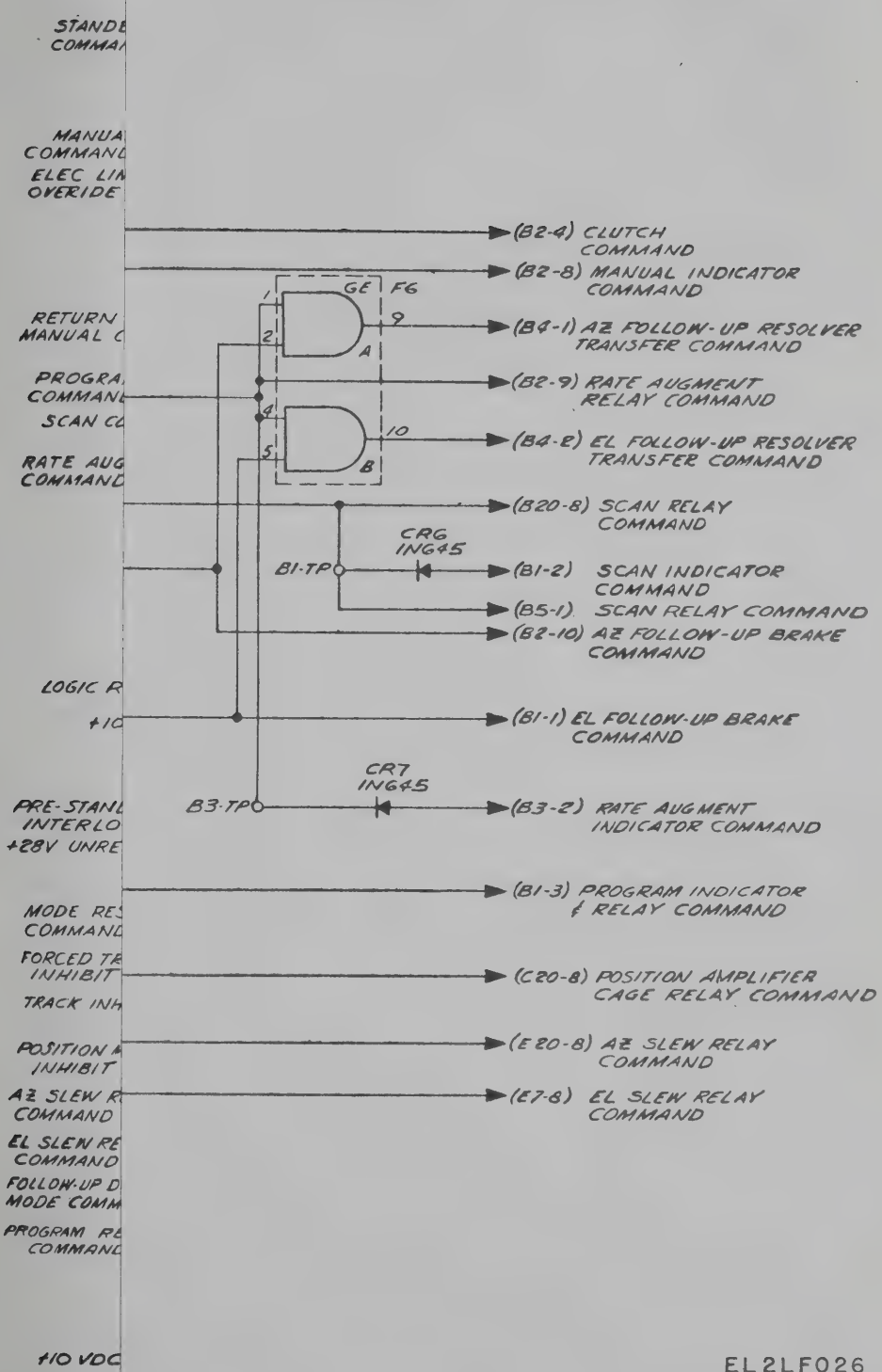


Figure FO 3-7.Ⓣ Upper module board, schematic diagram (sheet 7 of 7).


STANDE
COMMA
MANUA
COMMAND
ELEC LIN
OVERIDE
RETURN
MANUAL C
PROGRA
COMMAN
SCAN CO
RATE AUG
COMMAND
LOGIC R
+10
PRE-STAN
INTERLO
+28V UNRE
MODE RES
COMMAND
FORCED TR
INHIBIT
TRACK INH
POSITION A
INHIBIT
AZ SLEW R
COMMAND
EL SLEW RE
COMMAND
FOLLOW-UP D
MODE COMM
PROGRAM RE
COMMAND
+10 VDC
GE F6
1
2
9
A
4
5
10
B
B1-TP
B3-TP
CRG
ING45
CR7
ING45
(B2-4) CLUTCH COMMAND
(B2-8) MANUAL INDICATOR COMMAND
(B4-1) AZ FOLLOW-UP RESOLVER TRANSFER COMMAND
(B2-9) RATE AUGMENT RELAY COMMAND
(B4-2) EL FOLLOW-UP RESOLVER TRANSFER COMMAND
(B20-8) SCAN RELAY COMMAND
(B1-2) SCAN INDICATOR COMMAND
(B5-1) SCAN RELAY COMMAND
(B2-10) AZ FOLLOW-UP BRAKE COMMAND
(B1-1) EL FOLLOW-UP BRAKE COMMAND
(B3-2) RATE AUGMENT INDICATOR COMMAND
(B1-3) PROGRAM INDICATOR & RELAY COMMAND
(C20-8) POSITION AMPLIFIER CAGE RELAY COMMAND
(E20-8) AZ SLEW RELAY COMMAND
(E7-8) EL SLEW RELAY COMMAND

EL2LF026

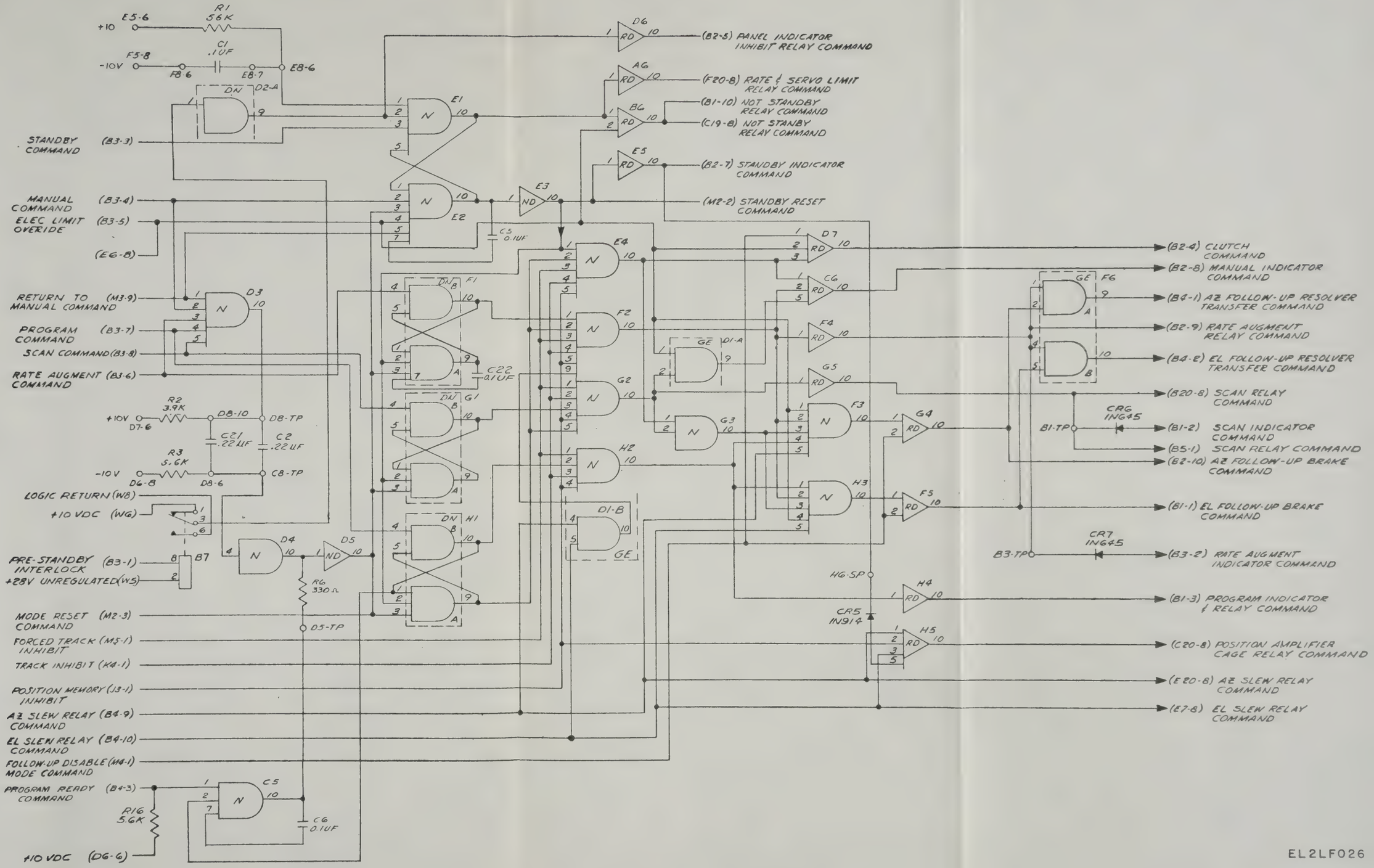


Figure FO 3-8. ① Upper module board, logic diagram (sheet 1 of 2).

SATELLITE DETECTION
DICATOR COMMAND

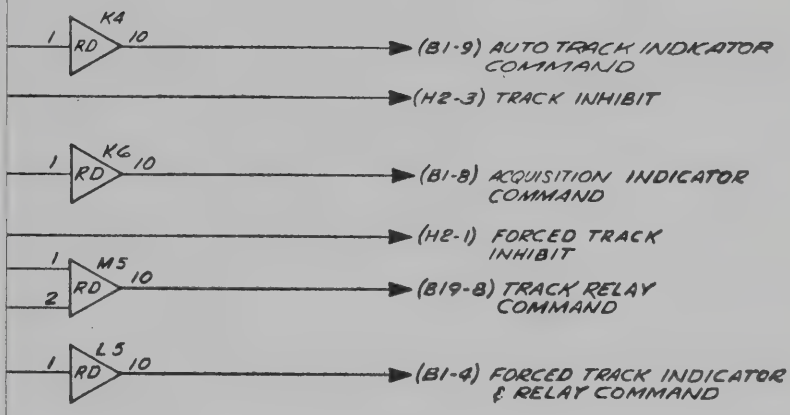
POSITION MEMORY
OR & RELAY COMMAND

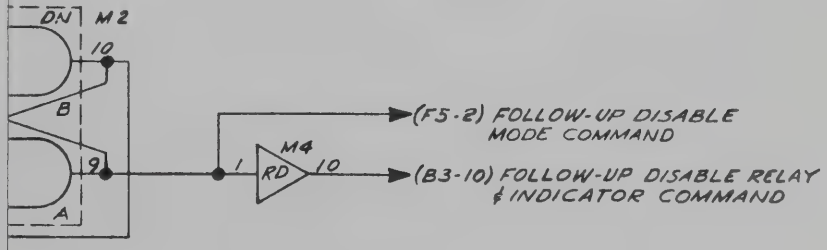
POSITION MEMORY
NHIBIT

POSITION MEMORY
SWITCH COMMAND

) INTEGRATE SWITCH
COMMAND

) NOT INTEGRATE
COMMAND





RETURN TO
L COMMAND

EL2LF027

eet 2 of 2).

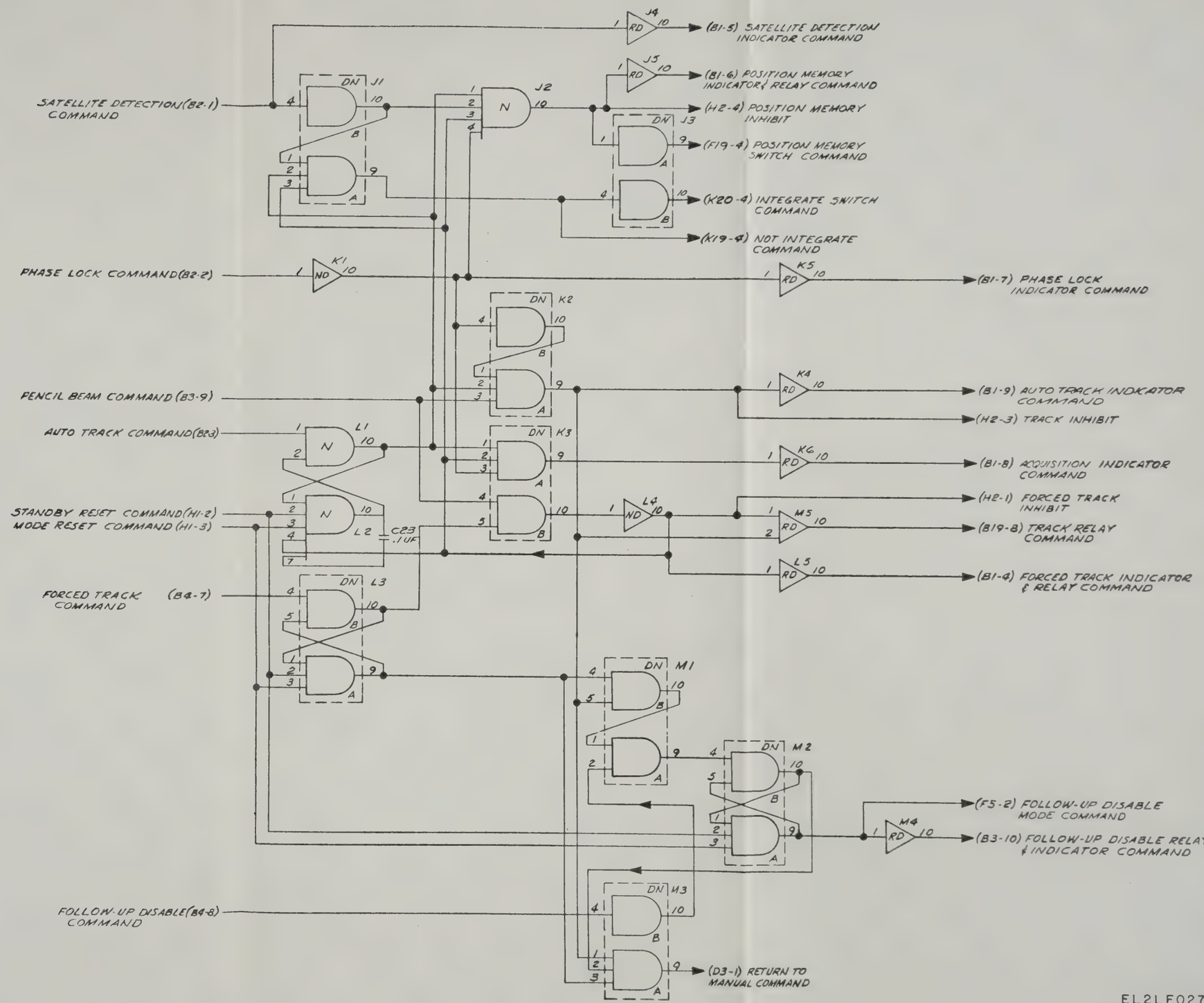


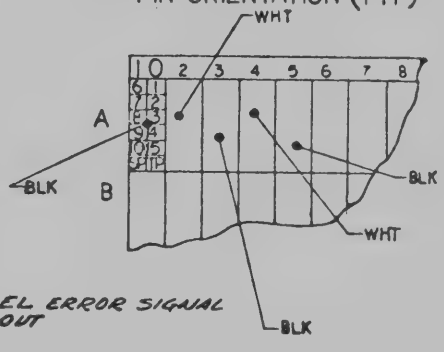
Figure FO 3-8. ②Upper module board, logic diagram (sheet 2 of 2).

→(A31-9) AZ ERROR SIGNAL OUT

59A

D

PIN ORIENTATION (TYP)



→(A31-10) EL ERROR SIGNAL OUT

SP

59A

B

EL2LF038

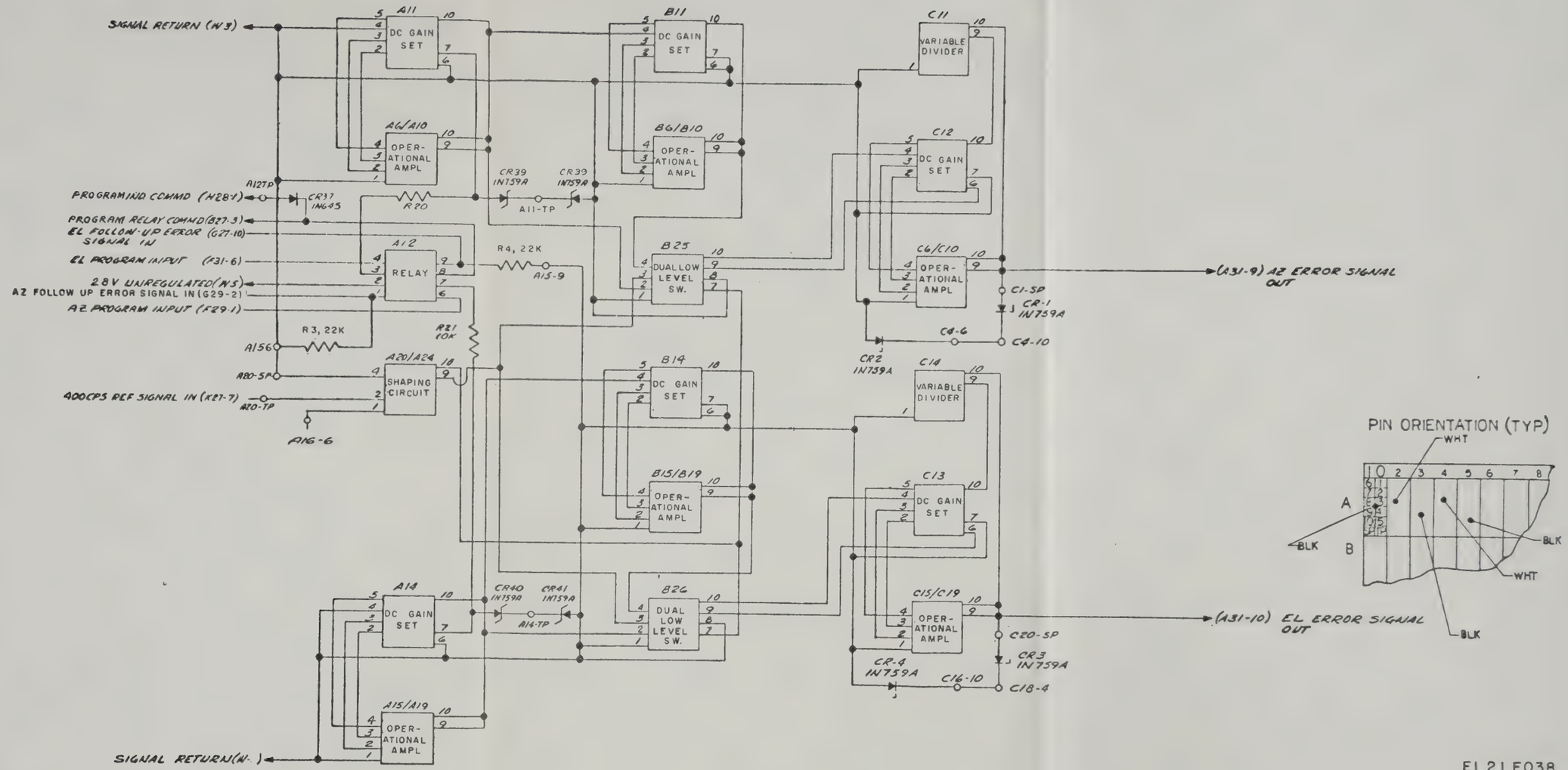
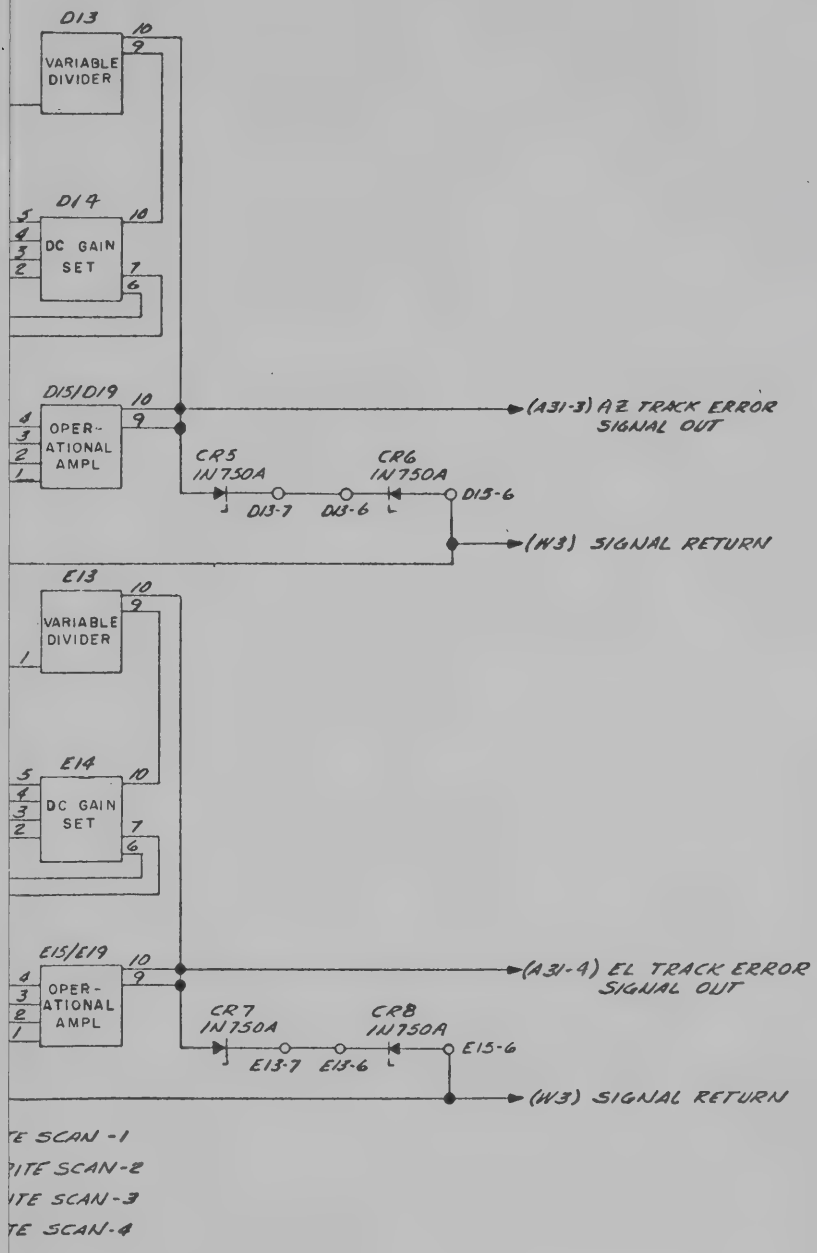


Figure FO 3-9.① Lower module board, schematic diagram (sheet 1 of 4).



EL2LF039

eet 2 of 4).

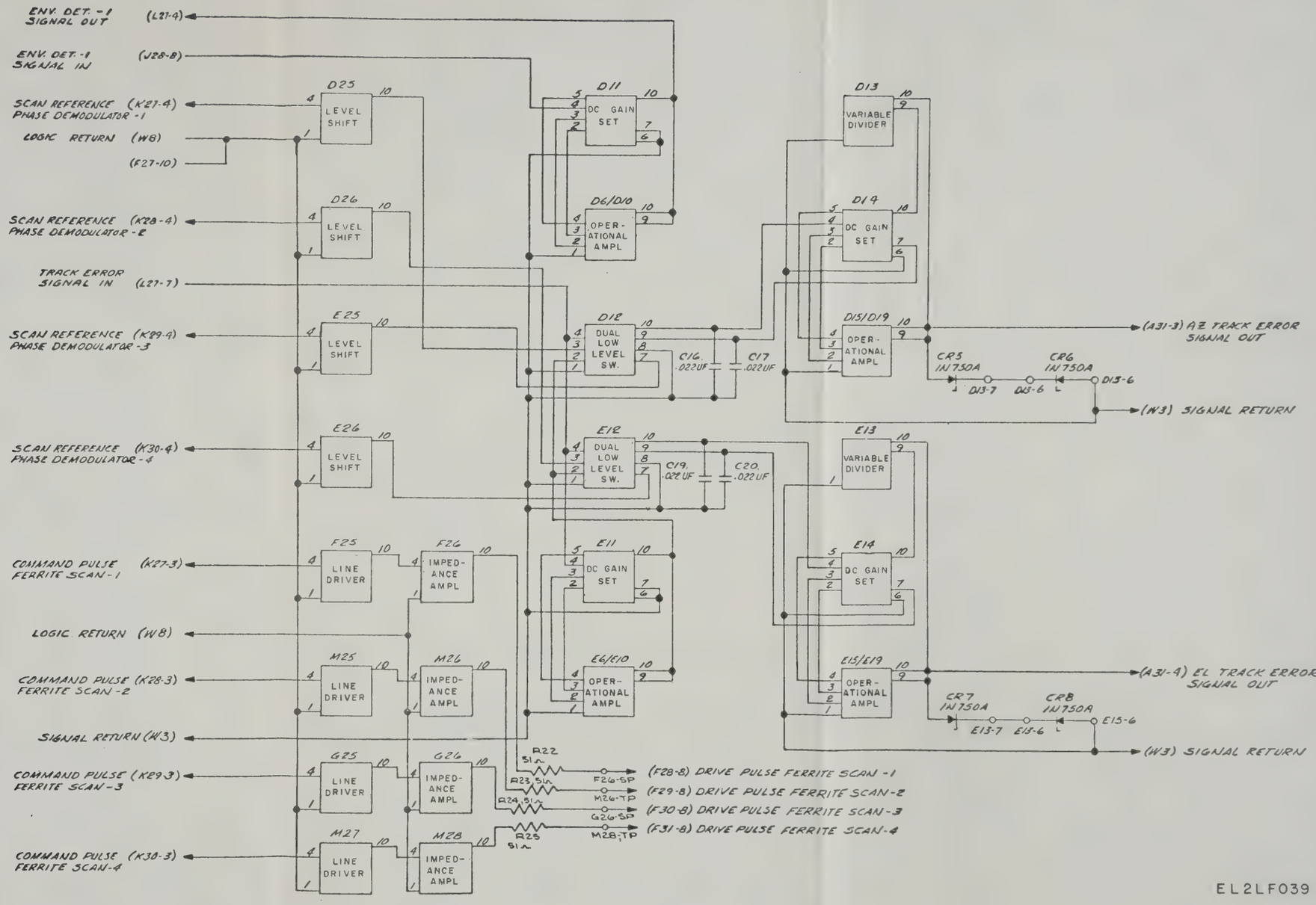
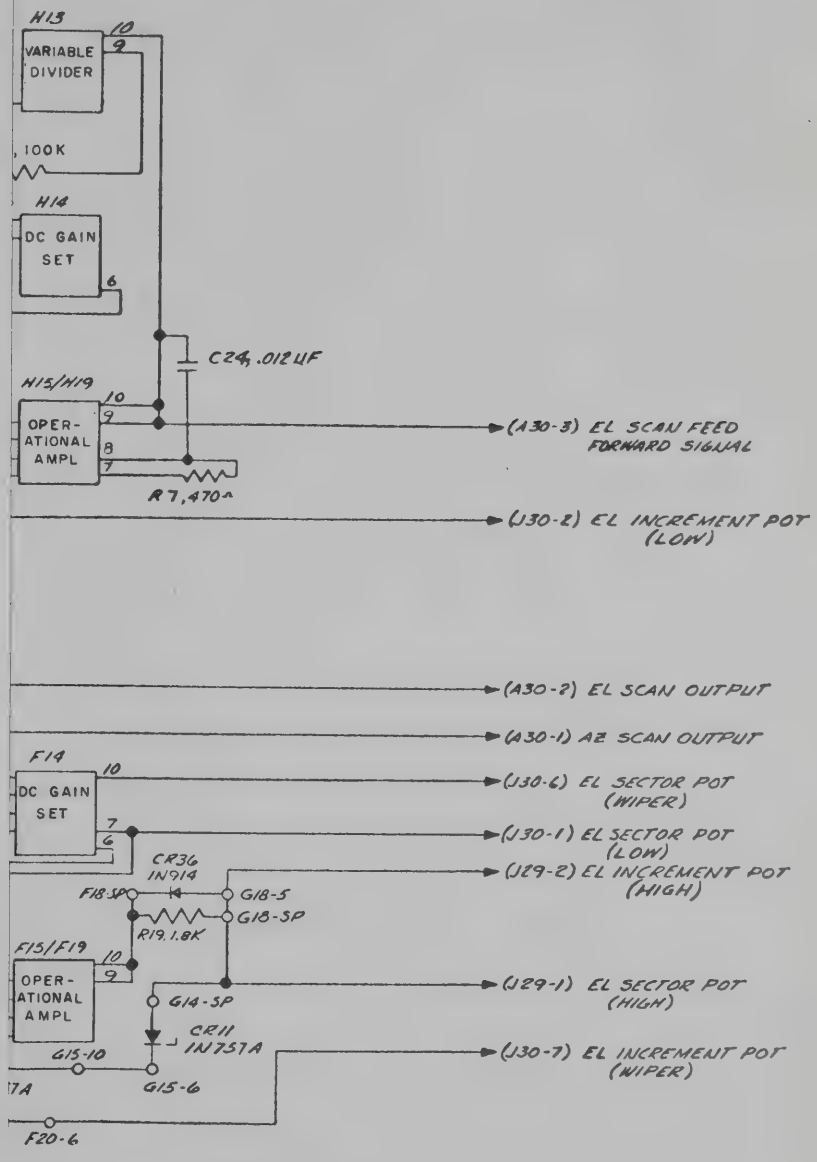


Figure FO 3-9.② Lower module board, schematic diagram (sheet 2 of 4).



EL2LF040

et 3 of 4).

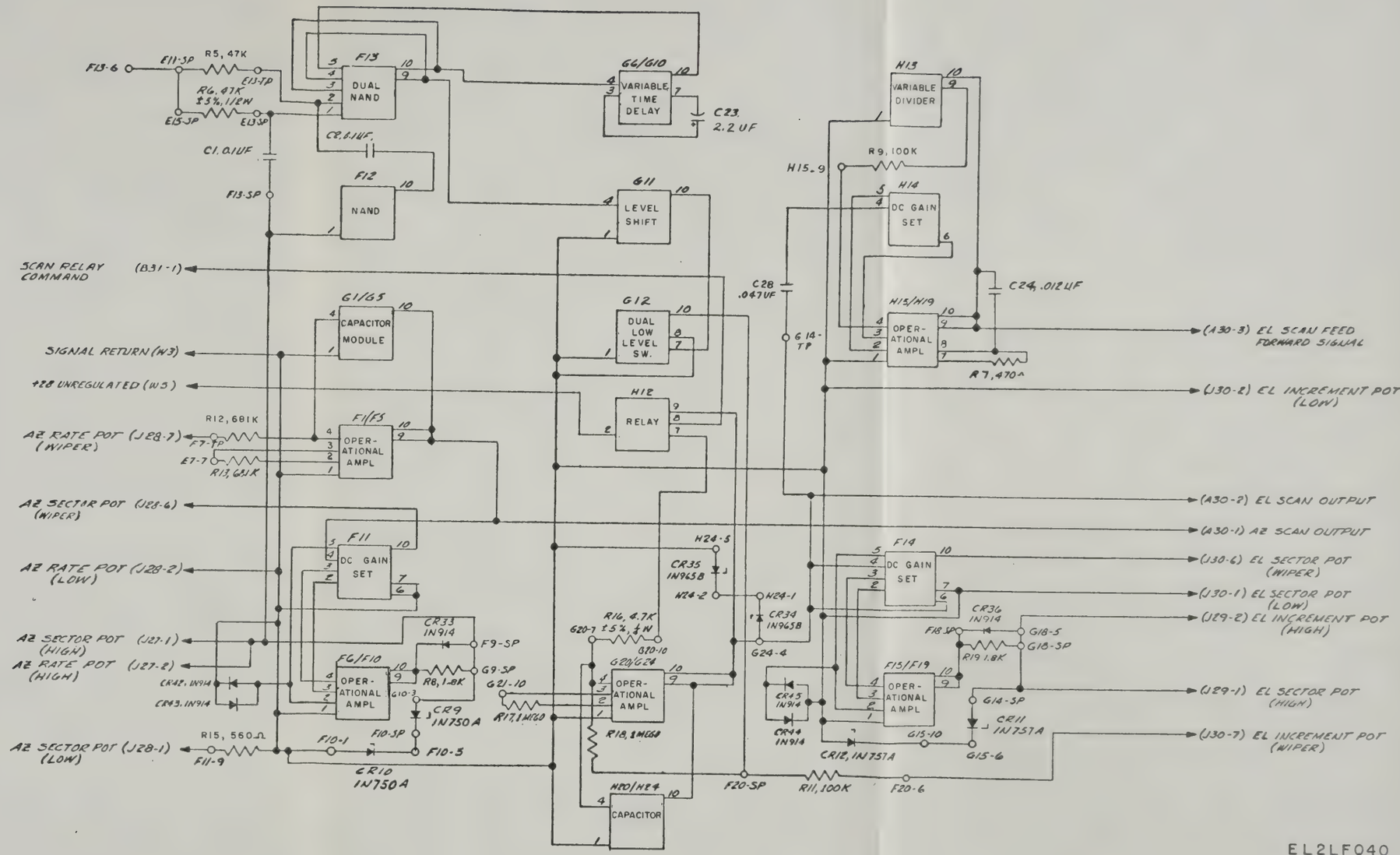


Figure FO 8-9. ③Lower module board, schematic diagram (sheet 8 of 4).

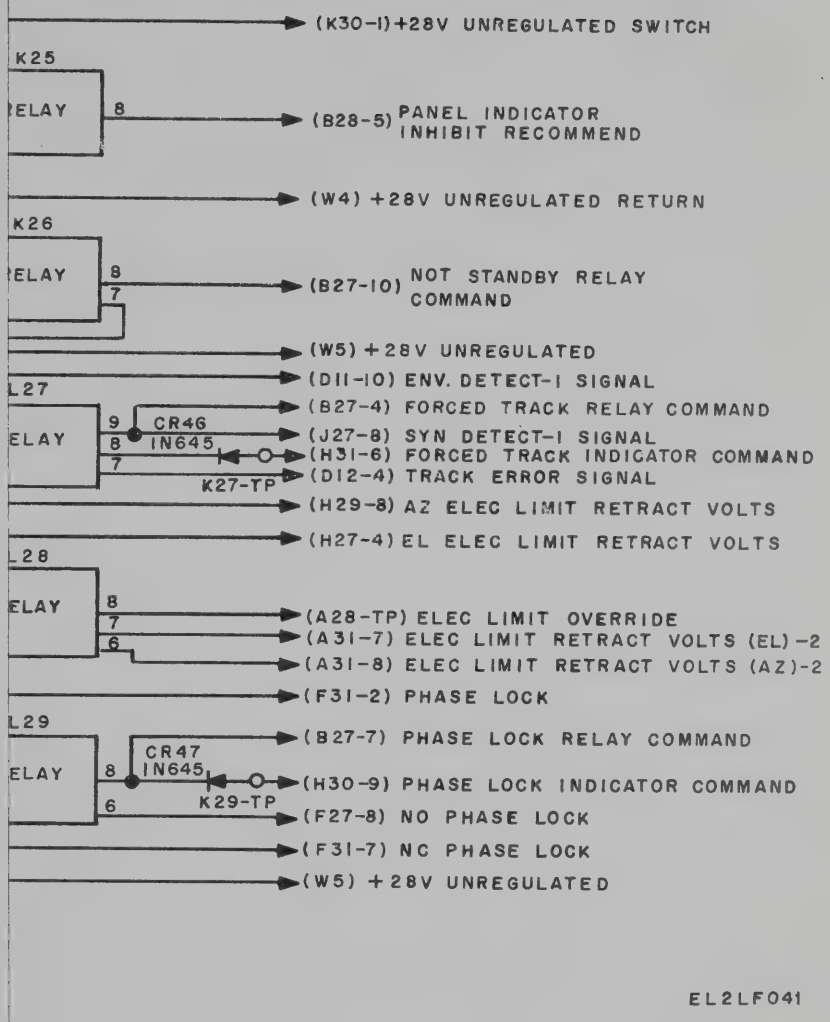


diagram (sheet 4 of 4).

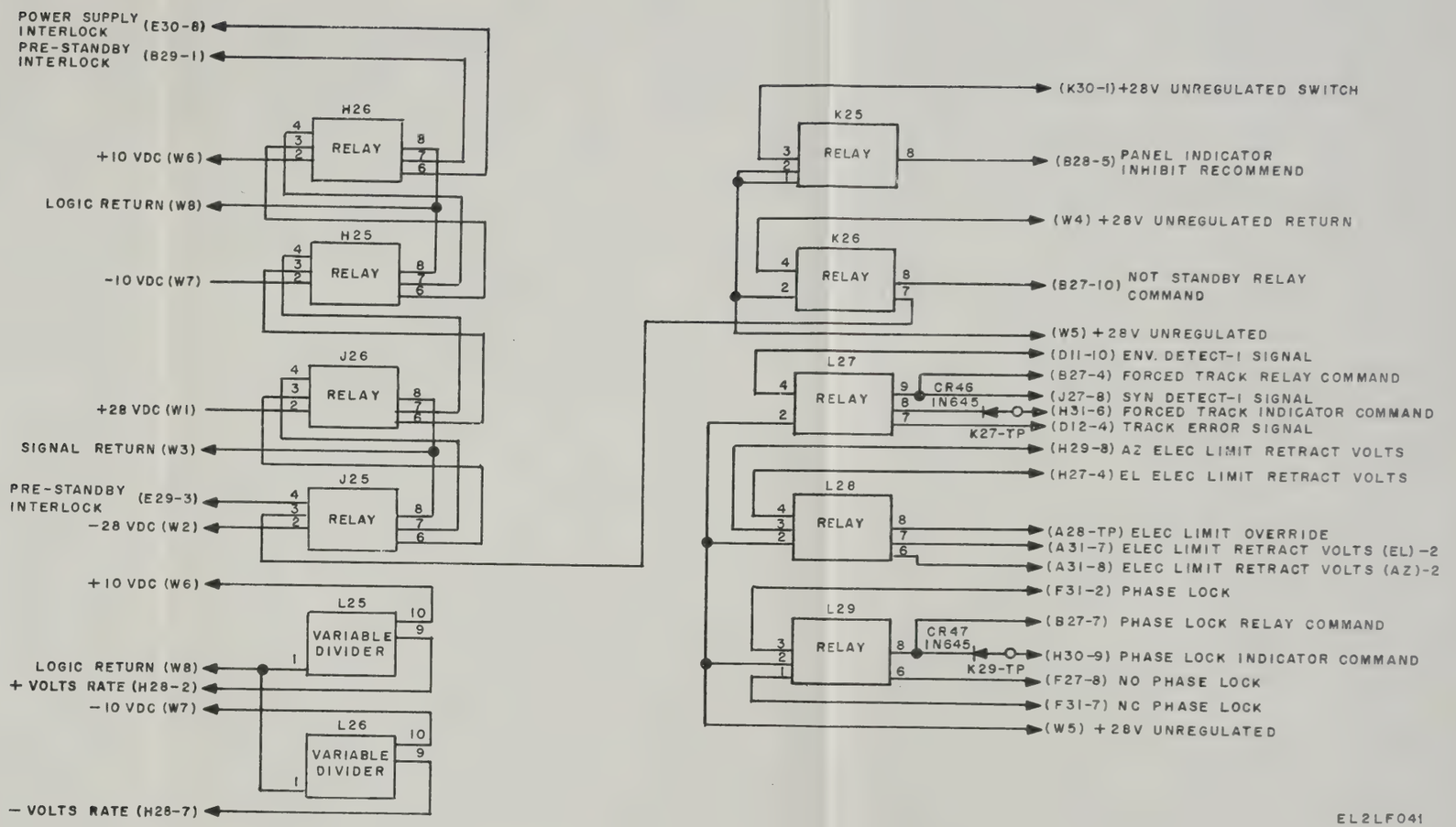
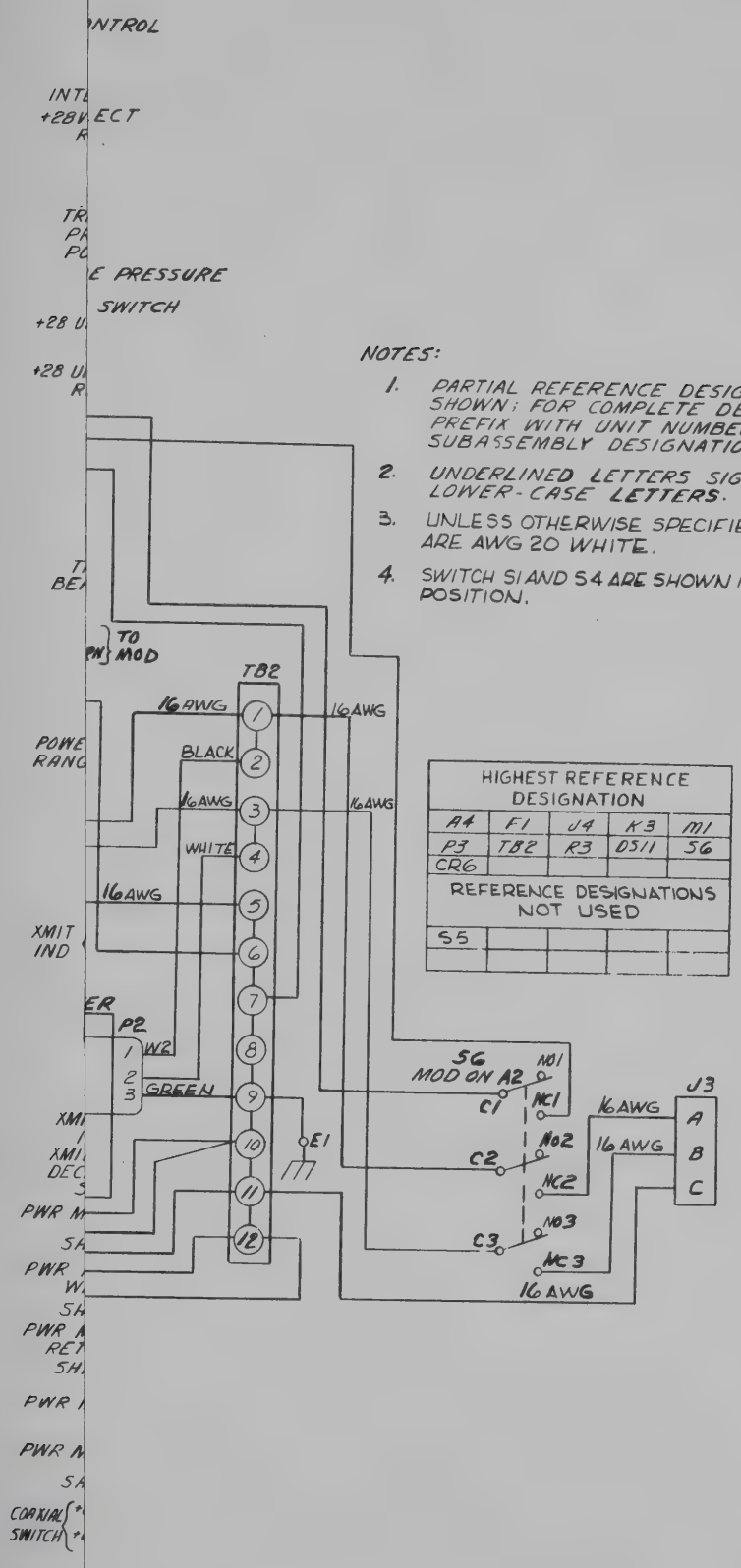


Figure FO 3-9.④Lower module board, schematic diagram (sheet 4 of 4).


NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATIONS.
2. UNDERLINED LETTERS SIGNIFY LOWER-CASE LETTERS.
3. UNLESS OTHERWISE SPECIFIED ALL WIRES ARE AWG 20 WHITE.
4. SWITCH S1 AND S4 ARE SHOWN IN MAINTAINED POSITION.
HIGHEST REFERENCE DESIGNATION
A4 F1 J4 K3 M1
P3 TB2 R3 DS11 S6
CR6
REFERENCE DESIGNATIONS NOT USED
S5
TO MOD
TB2
16 AWG
BLACK
WHITE
GREEN
P2
S6 MOD ON A2
NO1
NC1
C1
NO2
NC2
C2
NO3
NC3
C3
E1
J3
A
B
C
EL2LF046

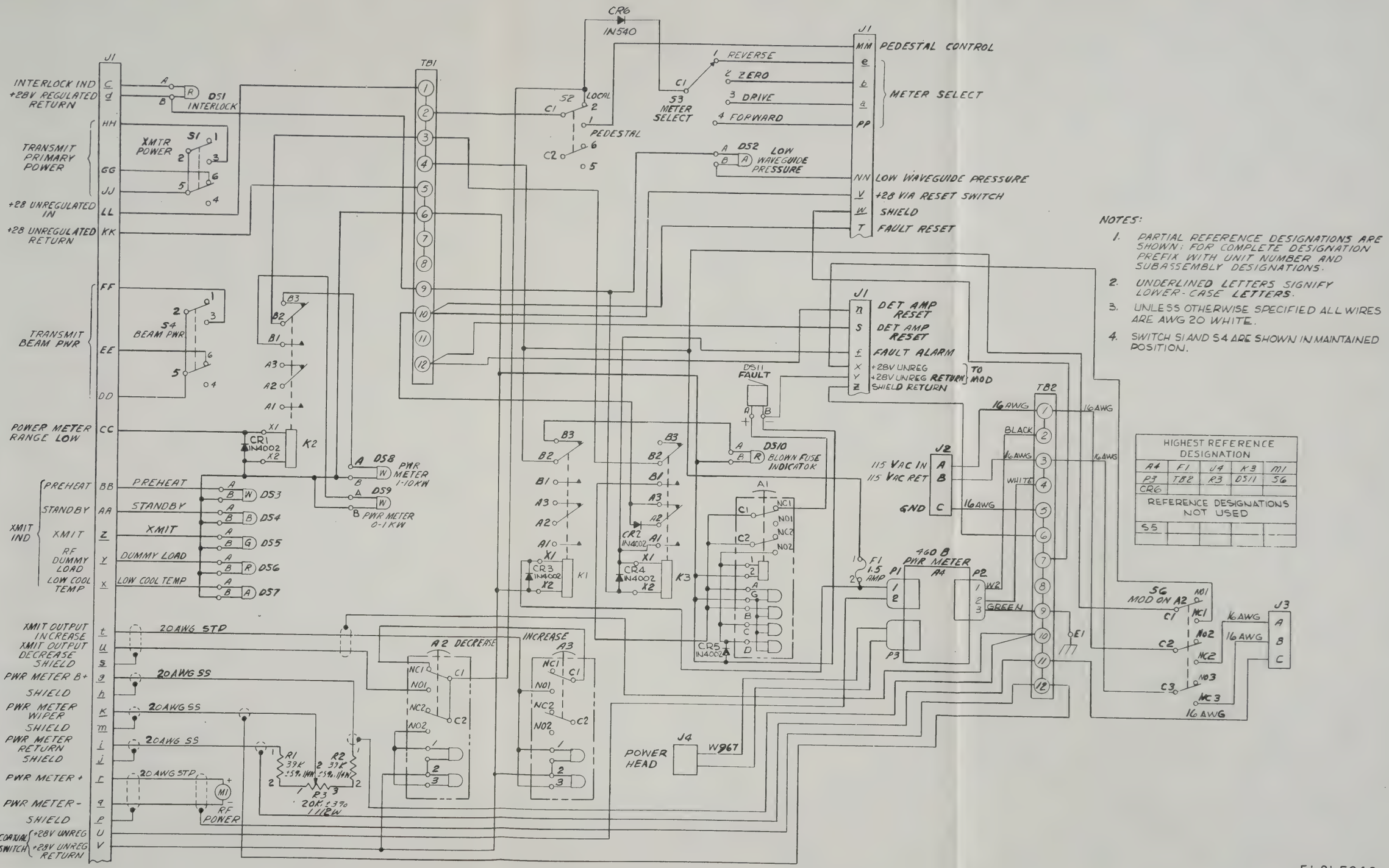
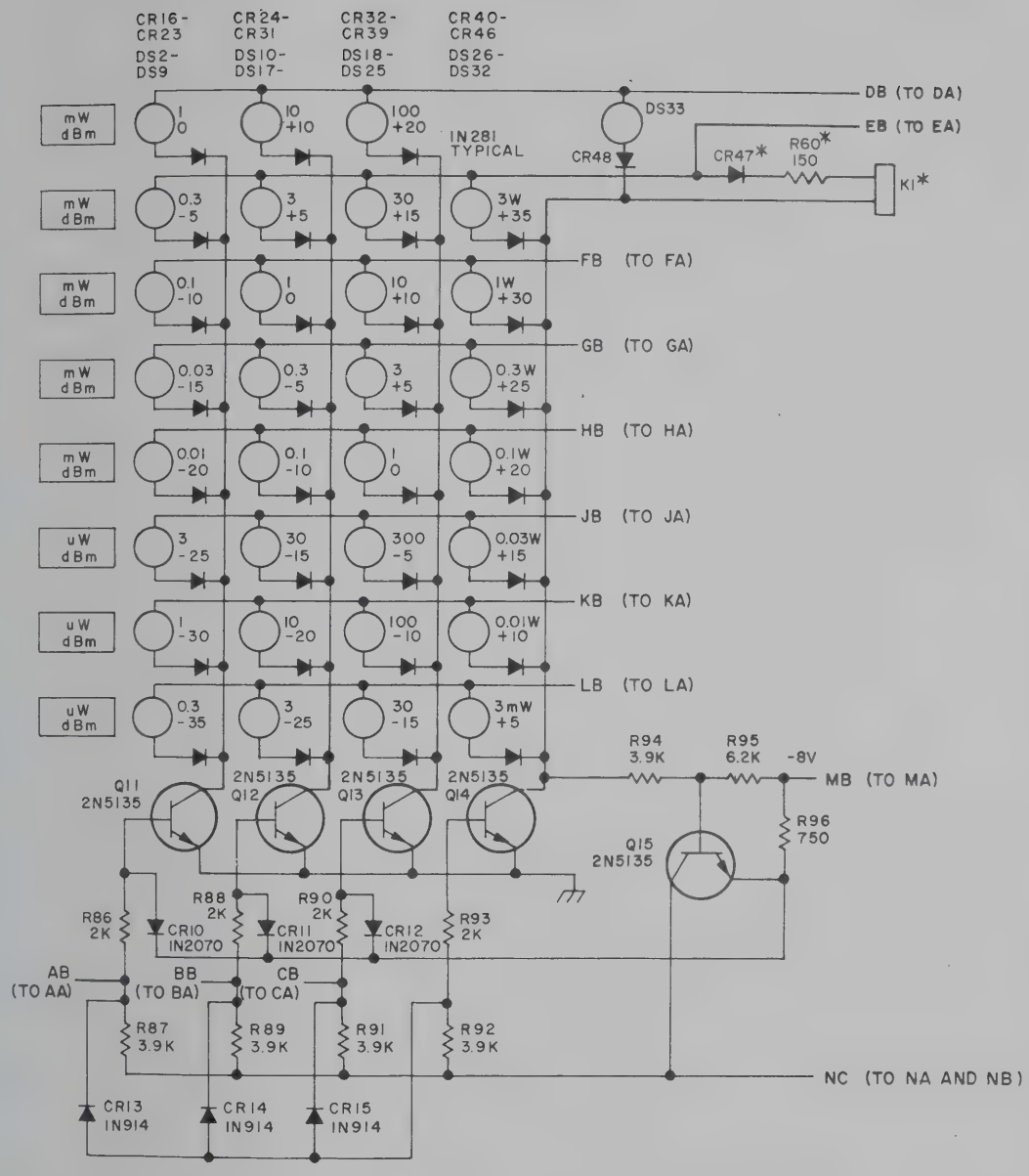


Figure FO 3-10. Rf power monitor and control 1A2A27, schematic diagram.

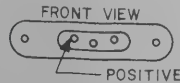


NOTES:

1. J1 AND J2 ARE FRONT AND REAR PANEL INPUT CONNECTORS RESPECTIVELY, AND ARE CONNECTED IN PARALLEL.
2. UNLESS OTHERWISE SPECIFIED :
   RESISTANCES ARE GIVEN IN OHMS
   CAPACITANCES ARE GIVEN IN MICROFARADS
3. WAVEFORM OBSERVED WHEN AR4 IS REMOVED AND TOP RANGE BUTTON IS DEPRESSED.

* INDICATES COMPONENTS USED ONLY IN THE MODEL 460B.

4. WIRING OF CONNECTOR J3 IS SHOWN BELOW;



5. DO NOT MAKE RESISTANCE CHECKS ON TRANSFORMER T1.

EL2LF047

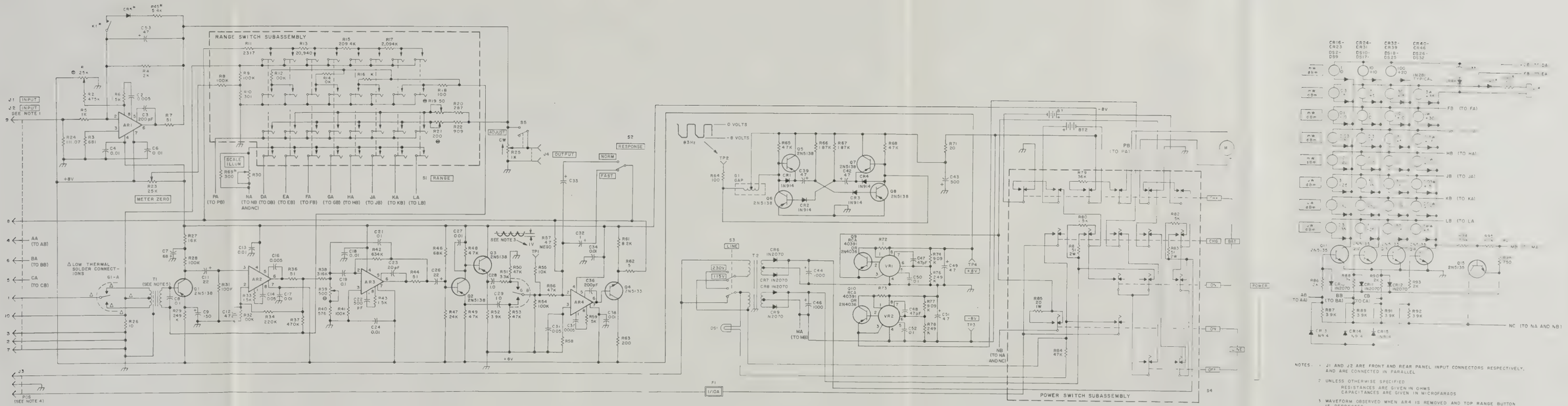
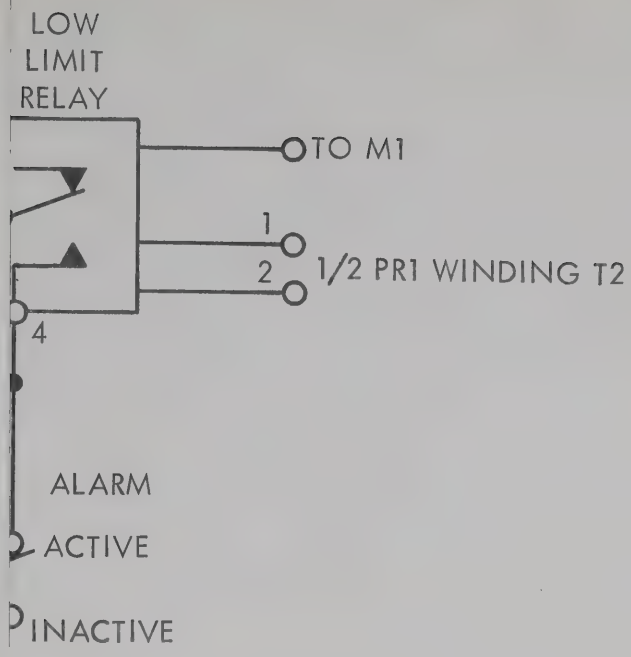


Figure FO3-11. ⑦Rf power meter 1A2A27A4, schematic diagram (sheet 1 of 2).

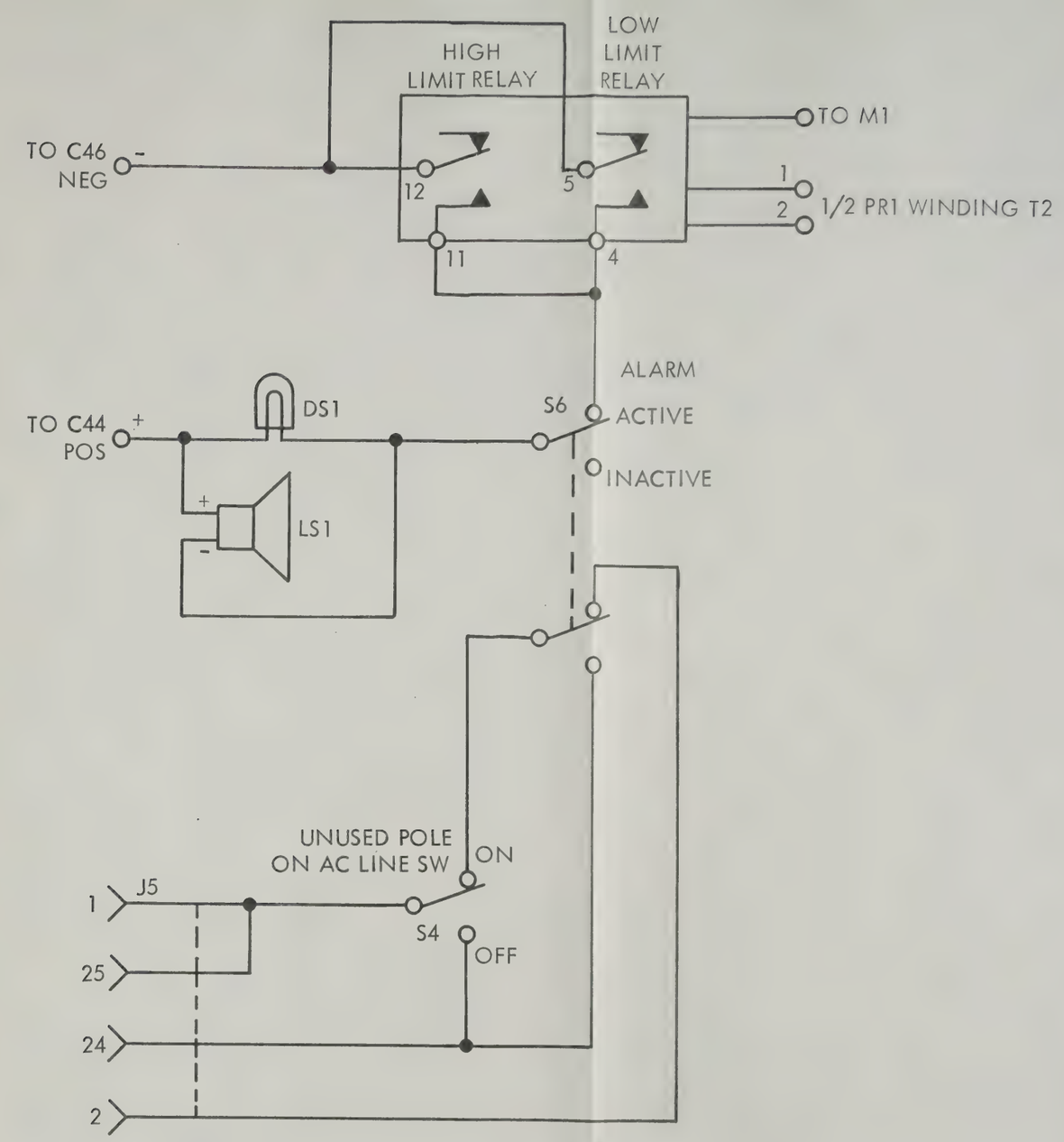


TES:

- RELAYS SHOWN IN UNENERGIZED POSITION.
- J5, PINS 1 AND 2 - NORMALLY CLOSED, OPENS IN ALARM INACTIVE OR AC OFF MODES.
- J5, PINS 24 AND 25 - NORMALLY OPEN, CLOSSES IN ALARM INACTIVE OR AC OFF MODES.
- FOR MAIN SCHEMATIC SEE 5249 OR SCHEMATIC DIAGRAM IN TECHNICAL MANUAL.

EL2LF048

A2A27A4, schematic diagram (sheet 2 of 2).



NOTES:

1 - RELAYS SHOWN IN UNENERGIZED POSITION.

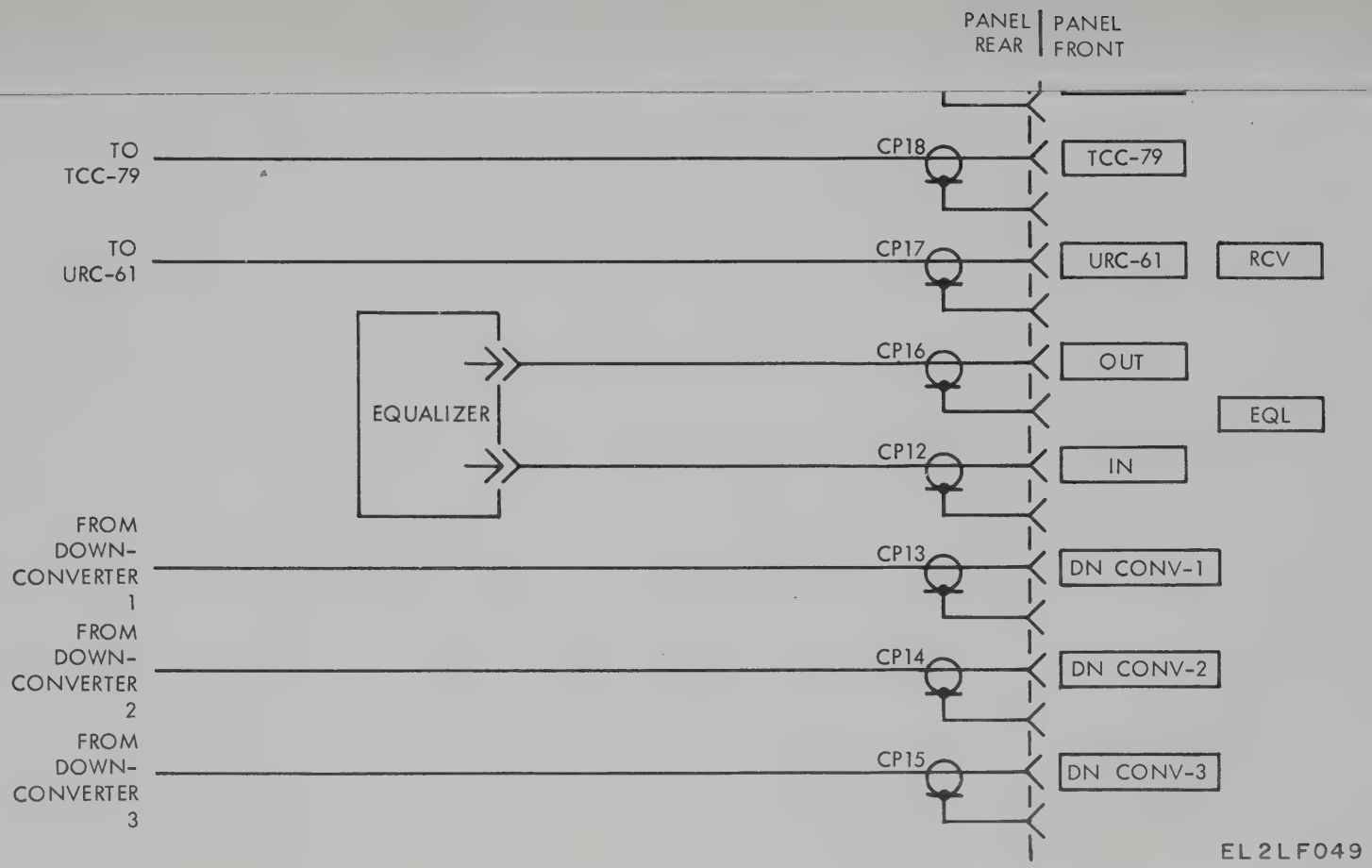
2 - J5, PINS 1 AND 2 - NORMALLY CLOSED, OPENS IN ALARM INACTIVE OR AC OFF MODES.

3 - J5, PINS 24 AND 25 - NORMALLY OPEN, CLOSSES IN ALARM INACTIVE OR AC OFF MODES.

4 - FOR MAIN SCHEMATIC SEE 5249 OR SCHEMATIC DIAGRAM IN TECHNICAL MANUAL.

EL2LF048

Figure FO 3-11.②Rf power meter 1A2A27A4, schematic diagram (sheet 2 of 2).


PANEL REAR
PANEL FRONT
TO TCC-79
CP18
TCC-79
TO URC-61
CP17
URC-61
RCV
CP16
OUT
EQUALIZER
EQL
CP12
IN
FROM DOWN-CONVERTER 1
CP13
DN CONV-1
FROM DOWN-CONVERTER 2
CP14
DN CONV-2
FROM DOWN-CONVERTER 3
CP15
DN CONV-3
EL2LF049

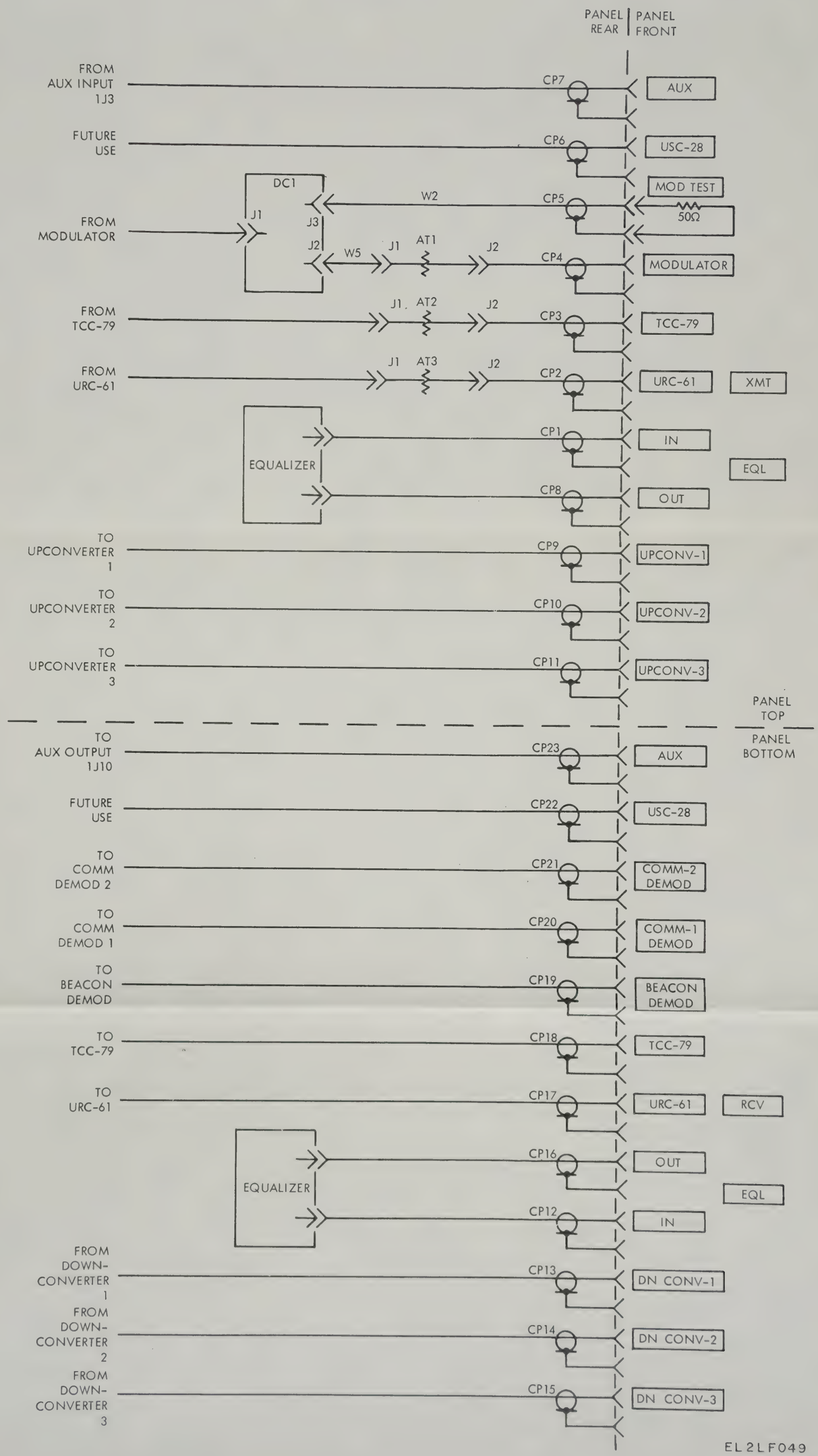
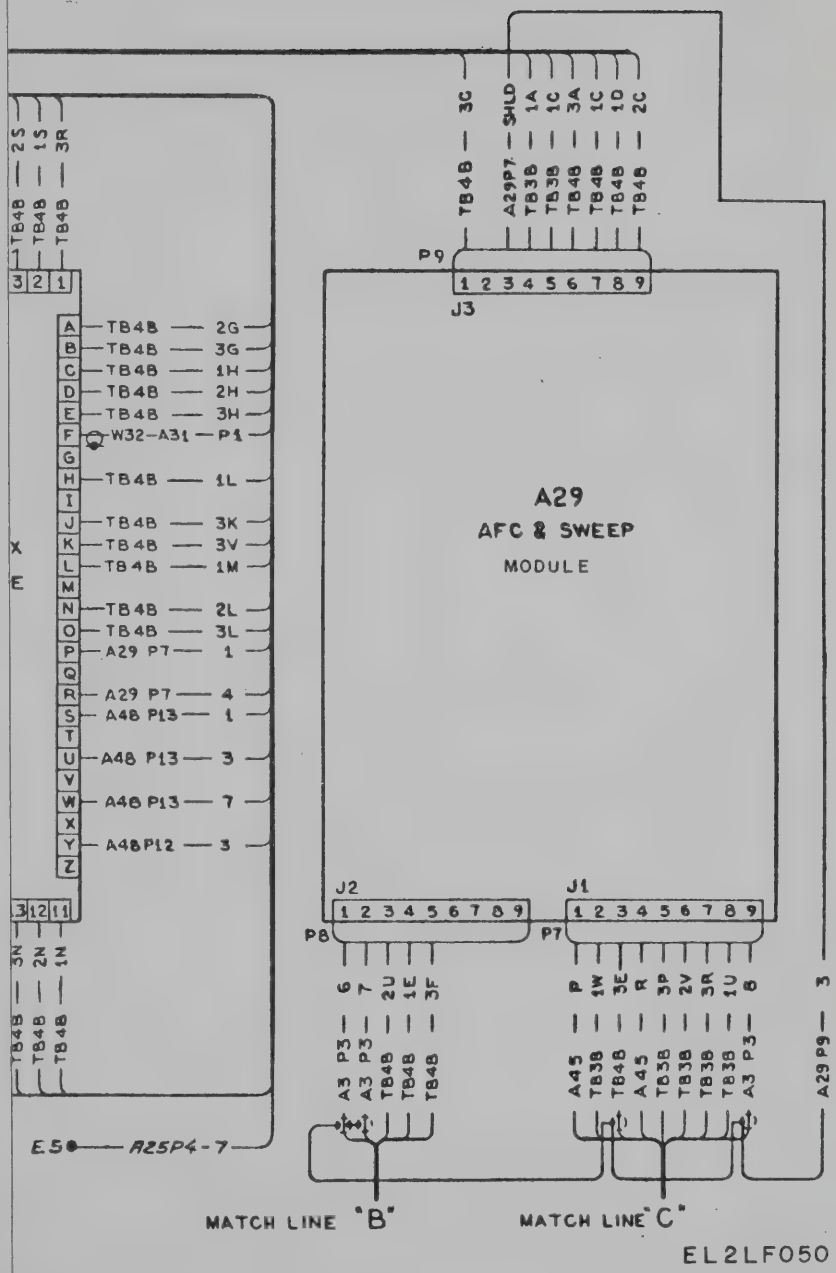


Figure FO 3-12. If patching panel 1A3A22, cabling diagram.

TED

, J4
AMPLIFIER A21.
PECTIVELY OF



1 of 10).

NOTES:

1. ▭ INDICATES EQUIPMENT MARKING.
2. MONITOR POINT NORMALLY TERMINATED IN 50 OHM COAXIAL TERMINATION.
3. A14 IS A 90° PHASE SHIFT ASSEMBLY.
4. P1 OF A18, A19, A20, A49 CONNECTED TO J3, J4 J5, J6 RESPECTIVELY OF 21.4 MHz LOOP AMPLIFIER A21.
5. P1 OF A41, A42 CONNECTED TO J3, J4 RESPECTIVELY OF 1.4MHz LOOP AMPLIFIER A40.

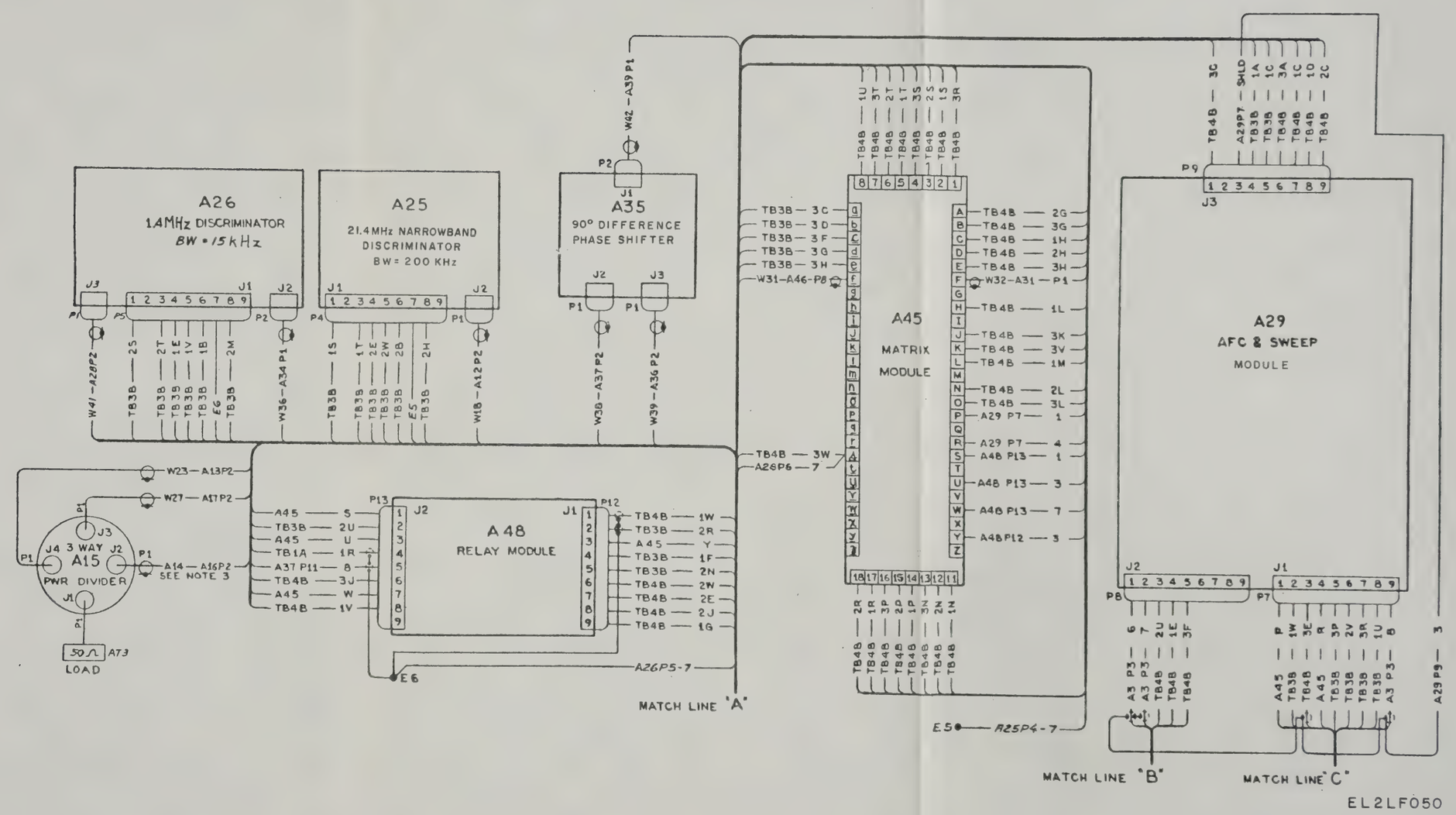
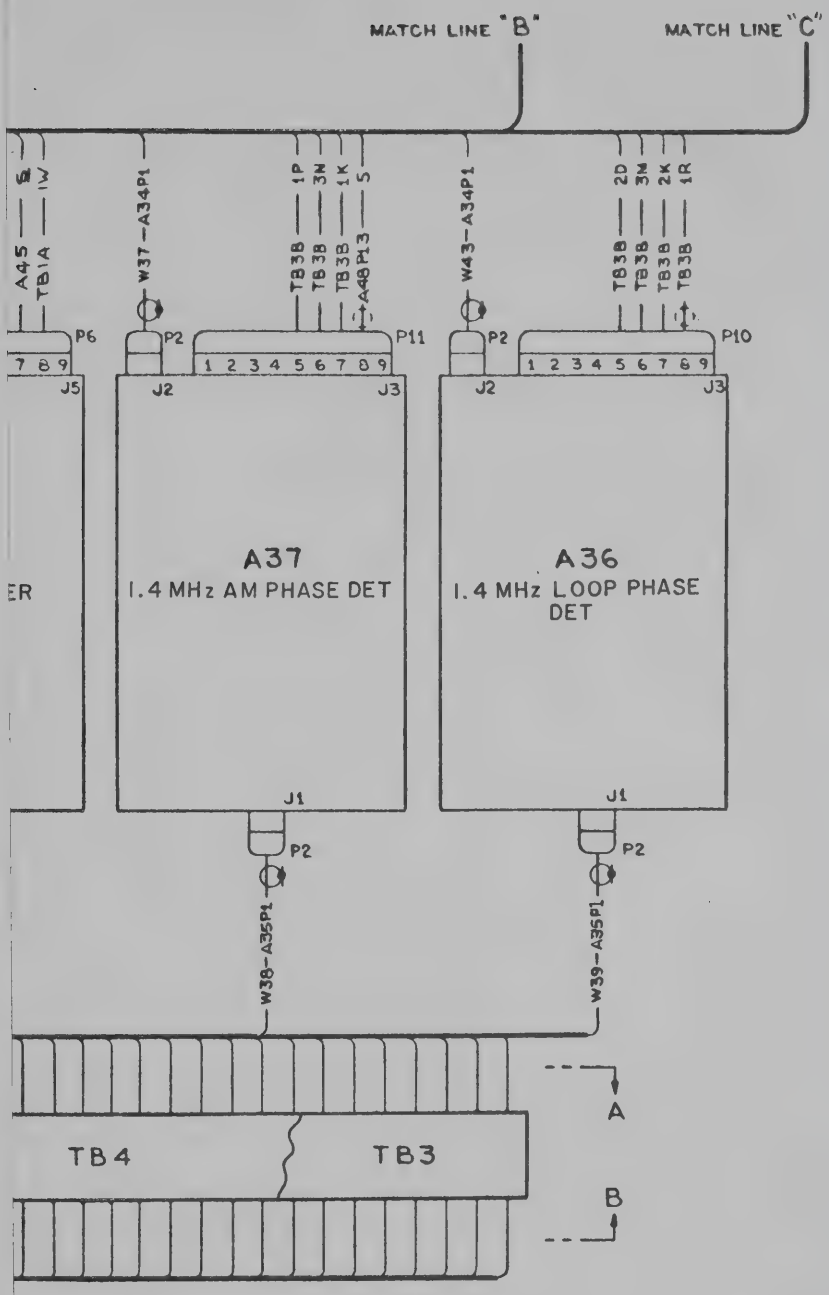


Figure FO 3-13. ①Comm demod 1A3A3, wiring diagram (sheet 1 of 10).


MATCH LINE "B"
MATCH LINE "C"
A45
TB1A
1W
W37-A34P1
TB38
1P
3N
1K
5
A48P13
W43-A34P1
TB38
2D
3M
2K
1R
P6
P2
P11
P2
P10
J5
J2
J3
J2
J3
A37
1.4 MHz AM PHASE DET
A36
1.4 MHz LOOP PHASE DET
J1
P2
J1
P2
W38-A35P1
W39-A35P1
TB4
TB3
A
B
EL2LF051

eet 2 of 10).

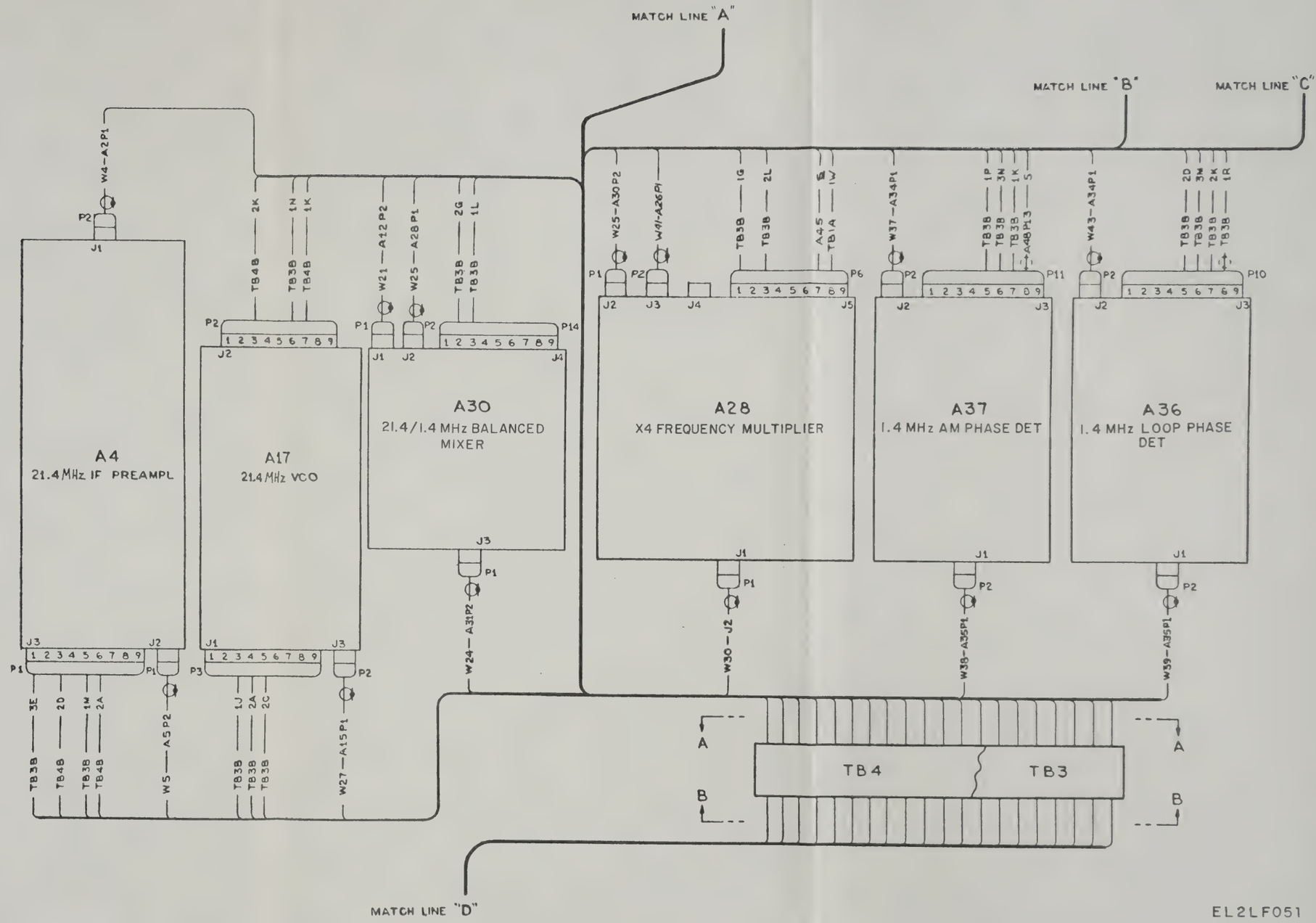
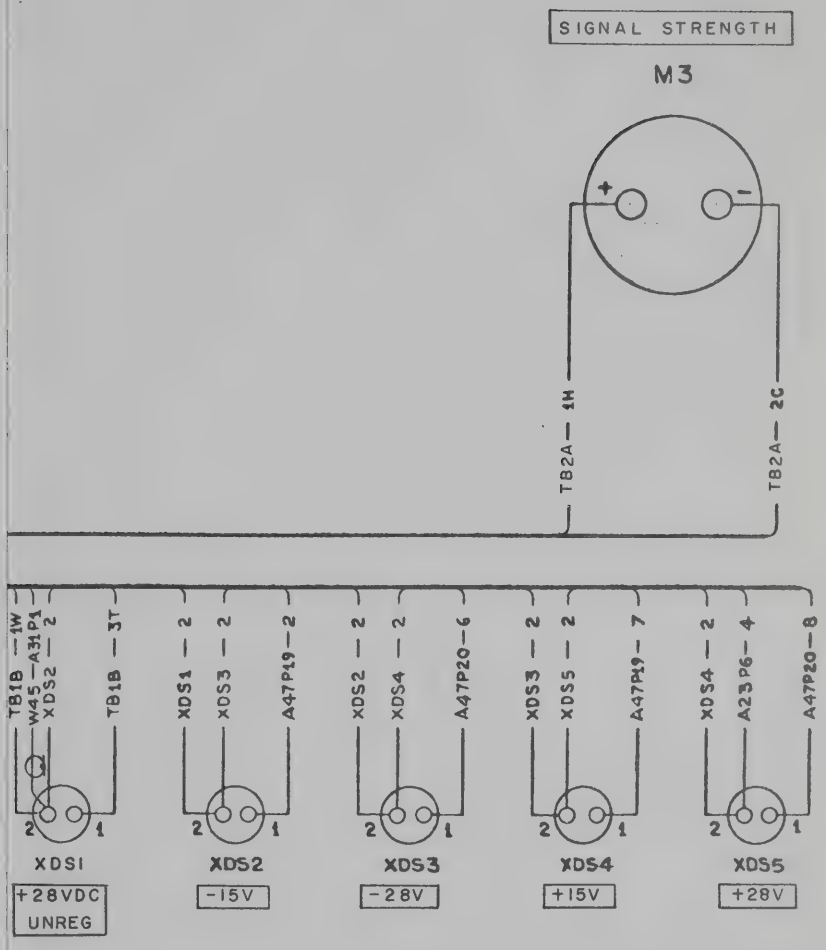


Figure FO 3-13.② Comm demod 1A3A3, wiring diagram (sheet 2 of 10).



EL2LF052

am (sheet 3 of 10).

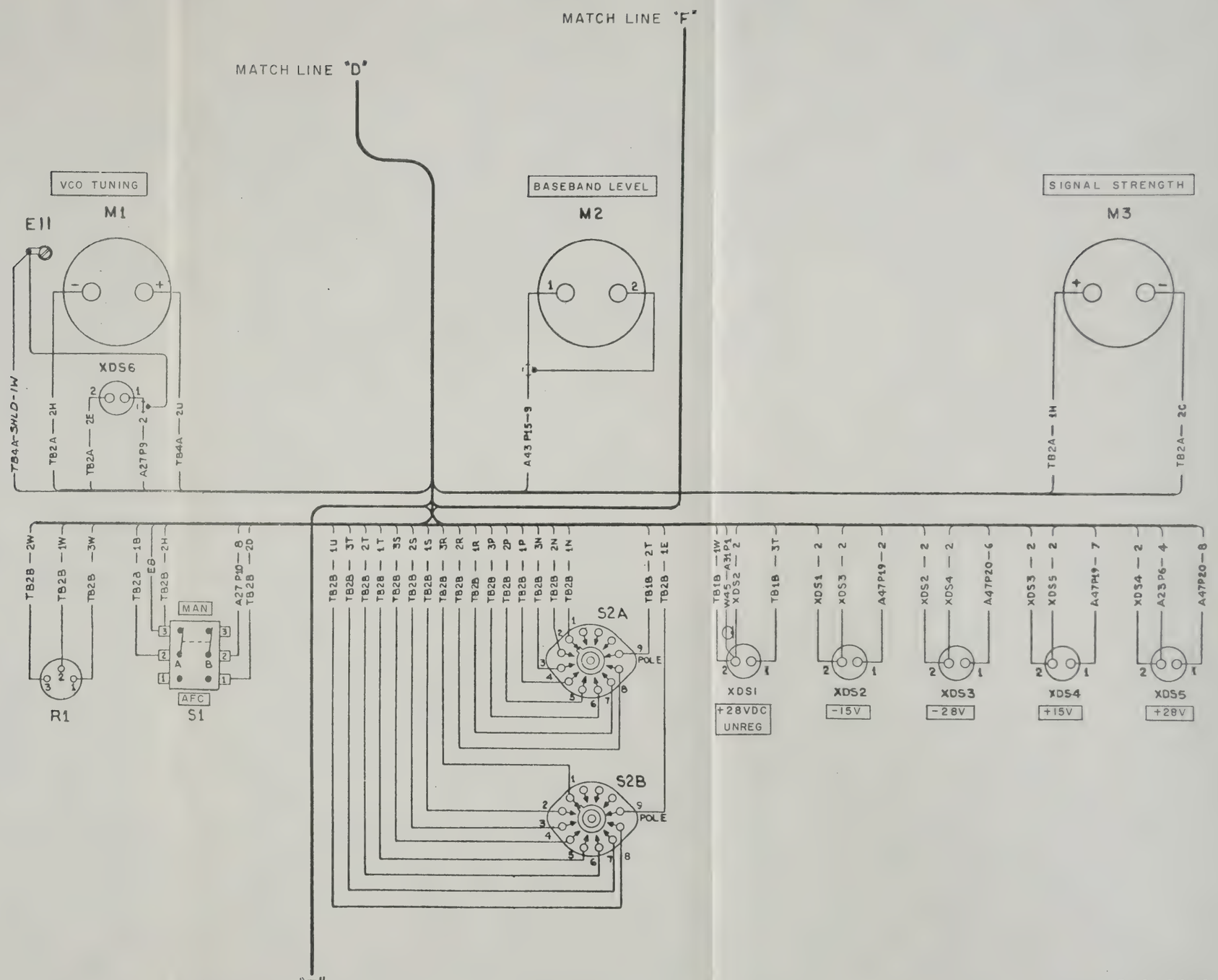
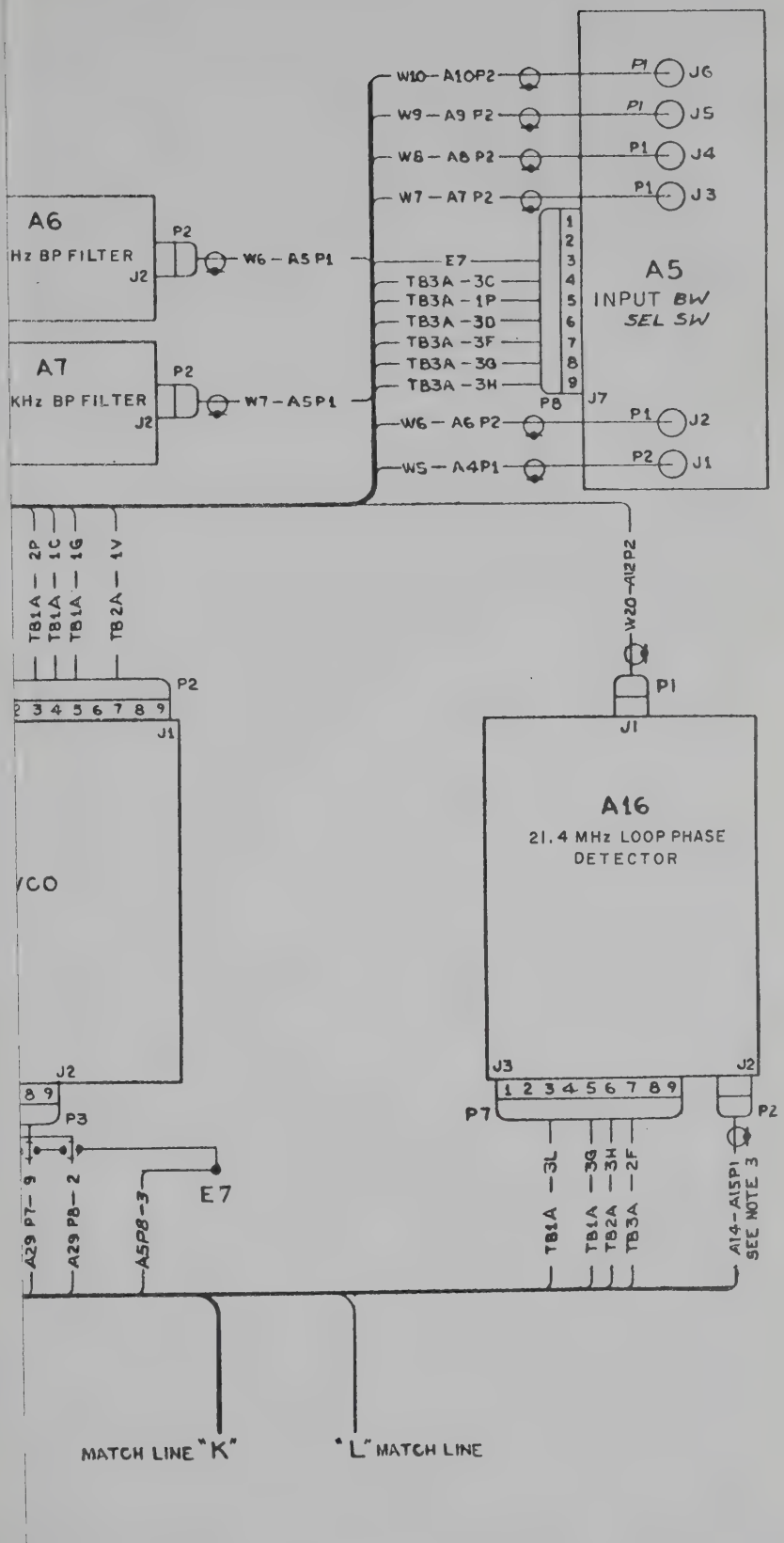


Figure FO 3-13.③ Comm demod 1A3A3, wiring diagram (sheet 3 of 10).


A6
Hz BP FILTER
J2
P2
W6 – A5 P1
A7
KHz BP FILTER
J2
P2
W7 – A5P1
W10 – A10P2
W9 – A9 P2
W8 – A8 P2
W7 – A7 P2
E7
TB3A – 3C
TB3A – 1P
TB3A – 3D
TB3A – 3F
TB3A – 3G
TB3A – 3H
P8
J7
W6 – A6 P2
W5 – A4P1
P1
J6
P1
J5
P1
J4
P1
J3
P1
J2
P2
J1
A5
INPUT BW
SEL SW
TB1A – 2P
TB1A – 1C
TB1A – 1G
TB2A – 1V
P2
J1
VCO
J2
P3
A29 P7 – 9
A29 P8 – 2
A5P8 – 3
E7
W20 – A12 P2
P1
J1
A16
21.4 MHz LOOP PHASE
DETECTOR
J3
J2
P7
P2
TB1A – 3L
TB1A – 3G
TB2A – 3H
TB3A – 2F
A14 – A15P1
SEE NOTE 3
MATCH LINE "K"
"L" MATCH LINE
EL2LF053

f 10).

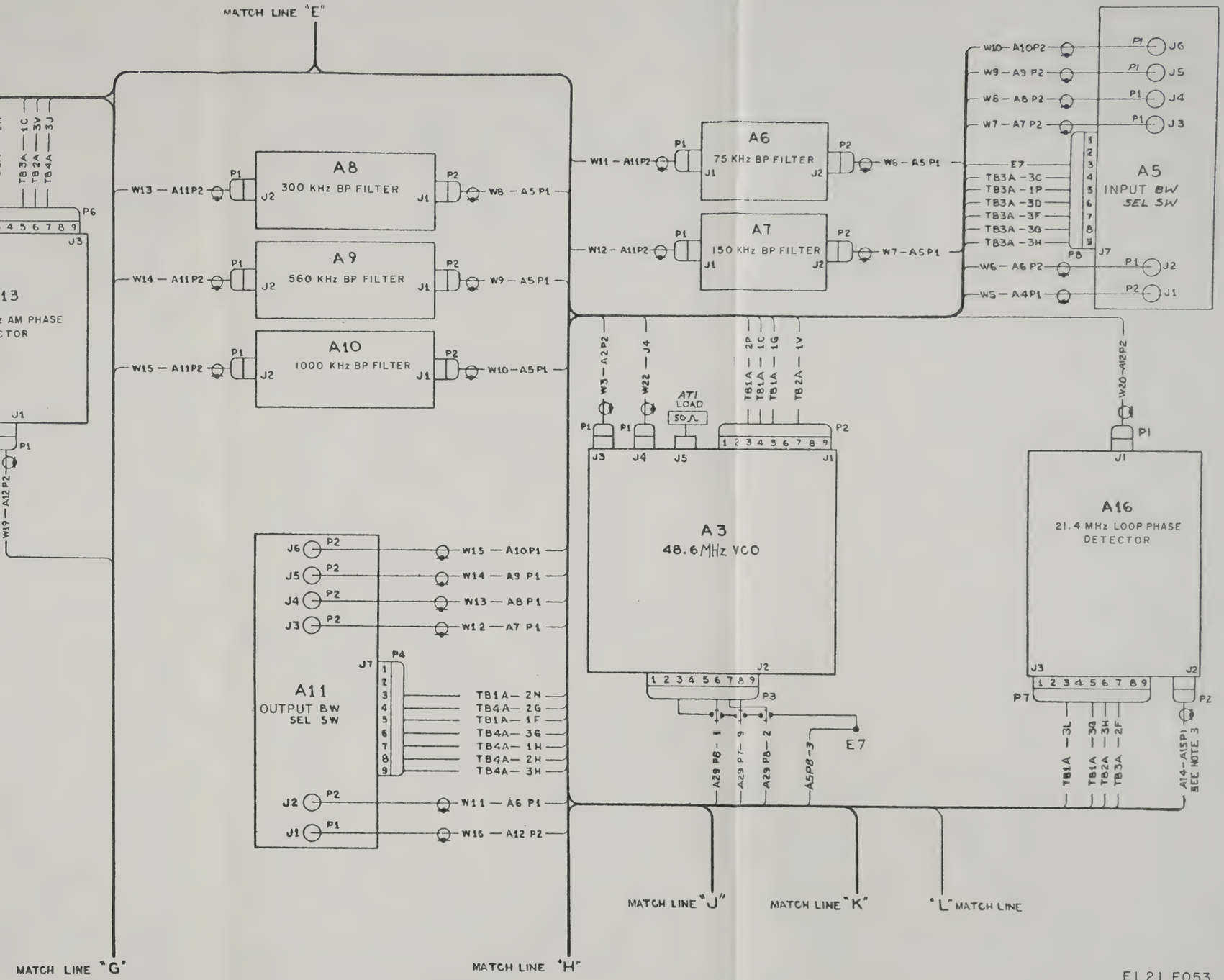
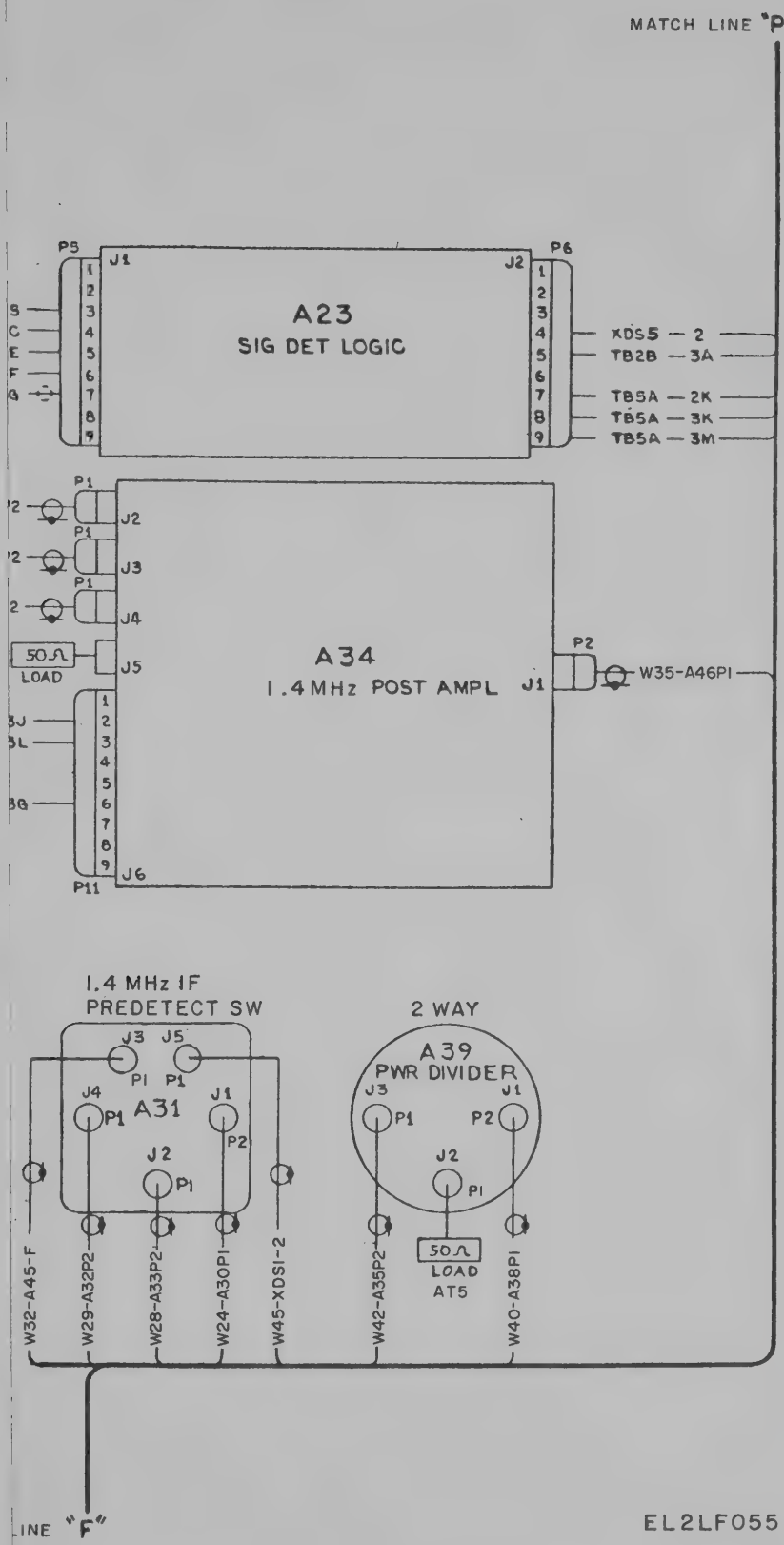


Figure FO 3-13.① Comm demod 1A3A3, wiring diagram (sheet 4 of 10).

ram (sheet 5 of 10).

Figure FO 3-13. ⑤Comm demod 1A3A3, wiring diagram (sheet 5 of 10).


MATCH LINE "P"
P5
J1
A23
SIG DET LOGIC
J2
P6
XDS5 — 2
TB2B — 3A
TB5A — 2K
TB5A — 3K
TB5A — 3M
P1
J2
J3
J4
50Ω
LOAD
J5
A34
1.4 MHz POST AMPL
J1
P2
W35-A46P1
J6
P11
1.4 MHz IF
PREDETECT SW
J3
J5
P1
P1
J4
P1
A31
J1
P2
J2
P1
2 WAY
A39
PWR DIVIDER
J3
P1
J1
P2
J2
P1
50Ω
LOAD
AT5
W32-A45-F
W29-A32P2
W28-A33P2
W24-A30P1
W45-XDS1-2
W42-A35P2
W40-A38P1
LINE "F"
EL2LF055

(sheet 6 of 10).

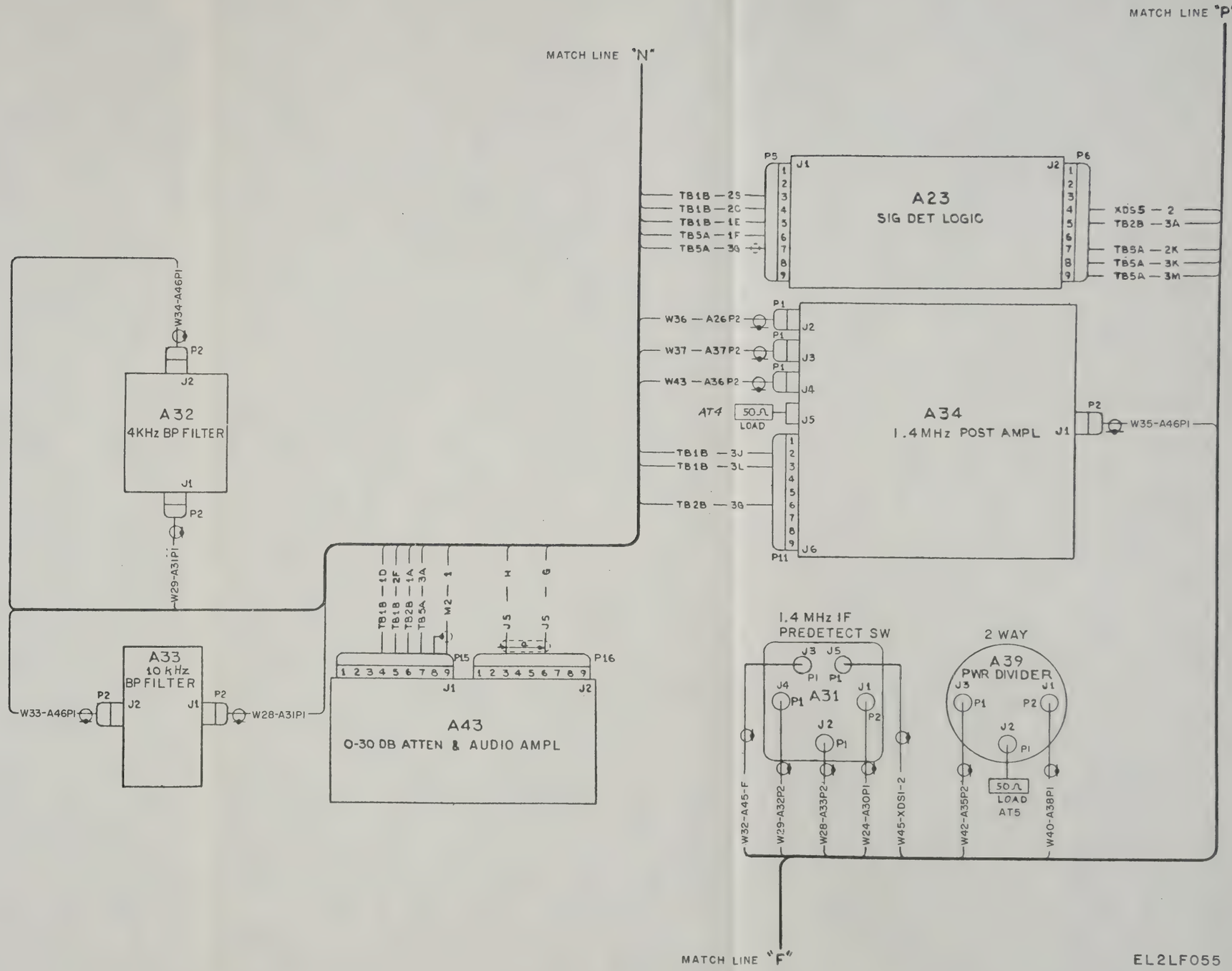
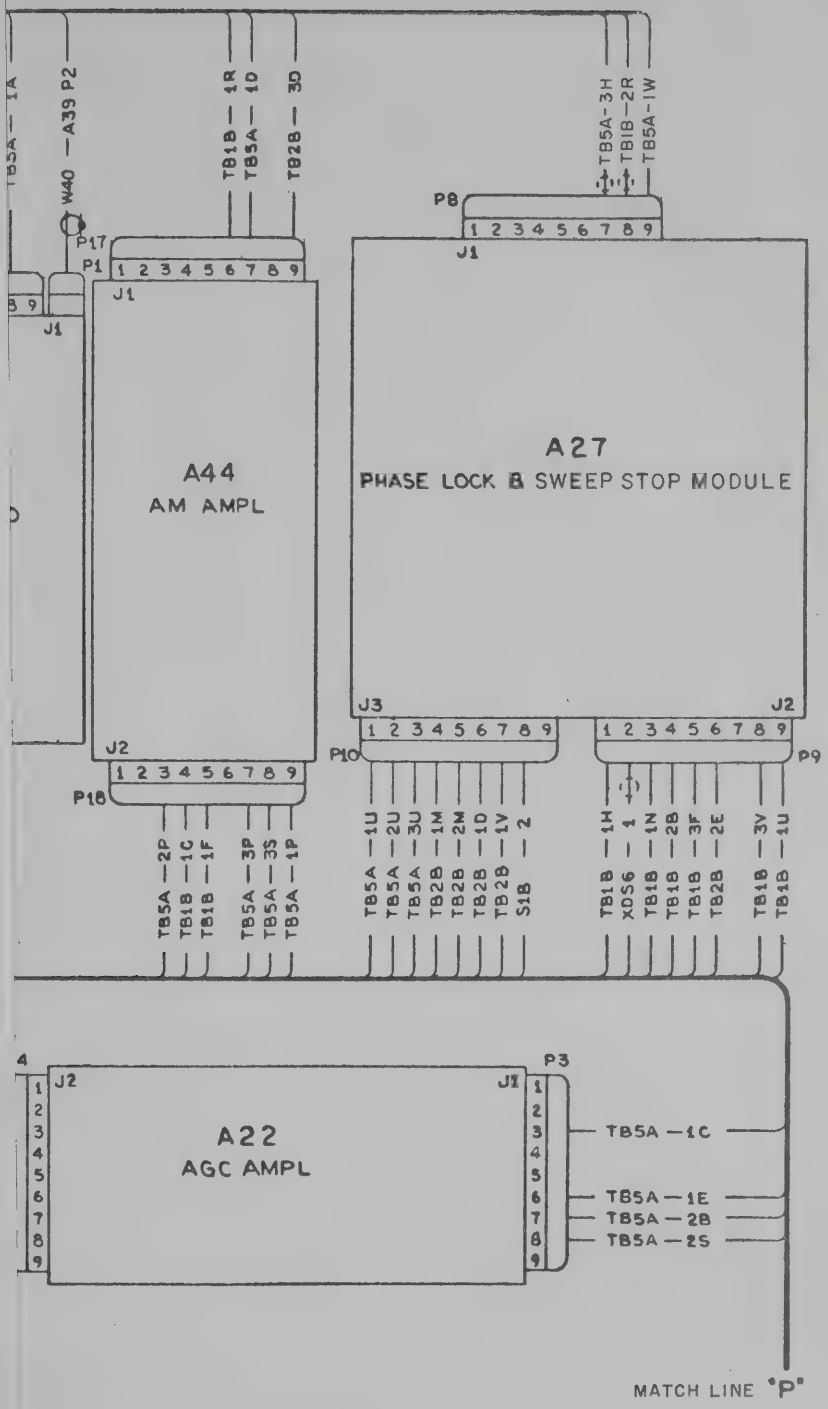


Figure FO 3-13. ⑥ Comm demod 1A3A3, wiring diagram (sheet 6 of 10).



EL2LF056

(Sheet 7 of 10).

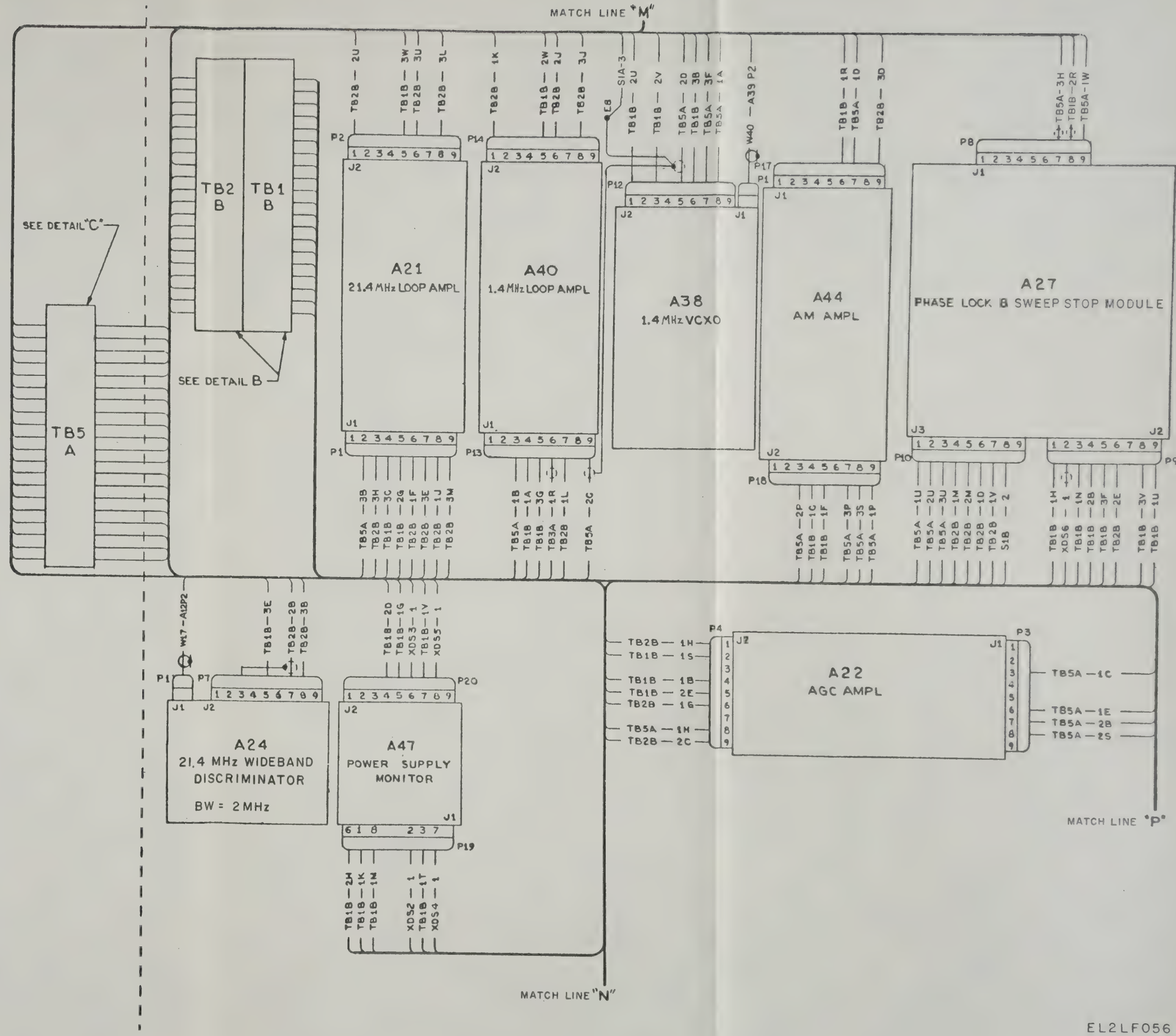
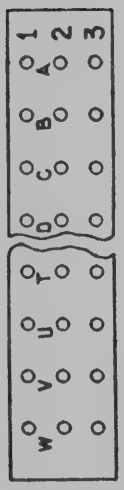
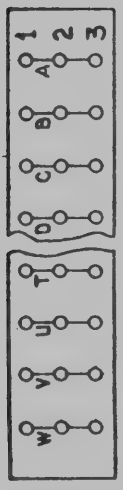


Figure FO 3-13. ⑦ Comm demond 1A3A3, wiring diagram (sheet 7 of 10).



TB2

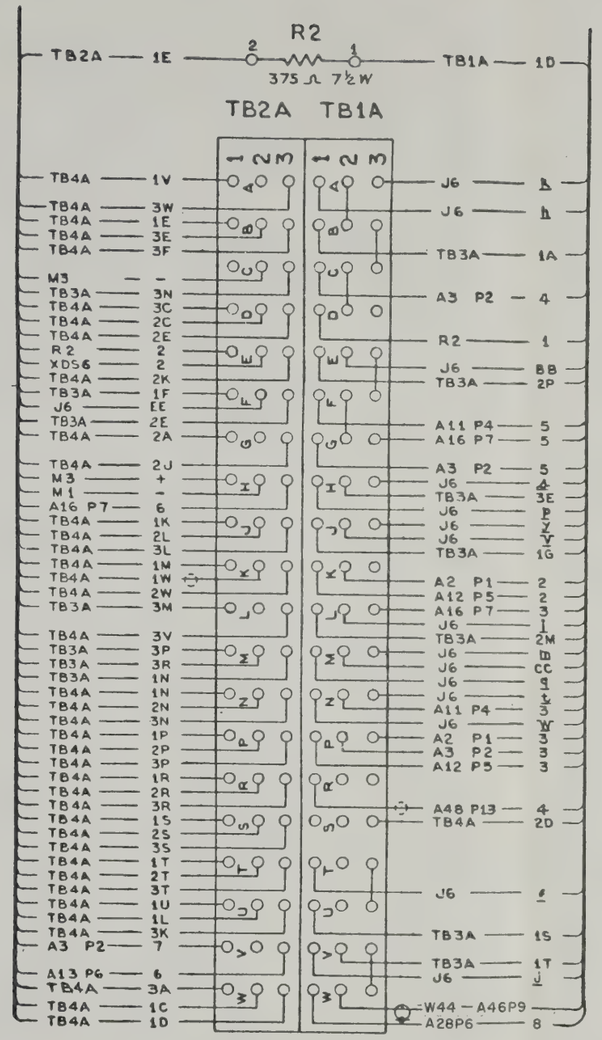
NO INTERNAL CONNECTIONS



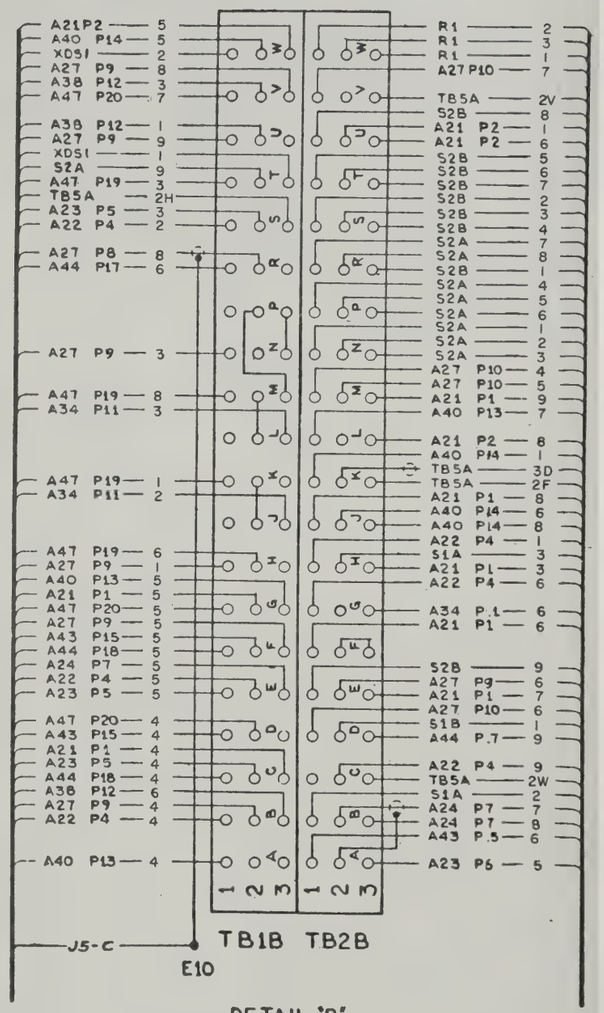
TB1

TYP INTERNAL CONNECTIONS

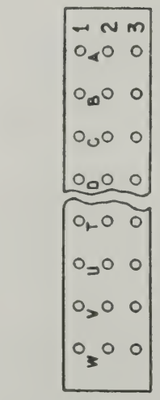
EL2LF057



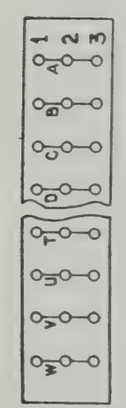
DETAIL "A"



DETAIL "B"



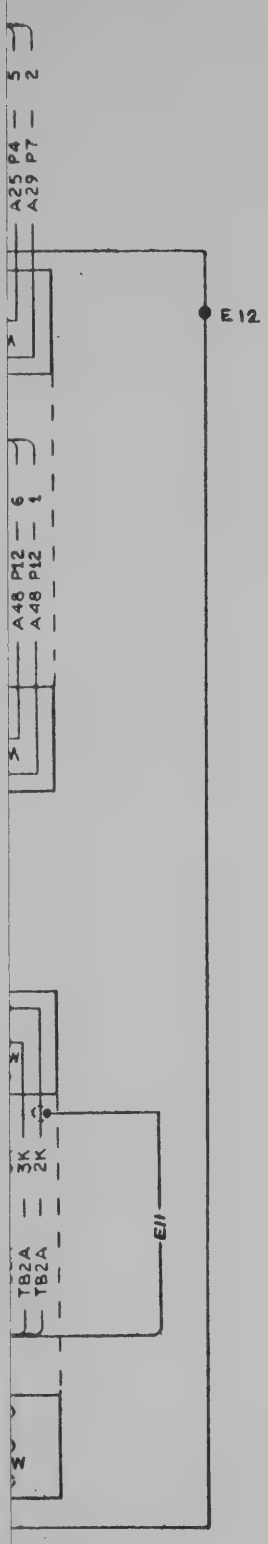
NO INTERNAL CONNECTIONS

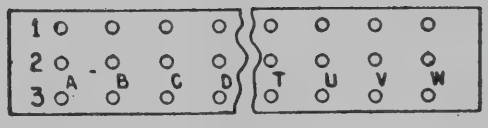


TYP INTERNAL CONNECTIONS

EL2LF057

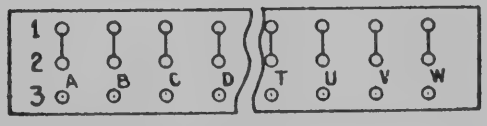
Figure FO 3-13. ⑧ *Comm demod 1A3A3, wiring diagram (sheet 8 of 10).*





TB4

NO INTERNAL CONNECTIONS



TB3

TYP INTERNAL CONNECTIONS

EL2LF058

am (sheet 9 of 10).

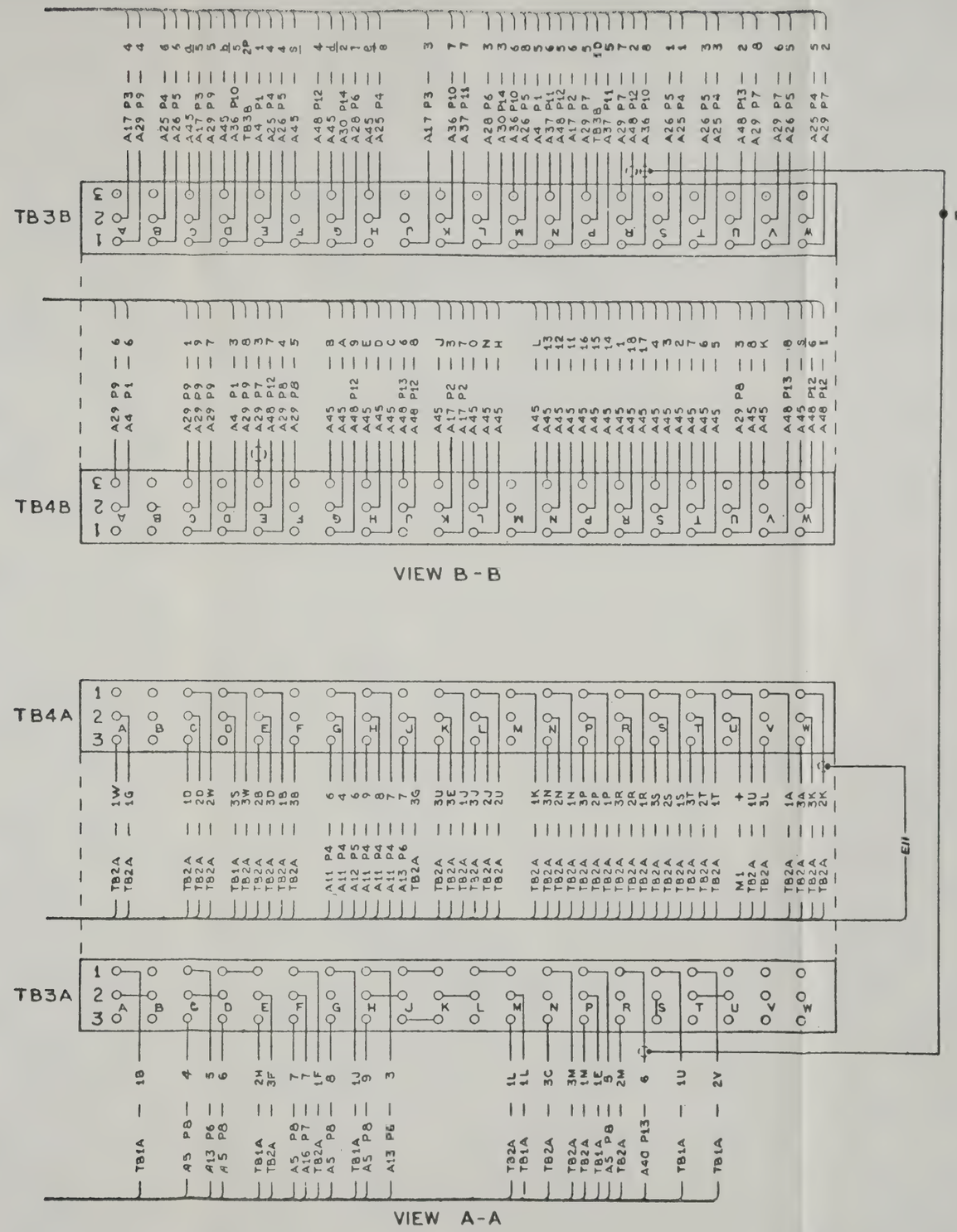
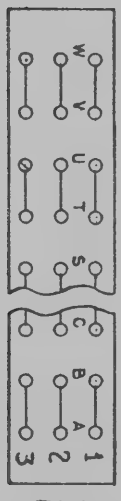


Figure FO 3-13.⑨Comm demod 1A3A3, wiring diagram (sheet 9 of 10).



TB5

TYP INTERNAL CONNECTIONS

EL2LF059

A3A3, wiring diagram (sheet 10 of 10).

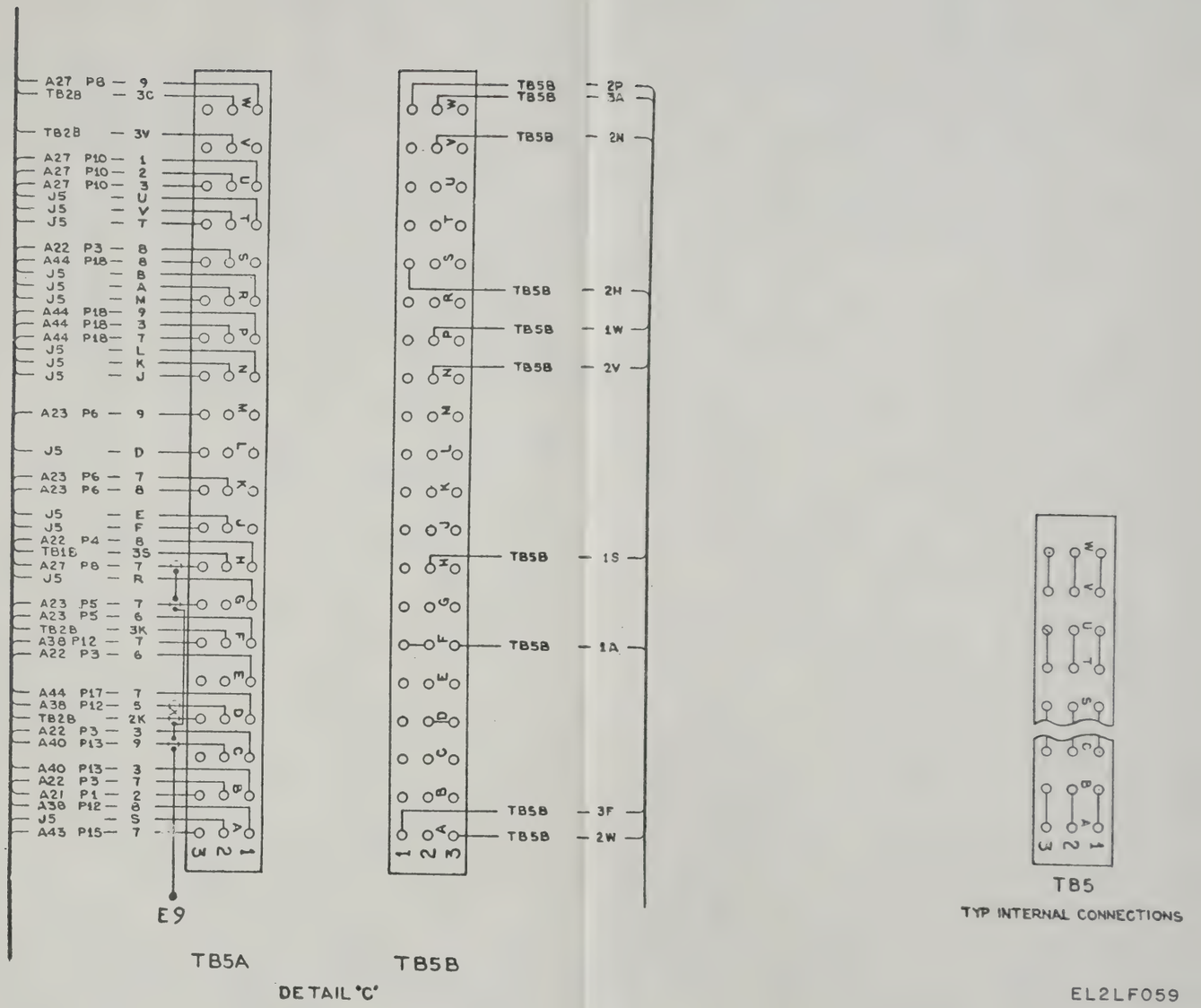
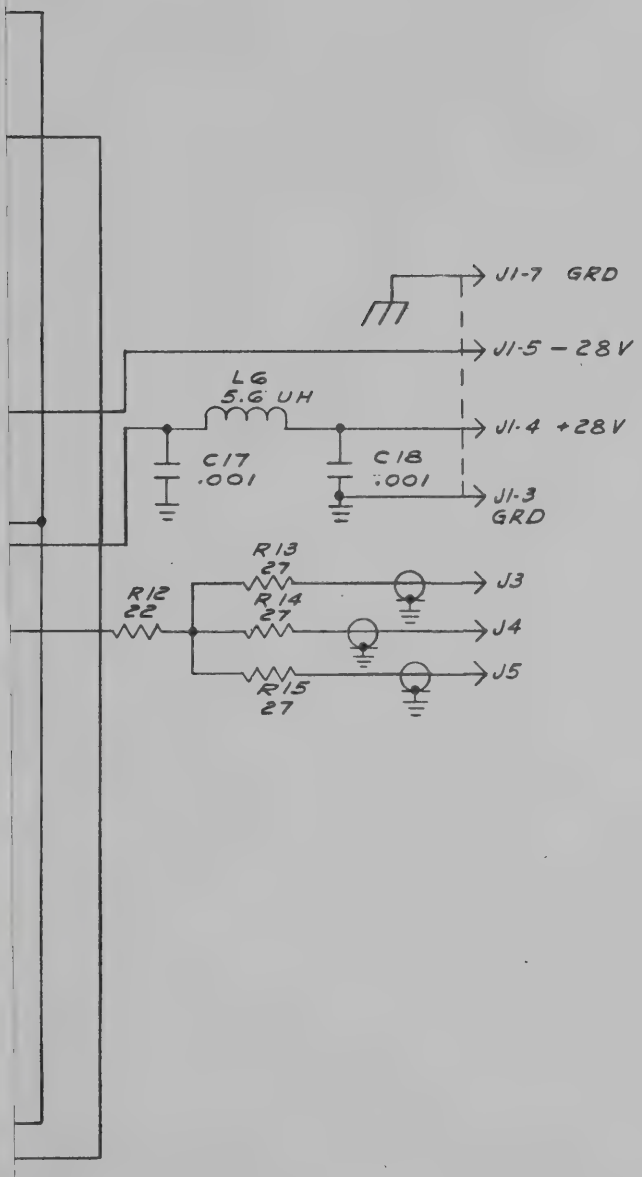


Figure FO 3-13. ⑩ Comm demod 1A3A3, wiring diagram (sheet 10 of 10).

NOTES:

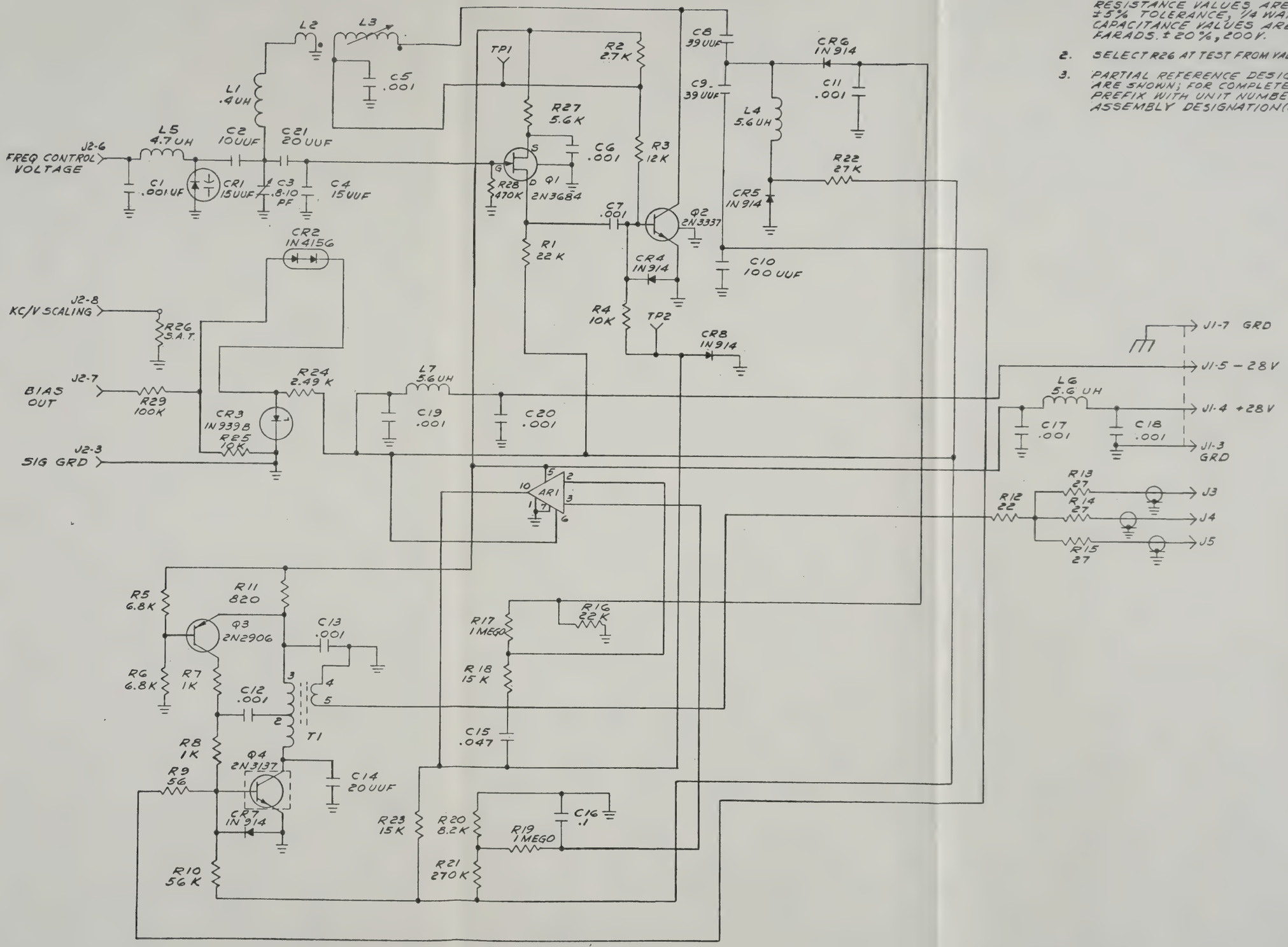
1. UNLESS OTHERWISE SPECIFIED ALL RESISTANCE VALUES ARE IN OHMS, ±5% TOLERANCE, 1/4 WATT. CAPACITANCE VALUES ARE IN MICRO-FARADS. ± 20%, 200V.
2. SELECT R26 AT TEST FROM VALUES 10K TO 235K
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUB-ASSEMBLY DESIGNATION(S).



EL2LF062

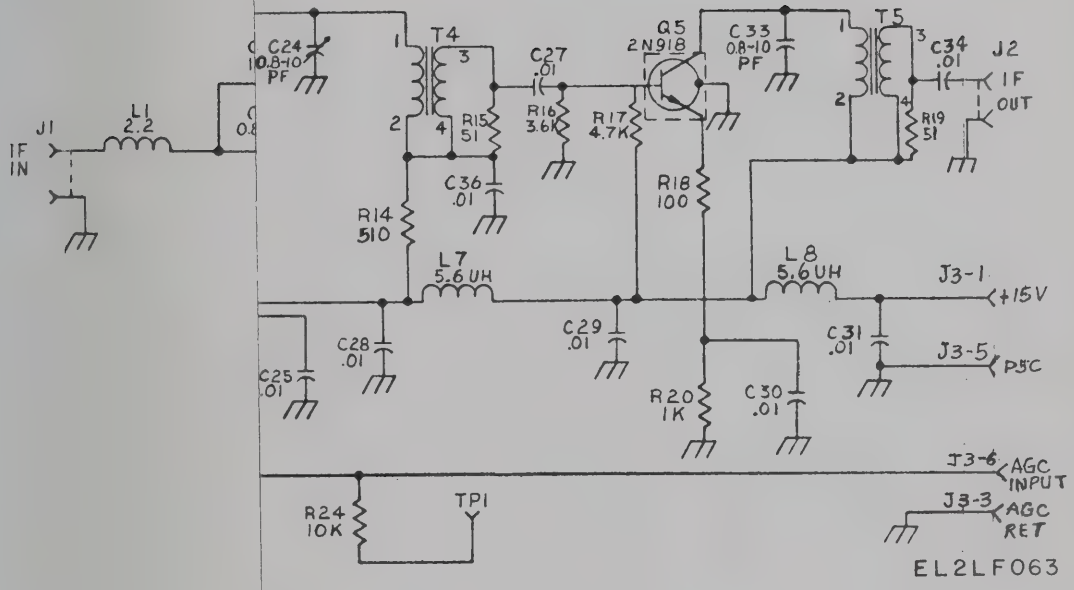
NOTES:

1. UNLESS OTHERWISE SPECIFIED ALL RESISTANCE VALUES ARE IN OHMS, ±5% TOLERANCE, 1/4 WATT. CAPACITANCE VALUES ARE IN MICROFARADS. ±20%, 200V.
2. SELECT R26 AT TEST FROM VALUES 10K TO 235K
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUB-ASSEMBLY DESIGNATION(S).



EL2LF062

Figure FO 3-14. Demod 48.6 MHz vco A3 schematic diagram.


J1
IF IN
L1 2.2
C24 10.8-10 PF
T4
C27 .01
Q5 2N918
C33 0.8-10 PF
T5
C34 .01
J2
IF OUT
R15 51
R16 3.6K
R17 4.7K
R19 51
C36 .01
R18 100
R14 510
L7 5.6 UH
L8 5.6 UH
J3-1
+15V
C28 .01
C29 .01
C31 .01
J3-5
P5C
C25 .01
R20 1K
C30 .01
J3-6
AGC INPUT
J3-3
AGC RET
R24 10K
TP1
EL2LF063

NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, ±5% TOLERANCE 1/4 WATT: CAPACITANCE VALUES ARE IN MICROFARADS, INDUCTANCE VALUES ARE IN MICROHENRIES.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATIONS PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S).
3. SELECT AT TEST VALUES FOR R4. 51 OHMS MIN, 360 OHMS MAX.

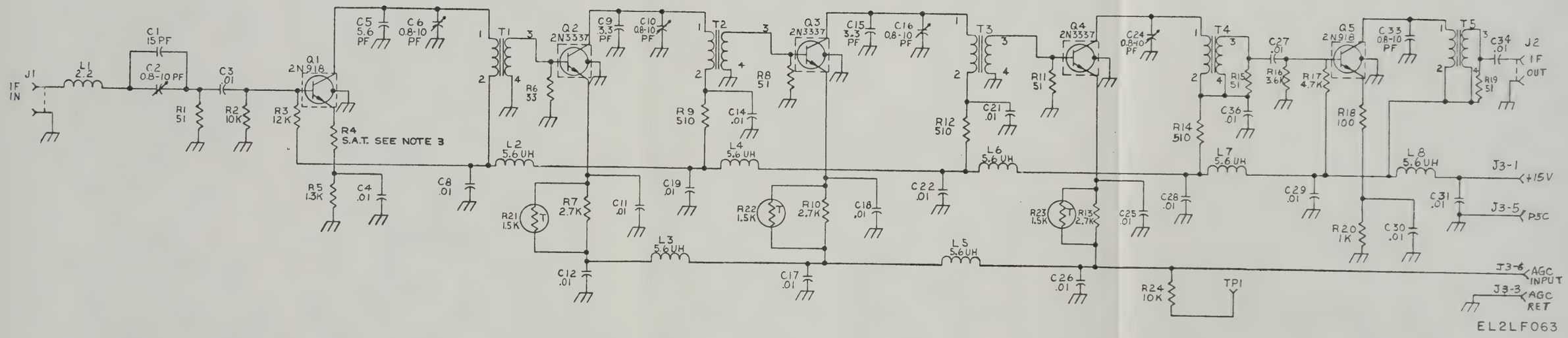
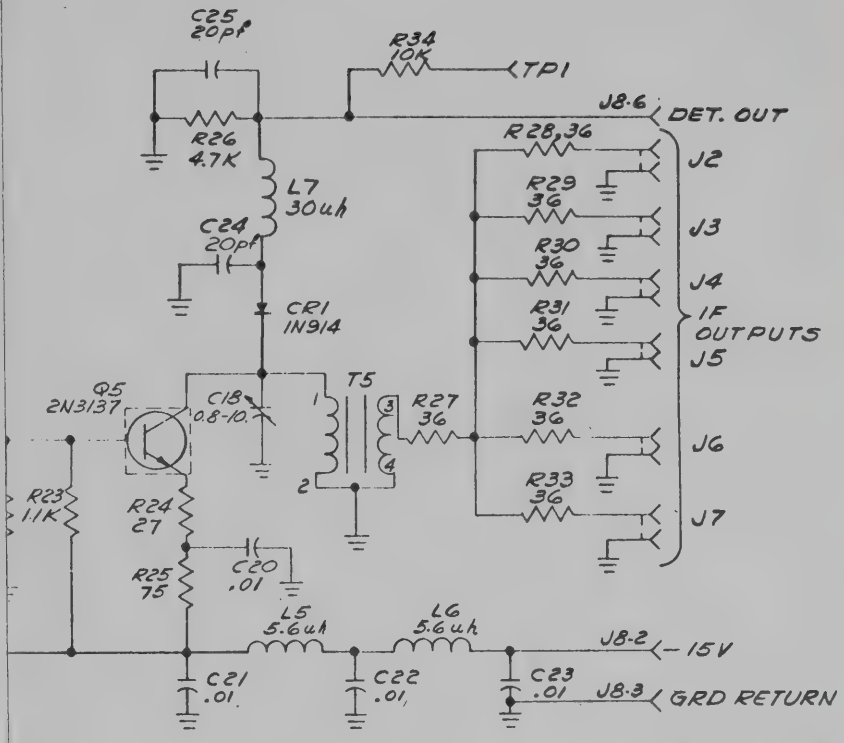


Figure FO3-15. 21.4 MHz if. preamplifier A4, schematic diagram.


C25
20pf
R34
10K
TP1
J8-6
DET. OUT
R26
4.7K
L7
30uh
C24
20pf
CR1
IN914
R28,36
J2
R29
36
J3
R30
36
J4
R31
36
J5
IF
OUTPUTS
Q5
2N3137
C18
0.8-10.
T5
R27
36
R32
36
J6
R33
36
J7
R23
11K
R24
27
R25
75
C20
.01
L5
5.6uh
L6
5.6uh
J8-2
-15V
C21
.01
C22
.01
C23
.01
J8-3
GRD RETURN
EL2LF069

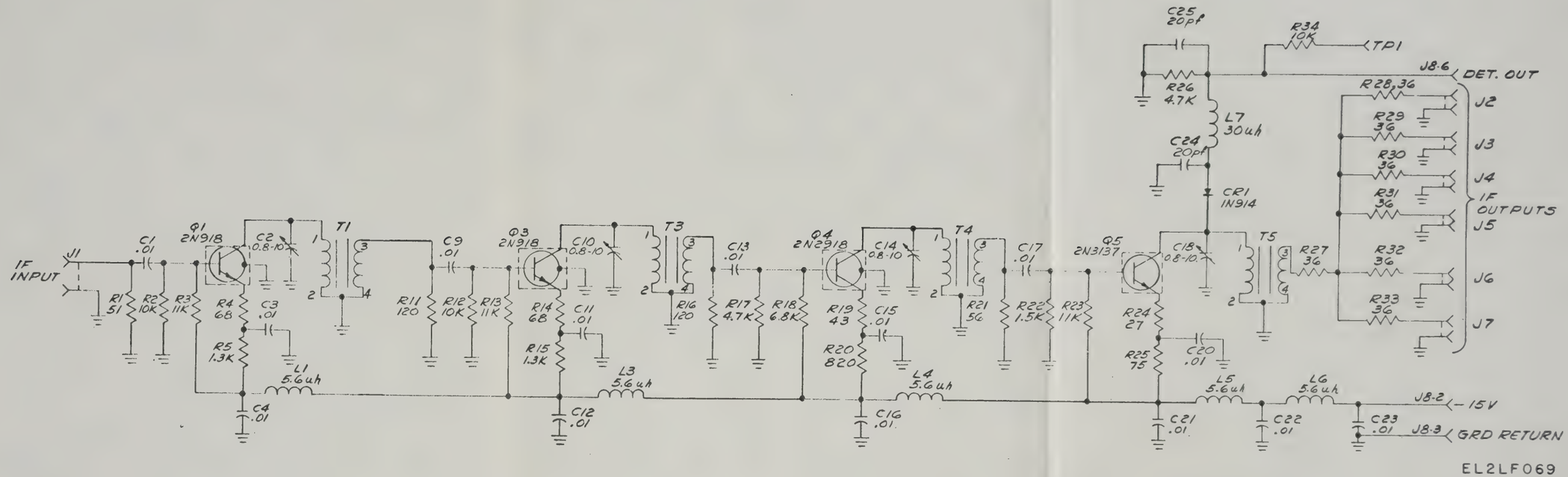
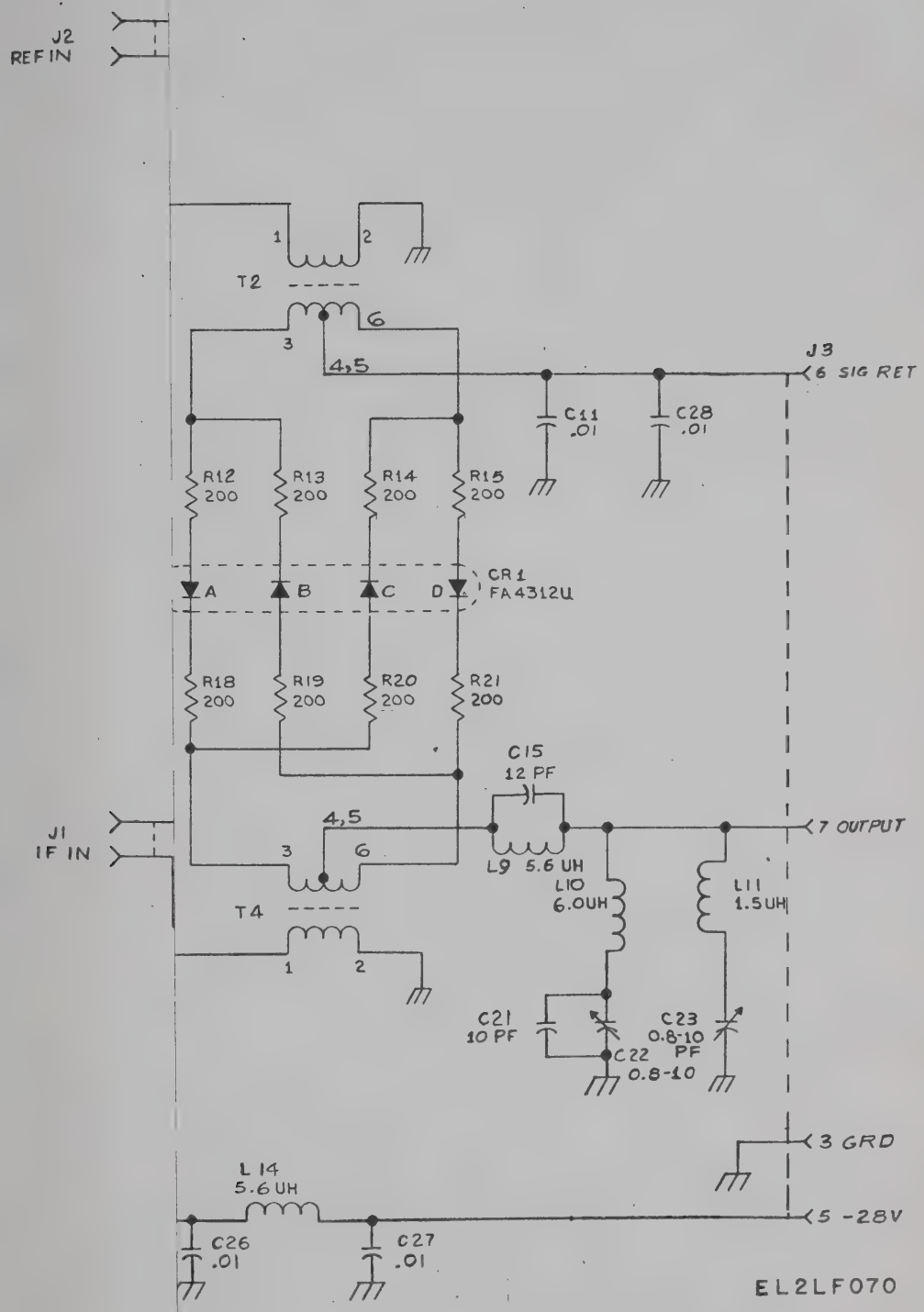
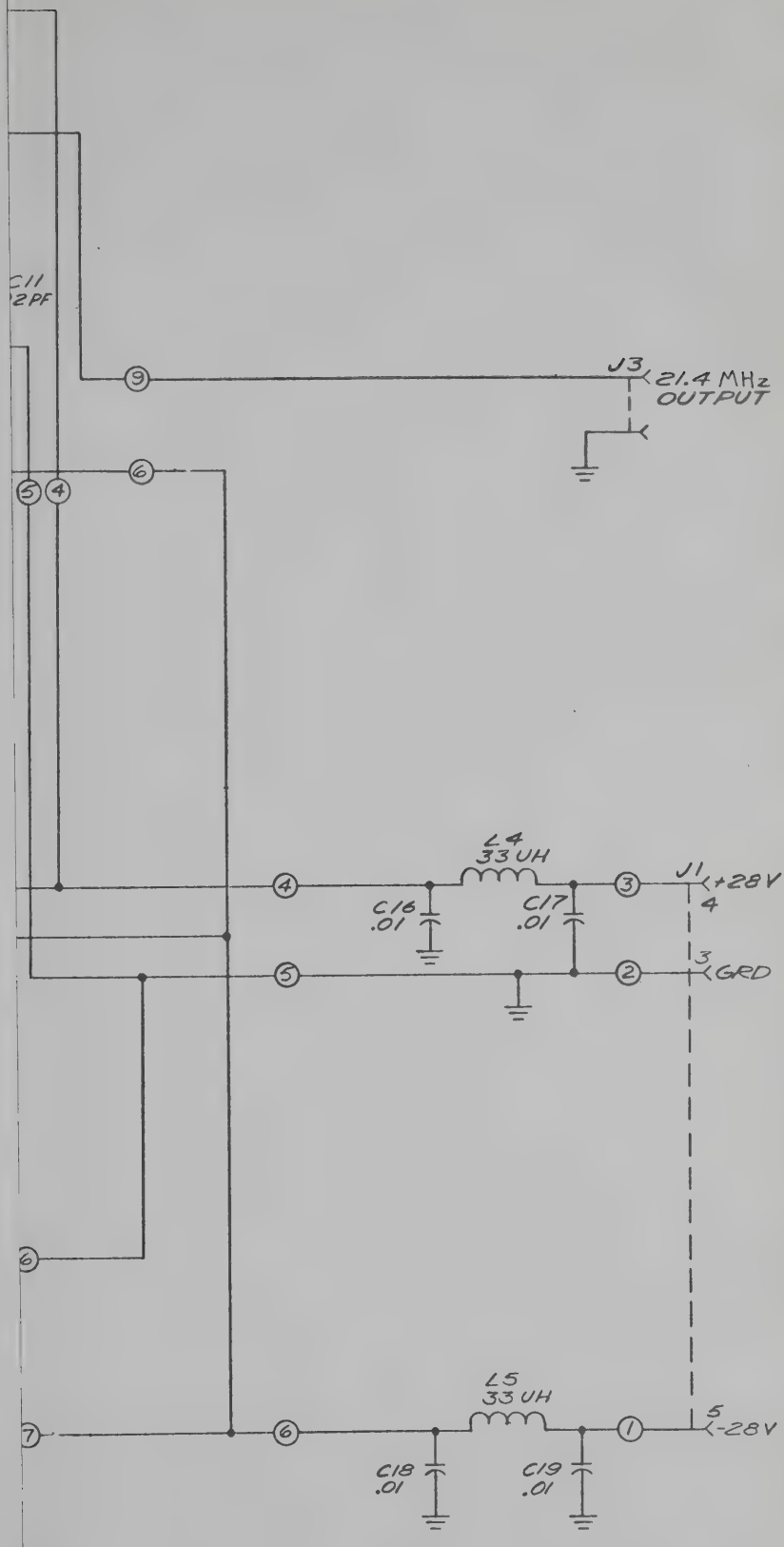


Figure FO 3-16. 21.4 MHz post amplifier A12, schematic diagram.


J2
REF IN
T2
1
2
3
6
4,5
J3
6 SIG RET
C11
.01
C28
.01
R12
200
R13
200
R14
200
R15
200
CR1
FA4312U
A
B
C
D
R18
200
R19
200
R20
200
R21
200
C15
12 PF
J1
IF IN
4,5
3
6
7 OUTPUT
L9 5.6 UH
L10
6.0UH
L11
1.5UH
T4
1
2
C21
10 PF
C22
0.8-10
C23
0.8-10
PF
3 GRD
L14
5.6 UH
5 -28V
C26
.01
C27
.01
EL2LF070

J2 REF IN
C3 .01
Q1 2N3137 HEAT SINK
R1 430
C1 1.0-28.0 PF
L1 1.5UH
C2 .01
L2 27UH
Q2 2N3866 HEAT SINK
C4 1.0-28.0 PF
R2 620
T1
R3 56
L3 5.6UH
R4 27
C6 .01
R5 2.7K
C5 .01
R6 1K
C7 .01
R7 100
R8 82
C8 .01
R9 2.2K
C9 .01
R10 3.9K
R11 470
C10 .01
L4 5.6UH
L5 5.6 UH
T2
J3 6 SIG RET
C11 .01
C28 .01
R12 200
R13 200
R14 200
R15 200
CR1 FA4312U
A B C D
R18 200
R19 200
R20 200
R21 200
C15 12 PF
L9 5.6 UH
L10 6.0UH
L11 1.5UH
7 OUTPUT
T4
C21 10 PF
C22 0.8-10
C23 0.8-10 PF
3 GRD
5 -28V
L14 5.6 UH
C26 .01
C27 .01
J1 IF IN
C16 .01
Q3 2N3137 HEAT SINK
R16 430
C12 1.0-28.0 PF
L6 1.5UH
C13 .01
L7 27UH
Q4 2N3866 HEAT SINK
C14 1.0-28.0 PF
R17 620
T3
R22 56
L8 5.6UH
R23 (SAT)
C18 .01
R24 2.7K
C17 .01
R26 1K
C19 .01
R27 100
R28 82
C20 .01
R29 2.2K
C24 .01
R30 3.9K
R31 470
C25 .01
L12 5.6 UH
L13 5.6 UH
EL2LF070

Figure FO 3-17. 214 MHz am. phase detector A13, schematic diagram.


C11
2PF
J3
21.4 MHz
OUTPUT
L4
33 UH
C16
.01
C17
.01
J1
+28V
4
3
GRD
L5
33 UH
C18
.01
C19
.01
5
-28V

EL2LF071

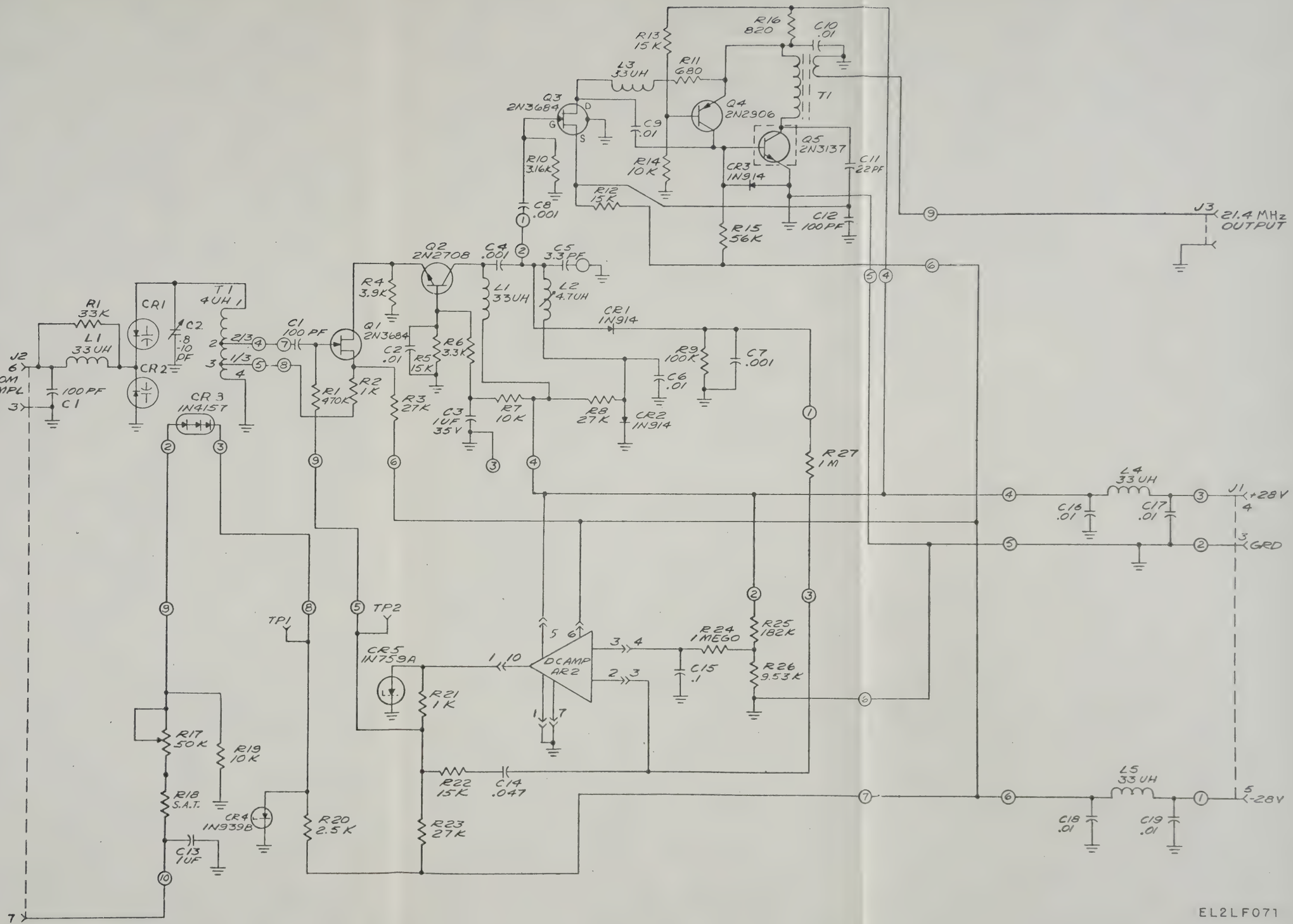
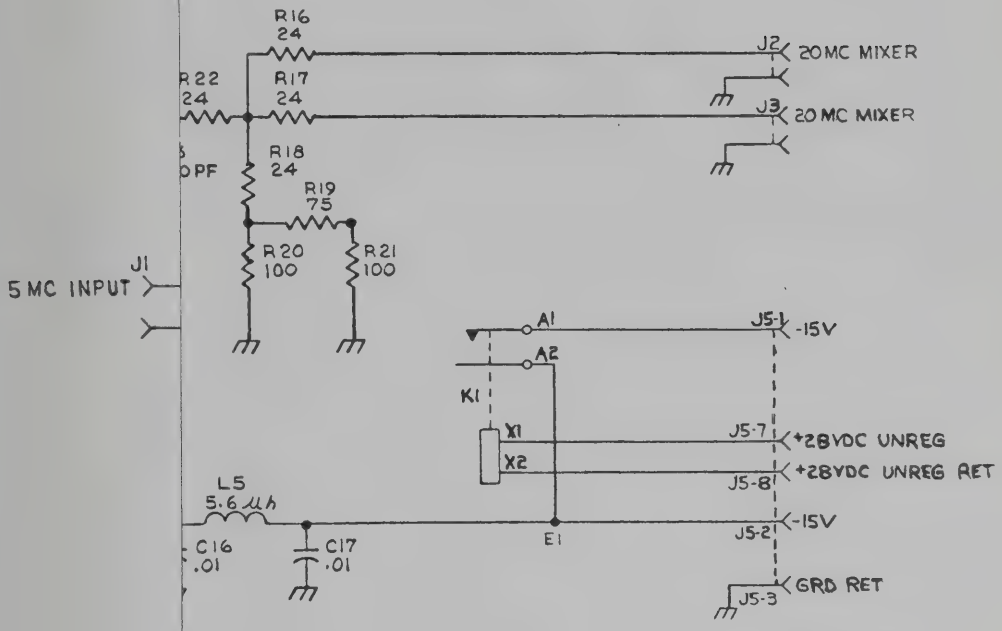


Figure FO 3-18. Demodulator 21.4 MHz vco, schematic diagram.


R16
24
J2
20MC MIXER
R22
24
R17
24
J3
20 MC MIXER
R18
24
R19
75
R20
100
R21
100
J1
5 MC INPUT
A1
J5-1
-15V
A2
K1
X1
J5-7
+28VDC UNREG
X2
+28VDC UNREG RET
J5-8
L5
5.6 μh
J5-2
-15V
C16
.01
C17
.01
E1
J5-3
GRD RET

EL2LF079

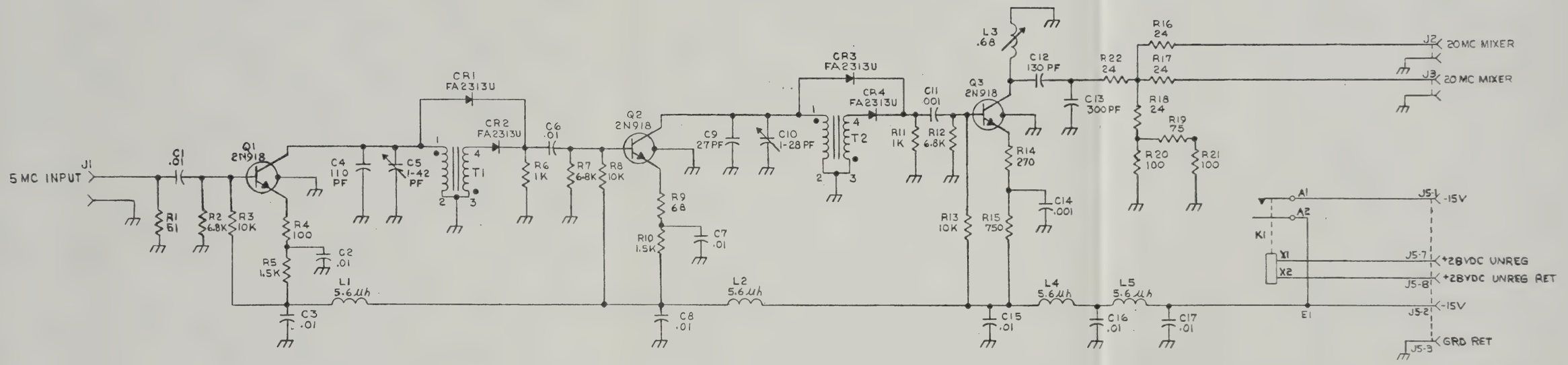
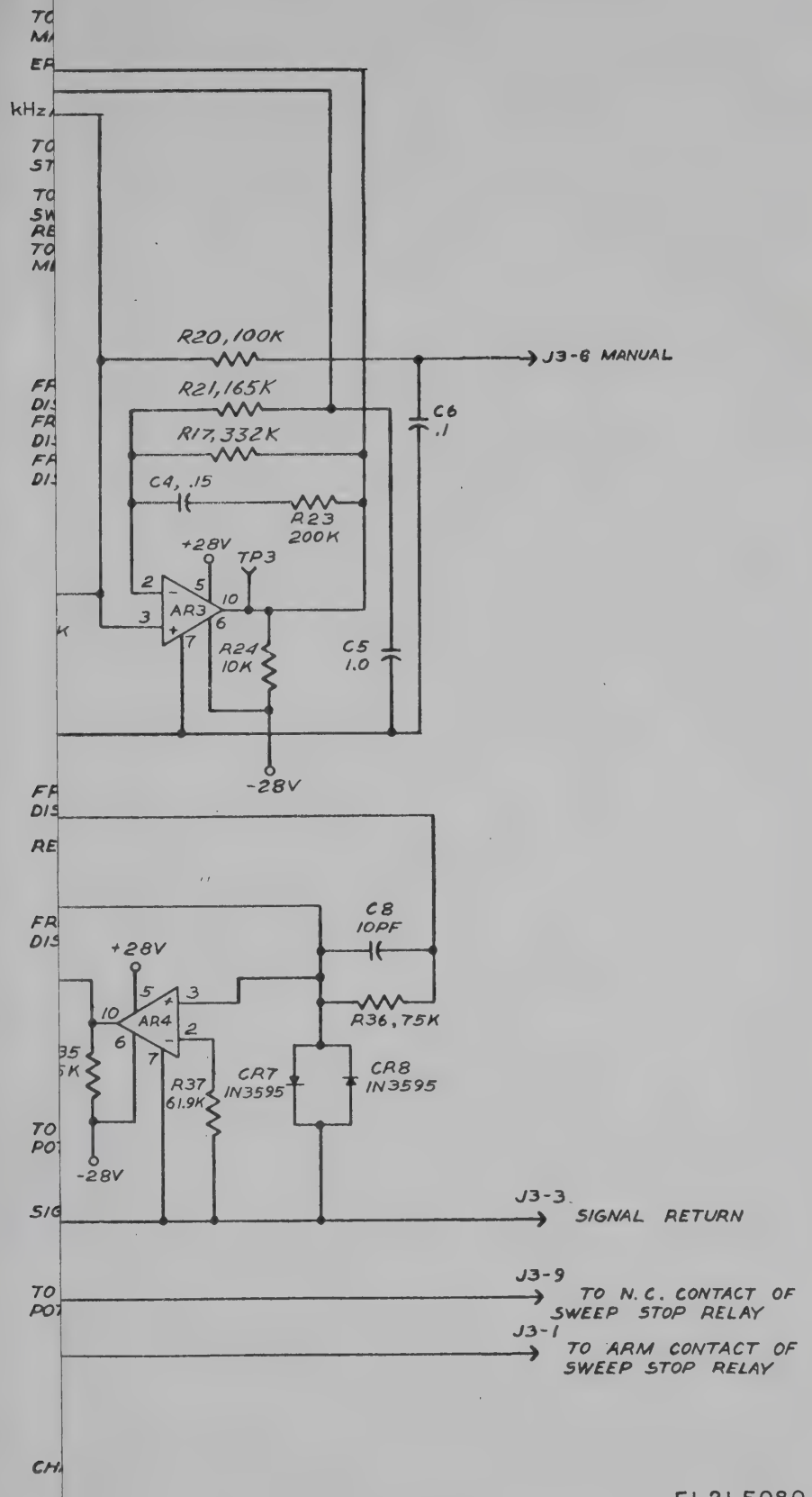


Figure FO 3-19. X4 frequency multiplier, schematic diagram.


R20, 100K
J3-8 MANUAL
R21, 165K
R17, 332K
C6
.1
C4, .15
R23
200K
+28V
TP3
AR3
R24
10K
C5
1.0
-28V
C8
10PF
+28V
AR4
R36, 75K
R37
61.9K
CR7
IN3595
CR8
IN3595
-28V
J3-3
SIGNAL RETURN
J3-9
TO N.C. CONTACT OF
SWEEP STOP RELAY
J3-1
TO ARM CONTACT OF
SWEEP STOP RELAY

EL2LF080

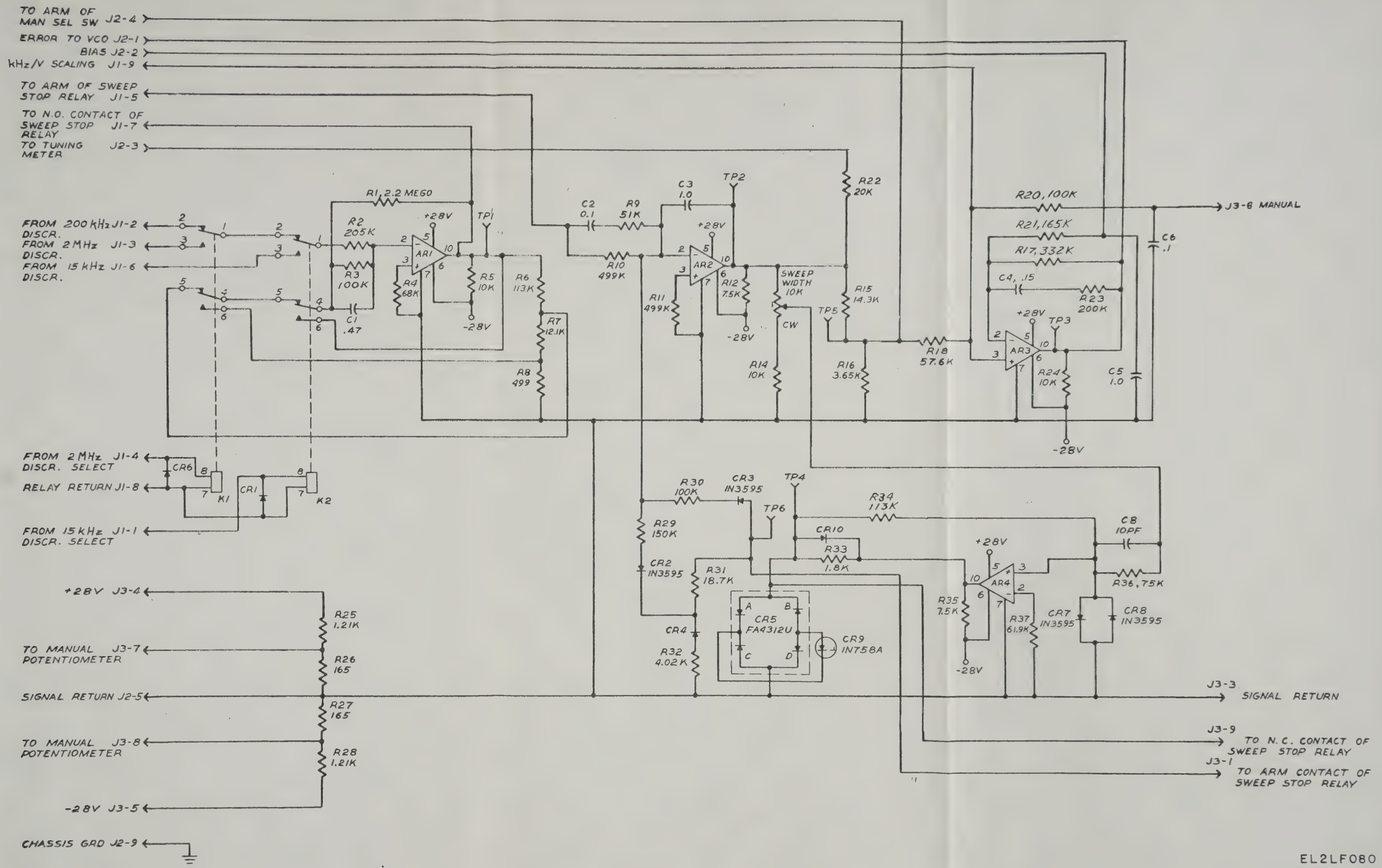
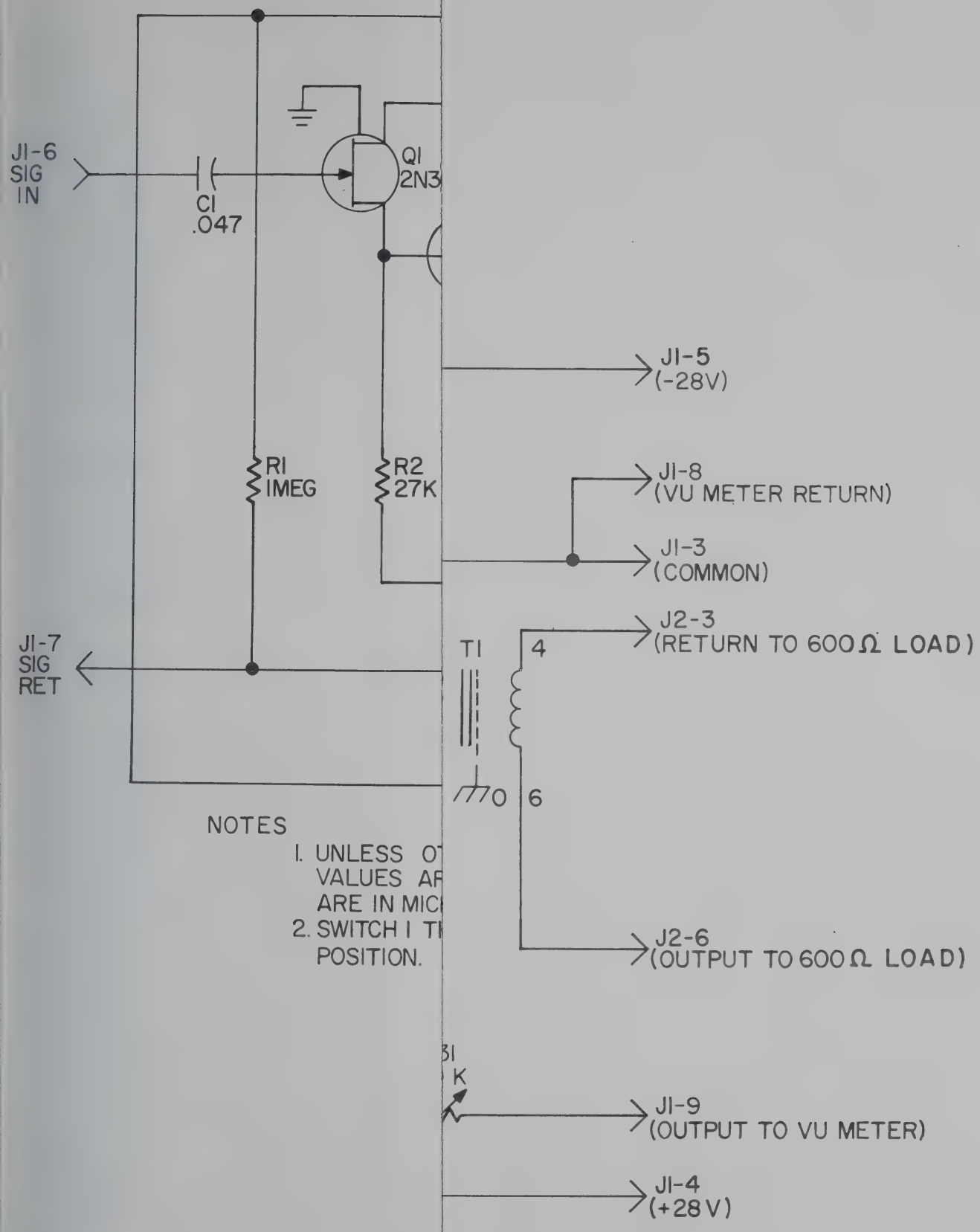


Figure FO 3-20. Afc and sweep circuit, schematic diagram.



NOTES

1. UNLESS O
VALUES AR
ARE IN MIC
2. SWITCH 1 T
POSITION.

EL2LF086

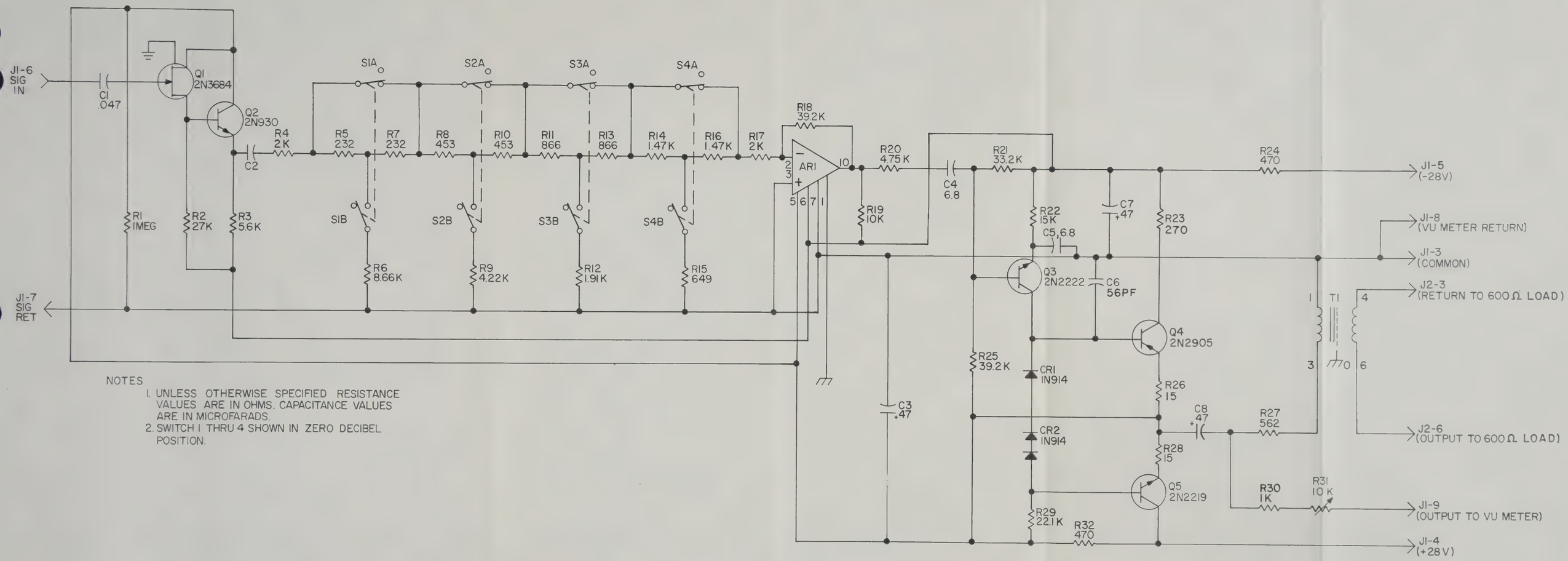
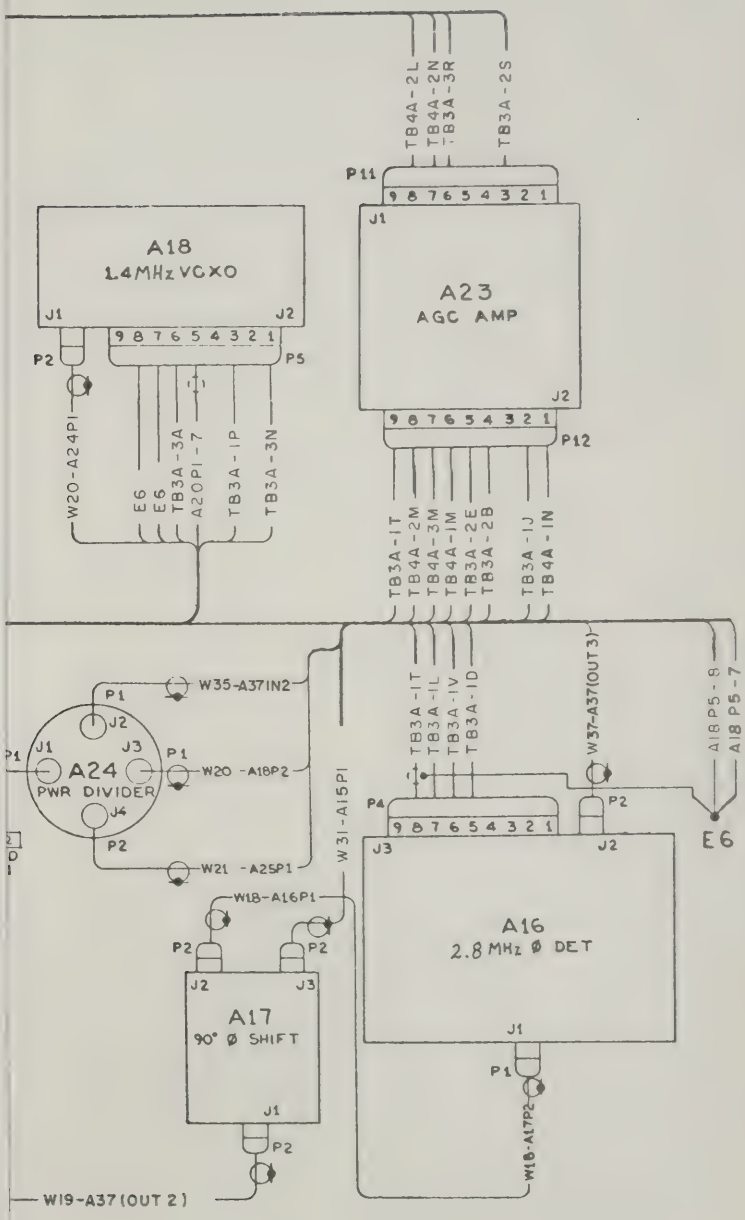


Figure FO 3-21. 0-30 dB attenuator and audio amplifier, schematic diagram.

EL2LF086



EL2LF090

of 9).

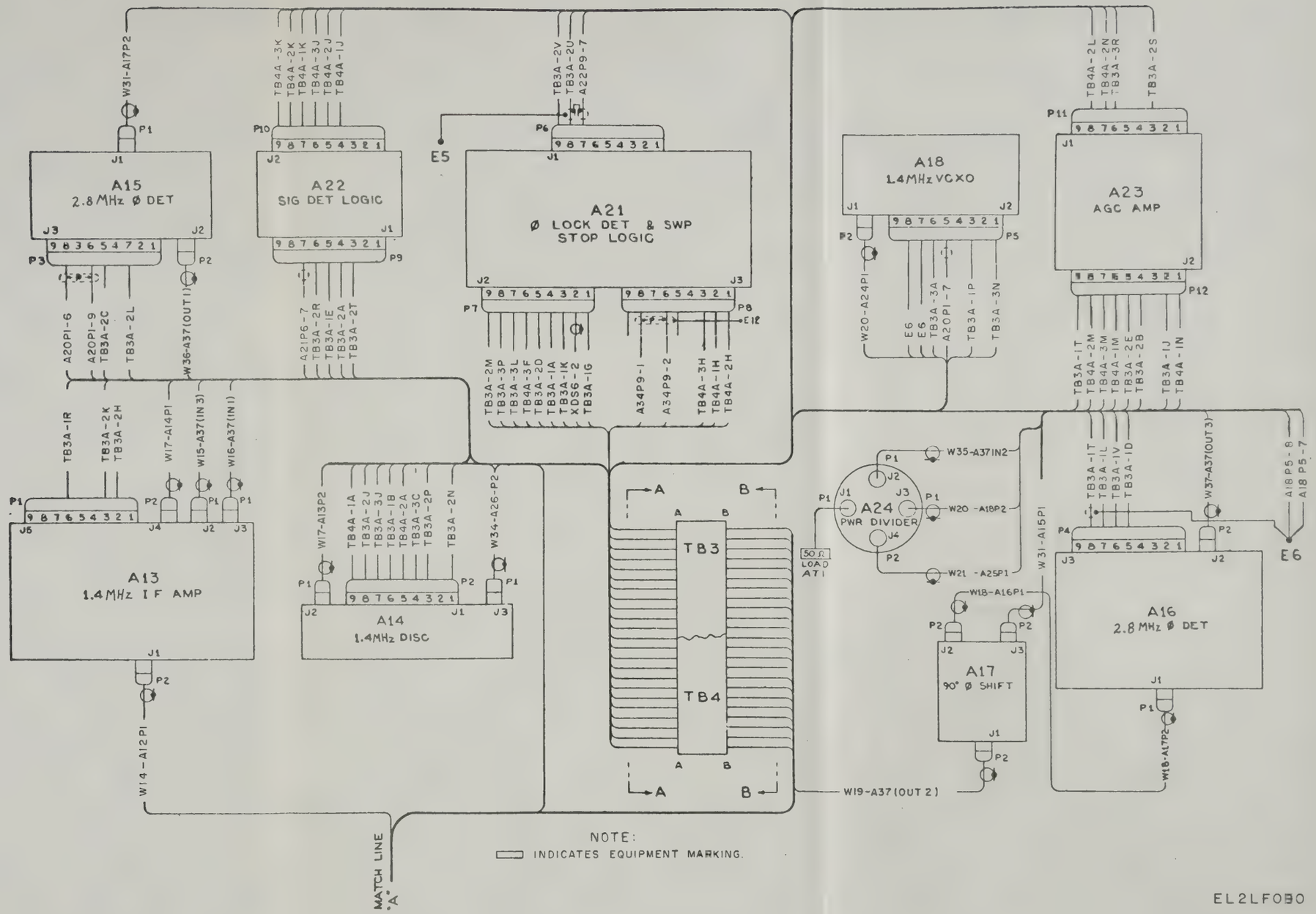
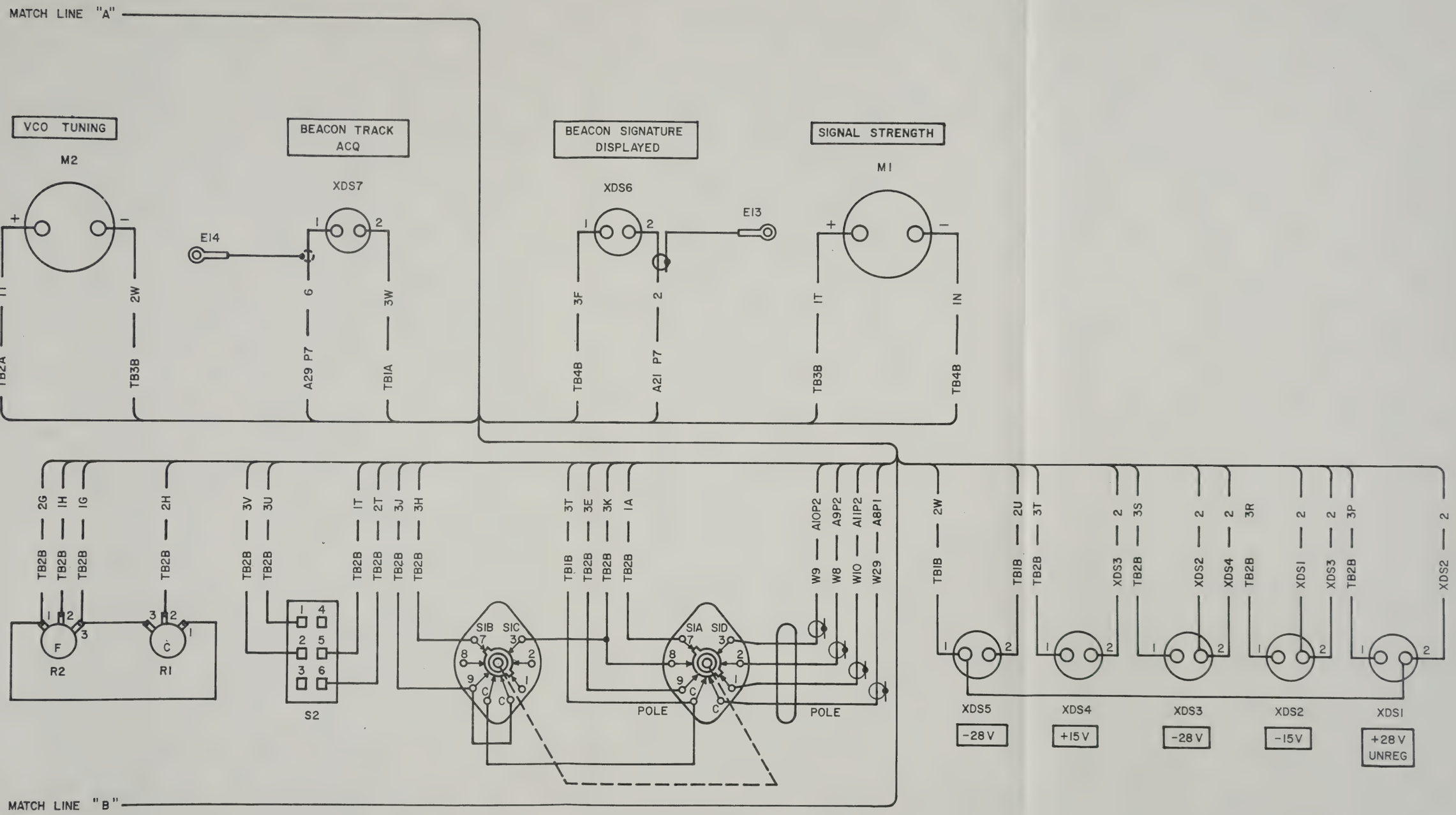


Figure FO 3-22. ① Beacon demod, wiring diagram (sheet 1 of 9).

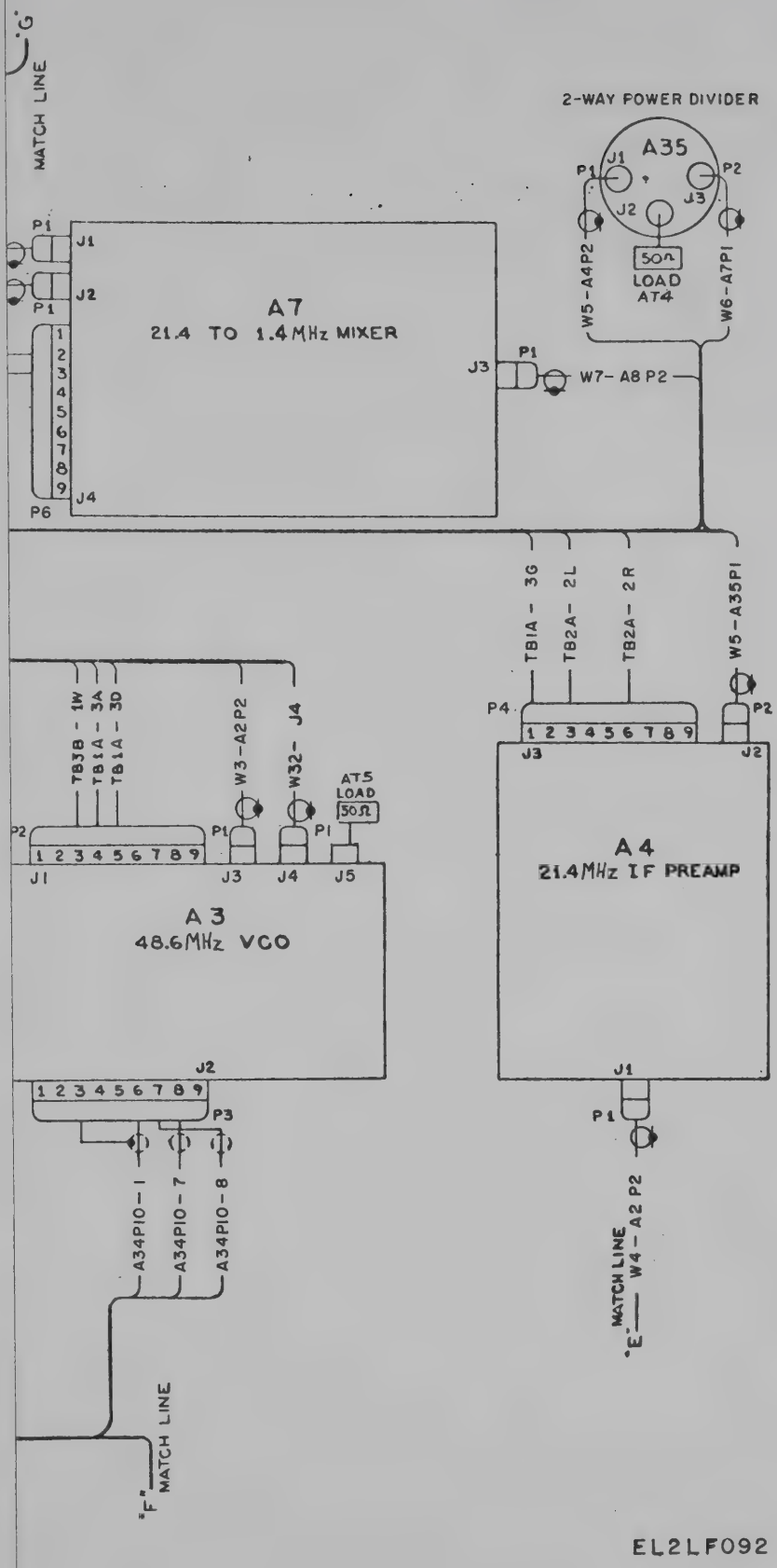
MATCH LINE
VCO TUNIN
M2
+
1T
TB2A
2G
1H
1G
TB2B
TB2B
TB2B
1
2
3
F
R2
3T
TB2B
XDS3
2
3S
TB2B
XDS2
2
XDS4
2
3R
TB2B
XDS1
2
XDS3
2
3P
TB2B
XDS2
2
1
2
XDS4
XDS3
XDS2
XDS1
+15V
-28V
-15V
+28V
UNREG
MATCH LINE "

EL2LF091



EL2LF091

Figure FO 3-22. ②Beacon demod. wiring diagram (sheet 2 of 9).


MATCH LINE "G"
2-WAY POWER DIVIDER
A35
J1
P1
P2
J2
J3
50Ω LOAD AT4
W5-A4P2
W6-A7P1
A7
21.4 TO 1.4 MHz MIXER
P1
J1
J2
P1
1 2 3 4 5 6 7 8 9
J4
P6
J3
P1
W7-A8P2
TB1A-3G
TB2A-2L
TB2A-2R
W5-A35P1
P4
1 2 3 4 5 6 7 8 9
J3
J2
P2
TB3B-1W
TB1A-3A
TB1A-3D
W3-A2P2
W32-J4
AT5 LOAD 50Ω
P2
1 2 3 4 5 6 7 8 9
P1
P1
J1
J3
J4
J5
A3
48.6MHz VCO
A4
21.4MHz IF PREAMP
J2
1 2 3 4 5 6 7 8 9
P3
J1
P1
A34P10-1
A34P10-7
A34P10-8
MATCH LINE "E"
W4-A2P2
MATCH LINE "F"
EL2LF092

3 of 9).

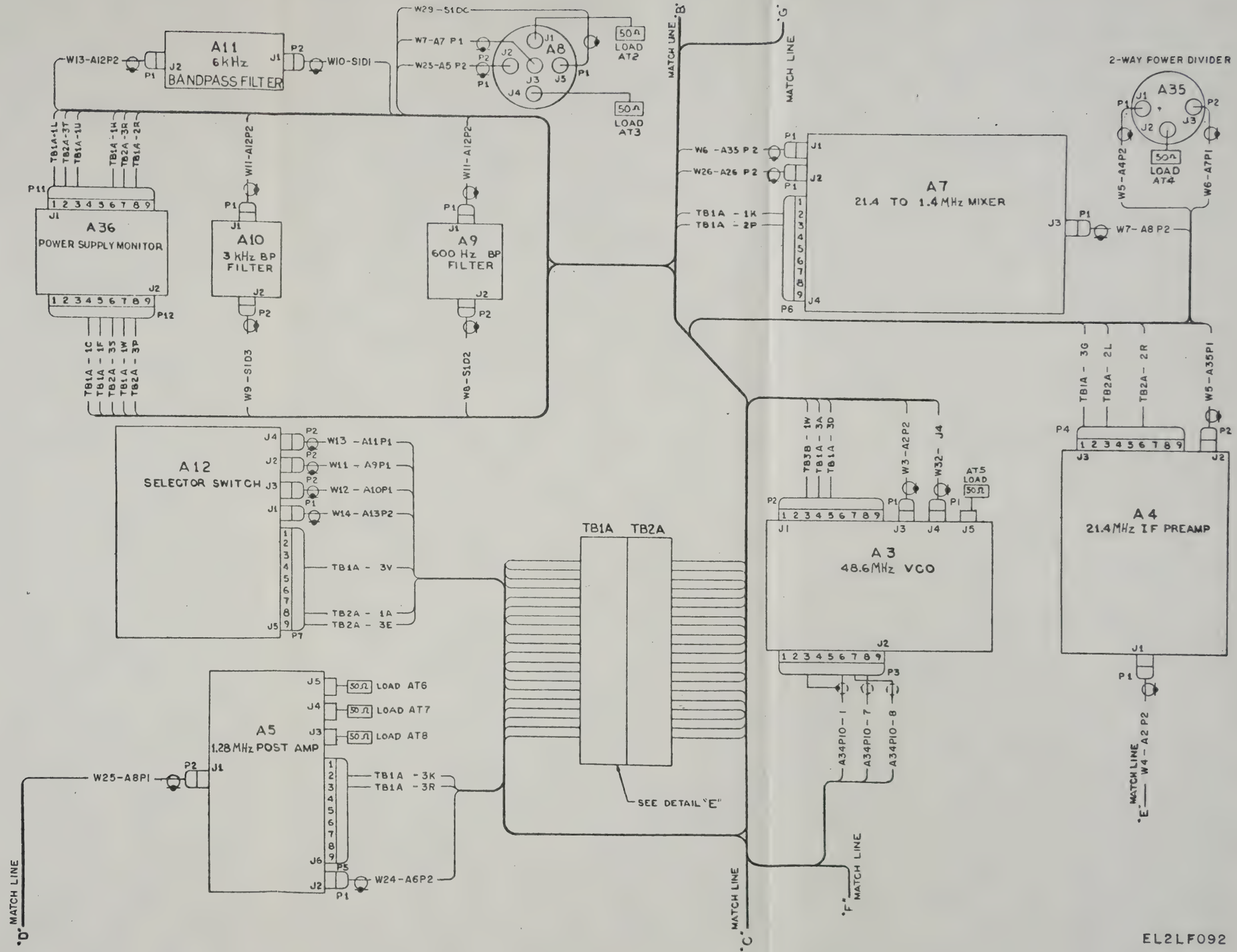


Figure FO 3-22.③ Beacon demod, wiring diagram (sheet 3 of 9).

"D" MATCH LINE
MATCH LINE "E"
W4-A4 P1
P2
J3
A2
70 MHz - 21.4 MHz MIXER
J2
J1
3 4 5 6 7 8 9
P2
P2
TB1A - 3M
W3-A3 P1
W2-A1 P1
W30-A30 P1
J1
J2
J5 - J
J5 - N
J5 - U
J5 - V
J6 - C
J5 - X
J5 - AA
J6 - E
J5 - HH
J5 - DD
J5 - GG
E1
E2
E3
E4

EL2LF093

Figure FO 3-22.④Beacon demod, wiring diagram (sheet 4 of 9).

iagram (sheet 5 of 9).

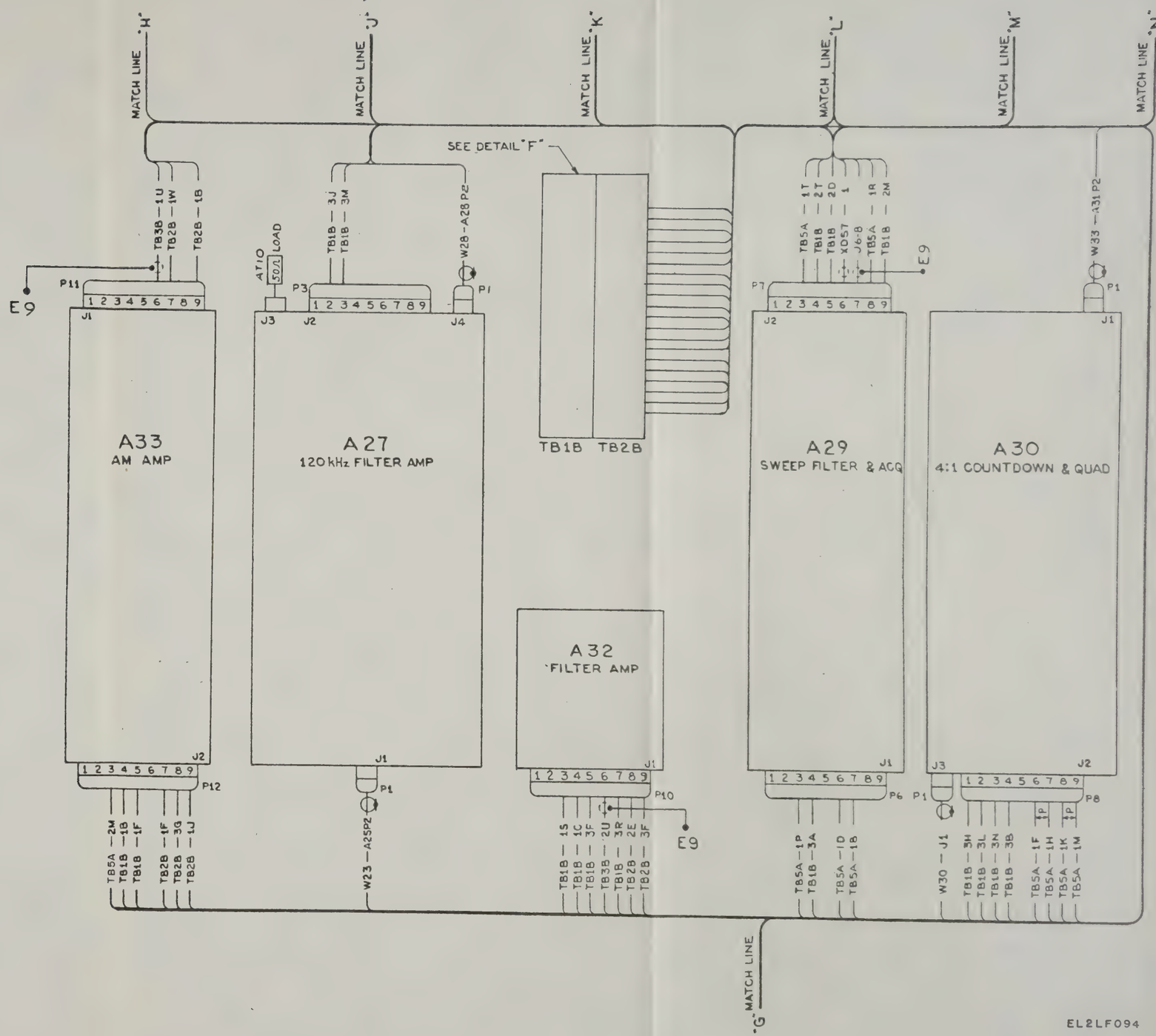


Figure FO 3-22. Ⓢ *Beacon demod, wiring diagram (sheet 5 of 9).*

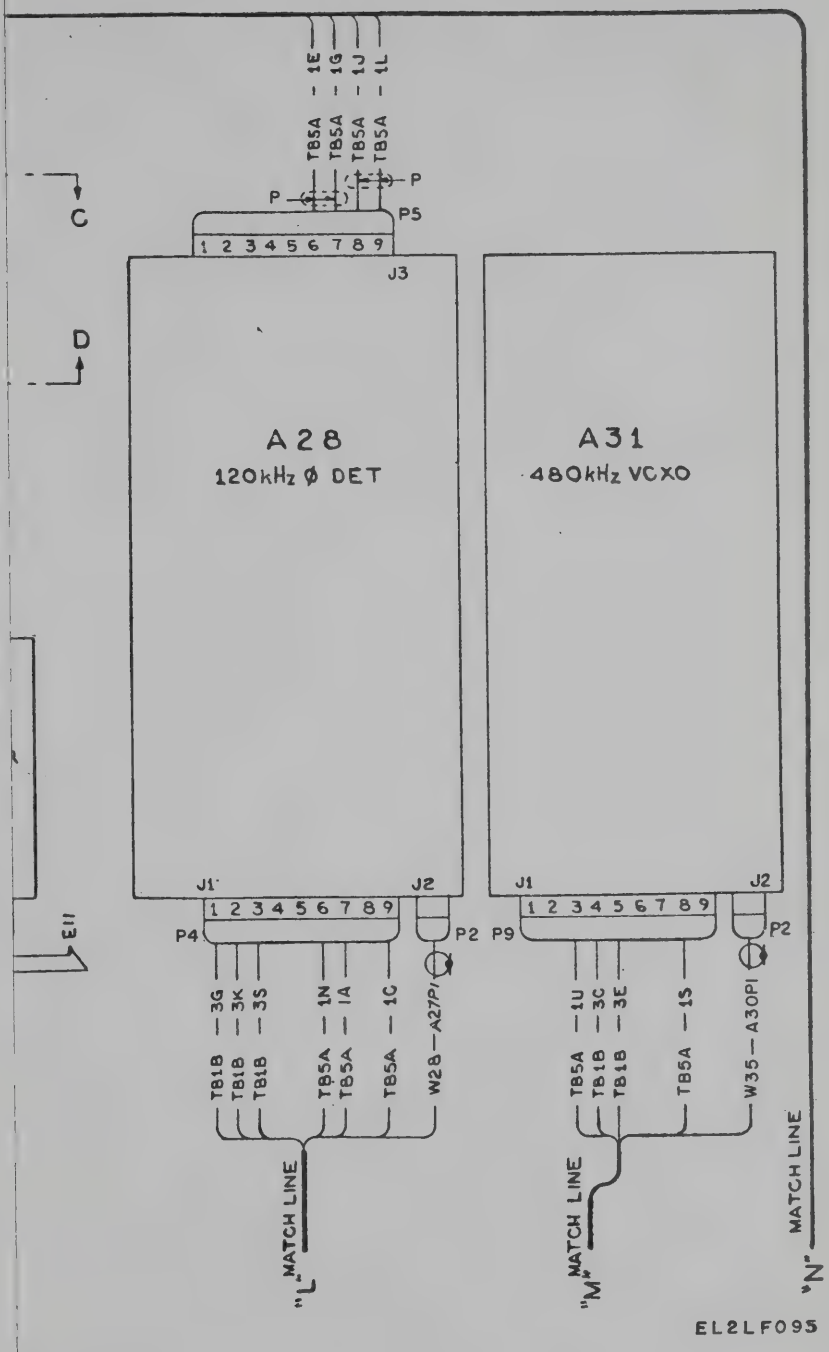
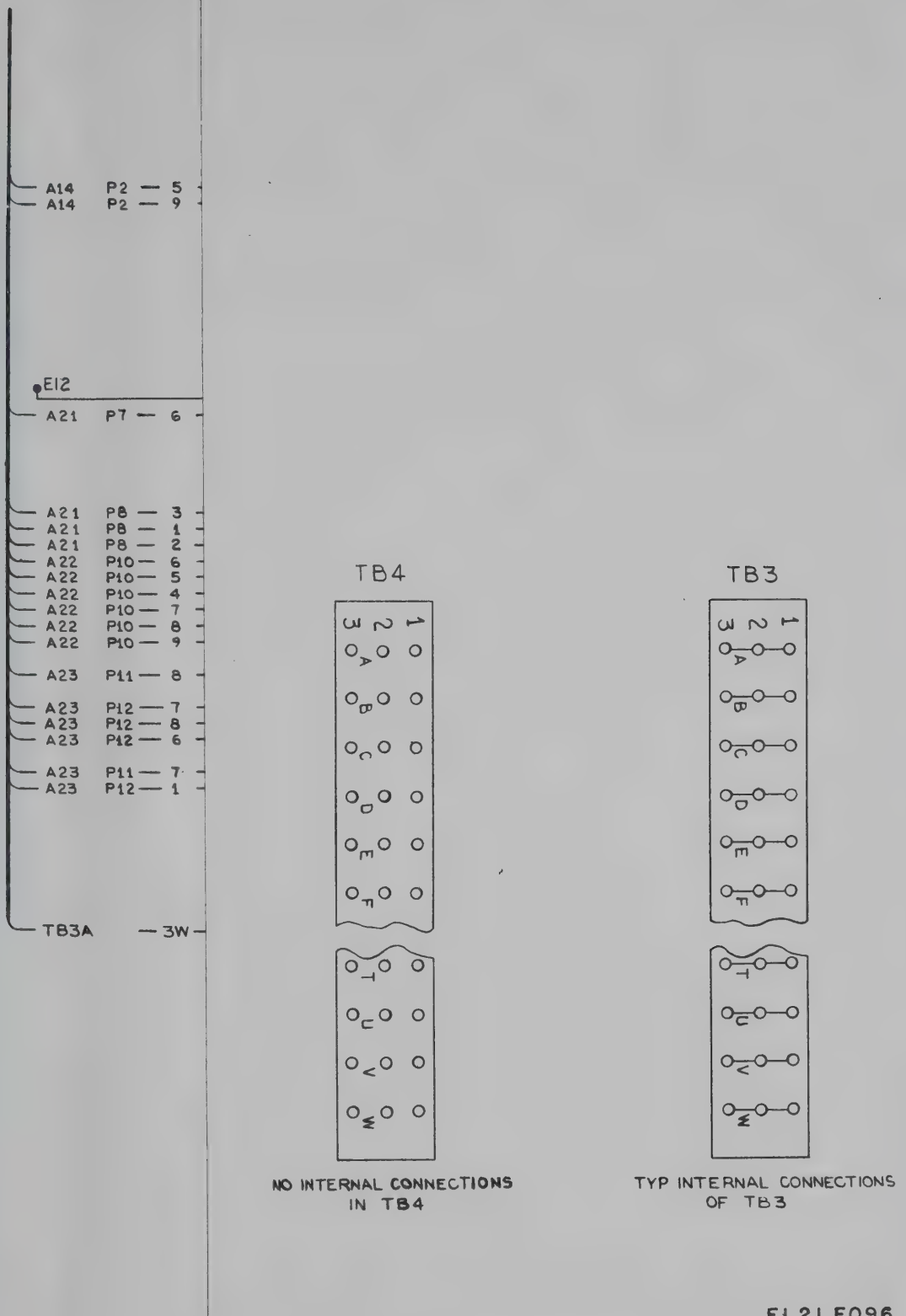
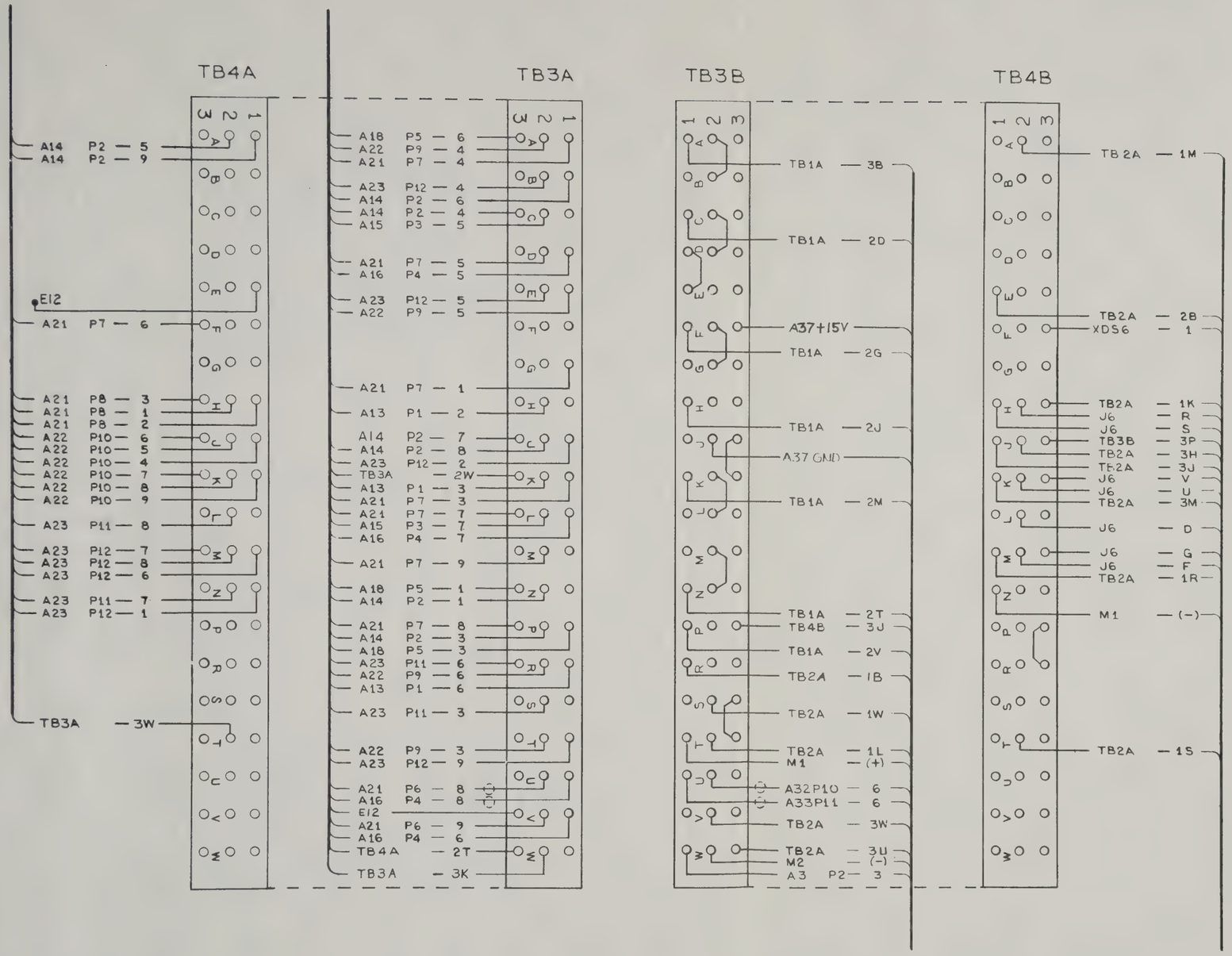


diagram (sheet 6 of 9).

Figure FO 3-22.⑥ Beacon demod, wiring diagram (sheet 6 of 9).

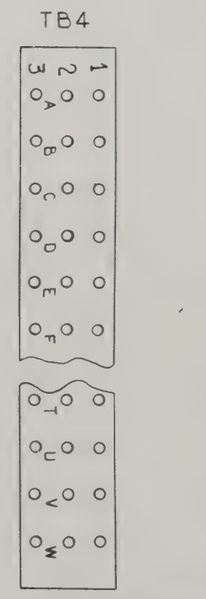

A14 P2 — 5
A14 P2 — 9
E12
A21 P7 — 6
A21 P8 — 3
A21 P8 — 1
A21 P8 — 2
A22 P10 — 6
A22 P10 — 5
A22 P10 — 4
A22 P10 — 7
A22 P10 — 8
A22 P10 — 9
A23 P11 — 8
A23 P12 — 7
A23 P12 — 8
A23 P12 — 6
A23 P11 — 7
A23 P12 — 1
TB3A — 3W
TB4
1 2 3
A B C D E F
T U V W
NO INTERNAL CONNECTIONS IN TB4
TB3
1 2 3
A B C D E F
T U V W
TYP INTERNAL CONNECTIONS OF TB3

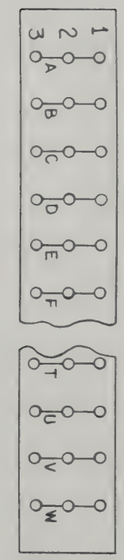
EL2LF096



VIEW A-A

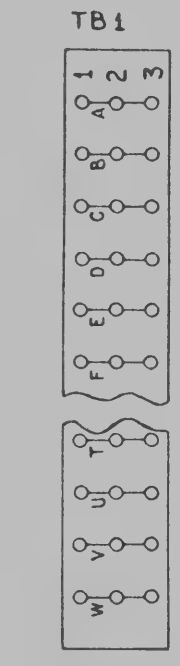
VIEW B-B



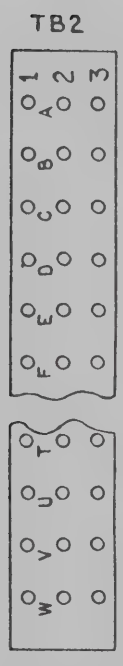


EL2LF096

Figure FO 3-22.①Beacon demod, wiring diagram (sheet 7 of 9).

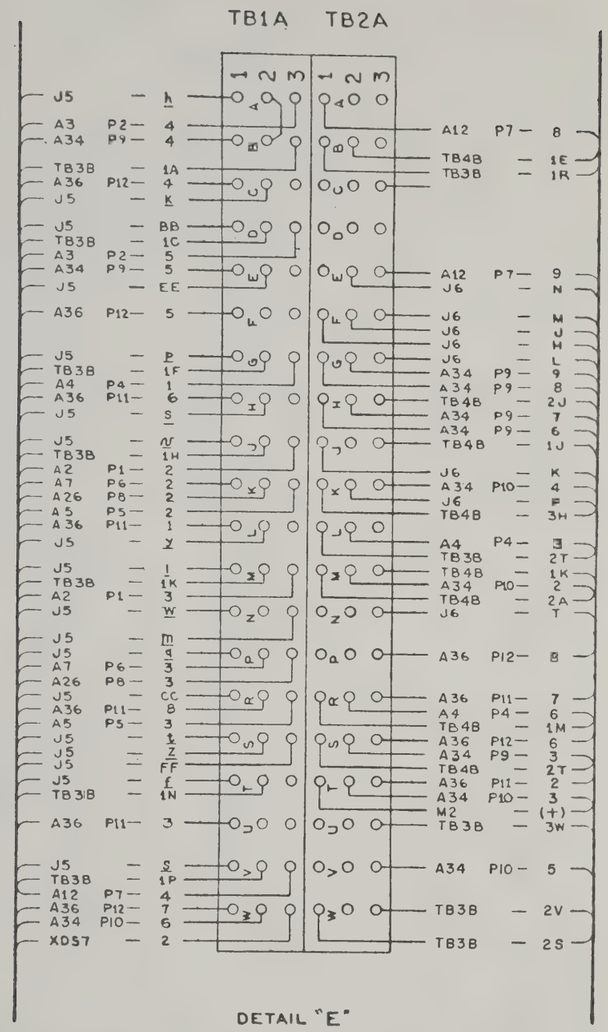


TYP INTERNAL CONNECTIONS
OF TB1

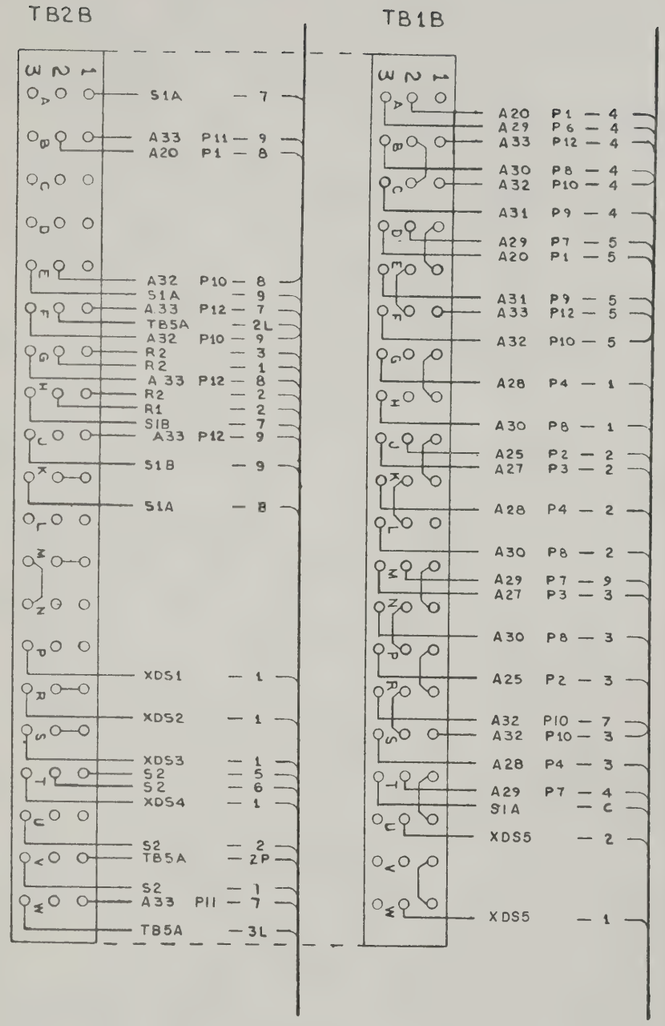


NO INTERNAL CONNECTIONS
IN TB2

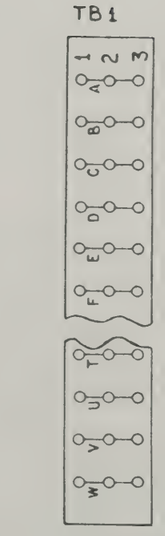
EL2LF097



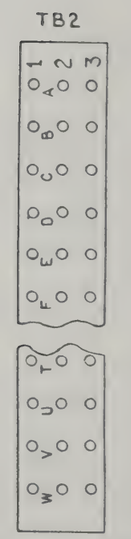
DETAIL "E"



DETAIL "F"



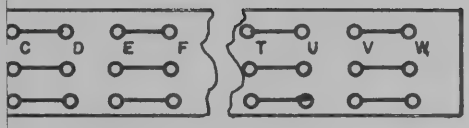
TYP INTERNAL CONNECTIONS OF TB1



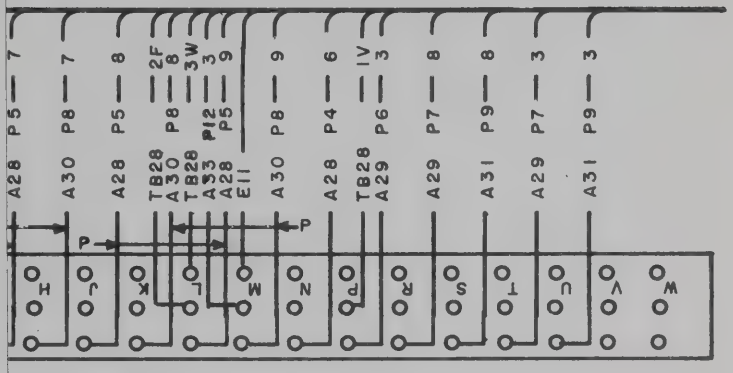
NO INTERNAL CONNECTIONS IN TB2

EL2LF097

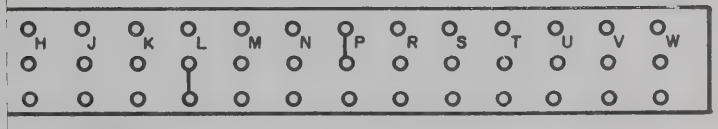
Figure FO 3-22.⑧ Beacon demod, wiring diagram (sheet 8 of 9).



ERNAL CONNECTIONS OF TB5



VIEW C-C



VIEW D-D

EL2LF098

) *Beacon demod, wiring diagram (sheet 9 of 9).*

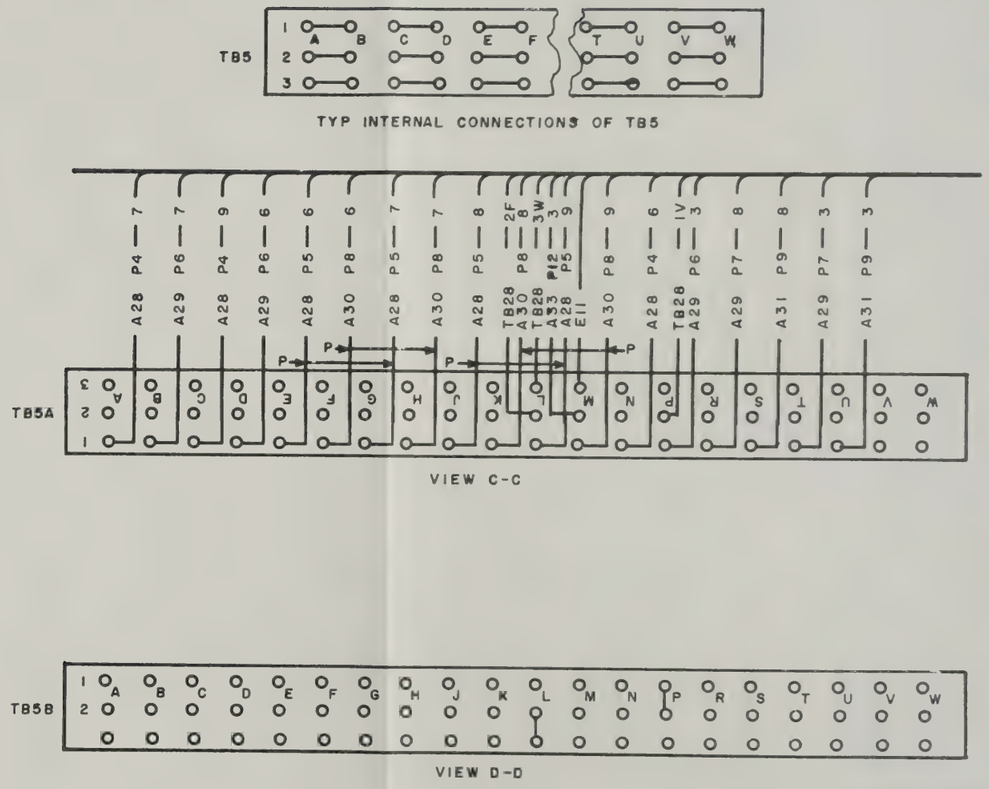
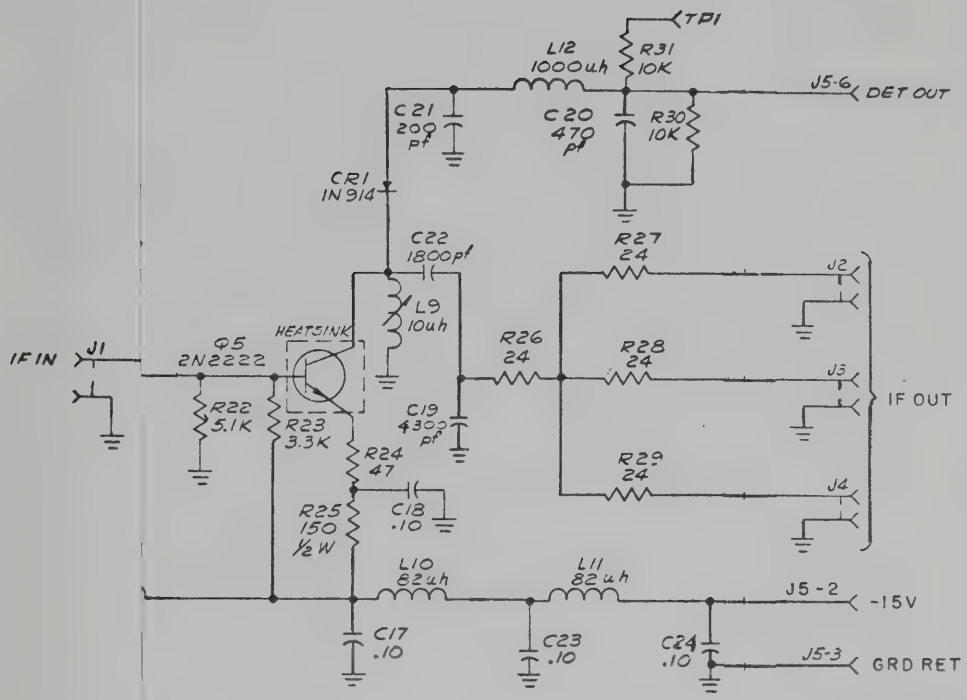


Figure FO 3-22.(6) Beacon demod, wiring diagram (sheet 9 of 9).


TP1
L12
1000uh
R31
10K
J5-6
DET OUT
C21
200
pf
C20
470
pf
R30
10K
CR1
IN914
C22
1800pf
R27
24
J2
L9
10uh
HEATSINK
IF IN
J1
Q5
2N2222
R26
24
R28
24
J3
IF OUT
R22
5.1K
R23
3.3K
C19
4300
pf
R24
47
R29
24
J4
R25
150
½W
C18
.10
L10
82uh
L11
82uh
J5-2
-15V
C17
.10
C23
.10
C24
.10
J5-3
GRD RET
EL2LF100

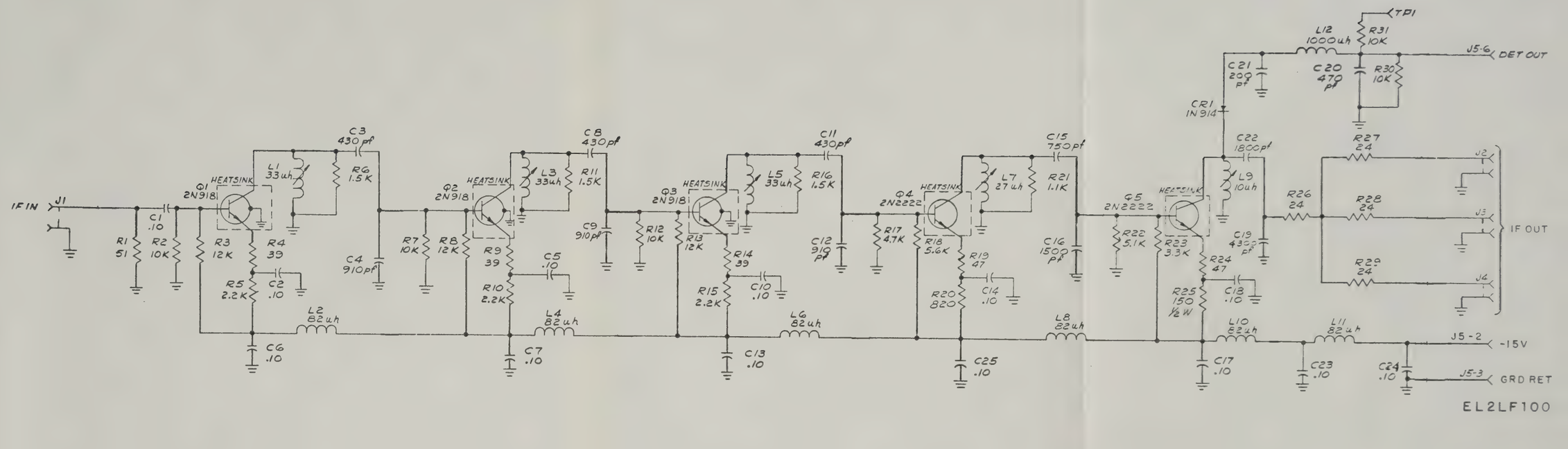


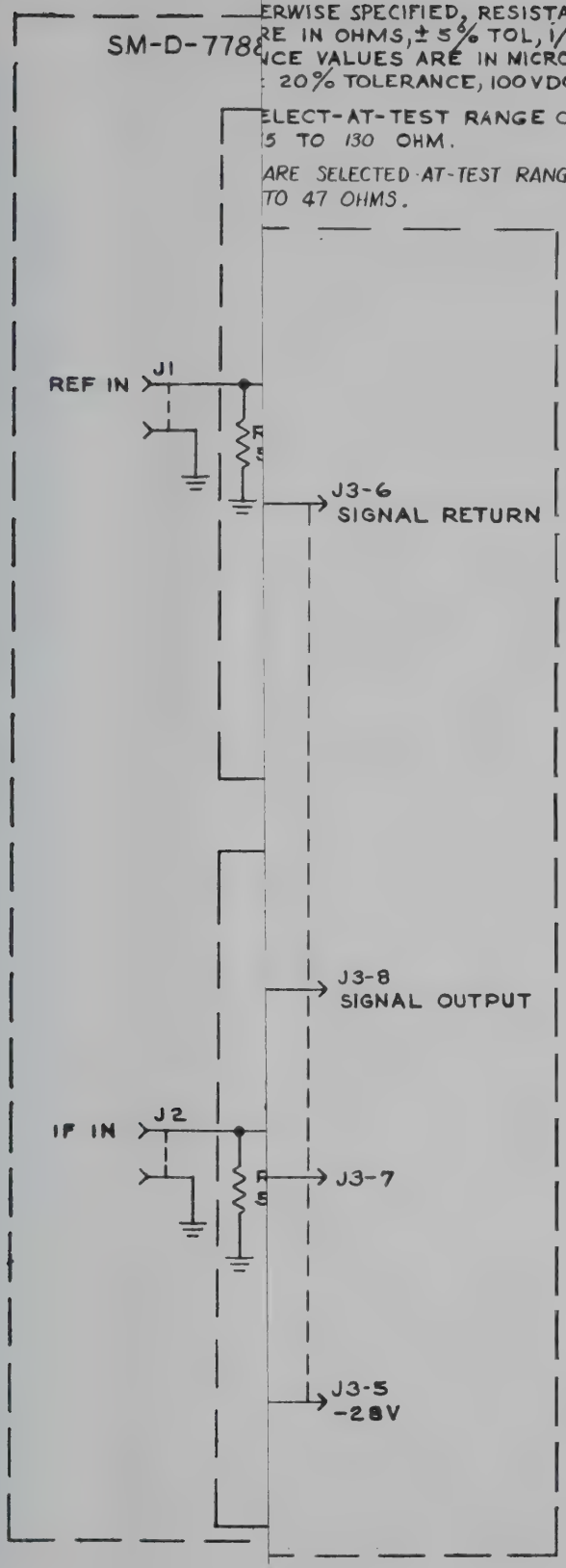
Figure FO 3-23. 14 MHz if. amplifier A13, schematic diagram.

SM-D-7788

ERWISE SPECIFIED, RESISTANCE
RE IN OHMS, ± 5% TOL, 1/4 W,
NCE VALUES ARE IN MICRO-
20% TOLERANCE, 100 VDC.

ELECT-AT-TEST RANGE OF
5 TO 130 OHM.

ARE SELECTED AT-TEST RANGE OF
TO 47 OHMS.



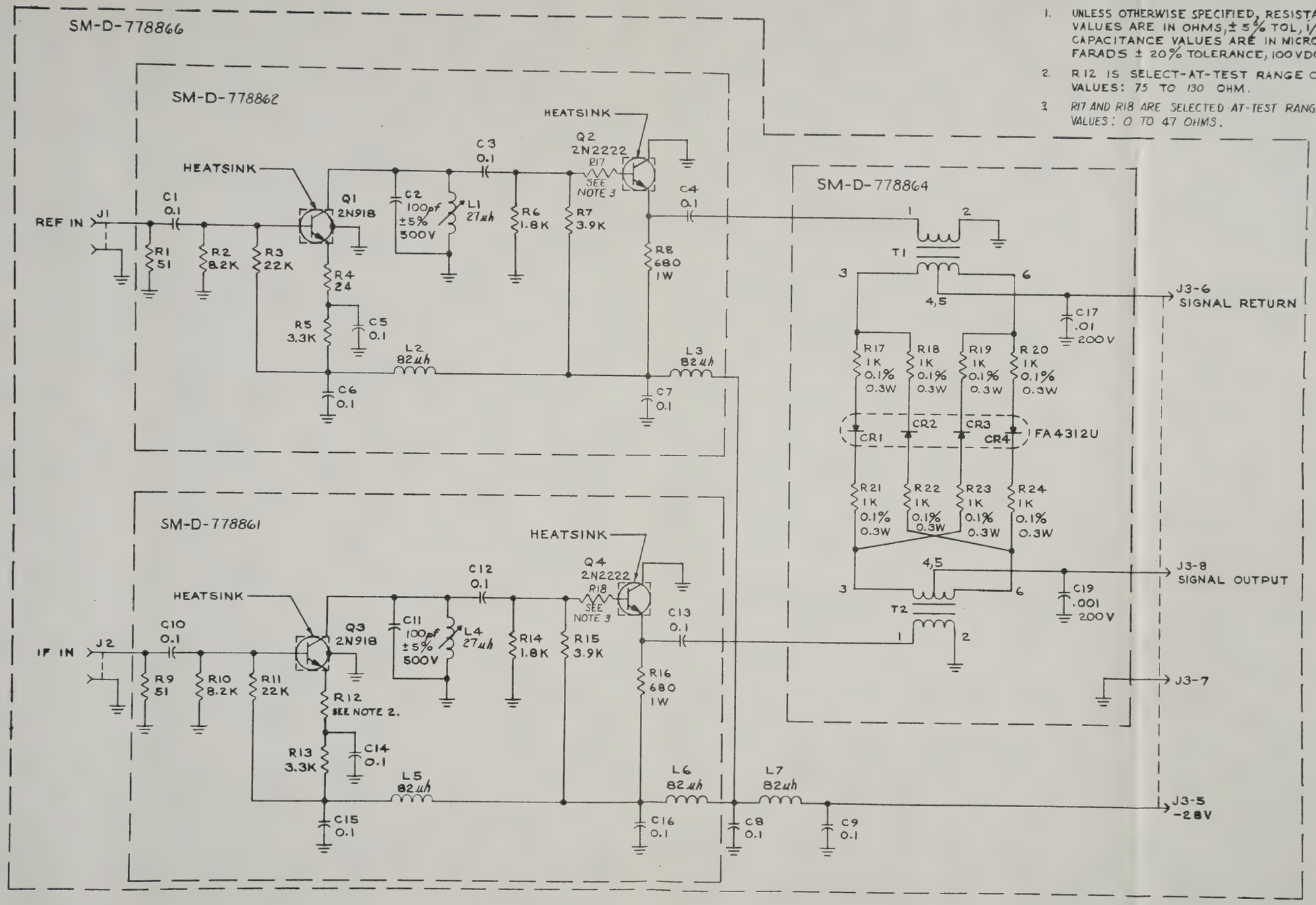
LAST NO. CHART	
LAST NO	UNUSED NO
J3	
R 24	
C 19	C 18
T 2	
Q 4	
L 7	

EL2LF101

NOTES:

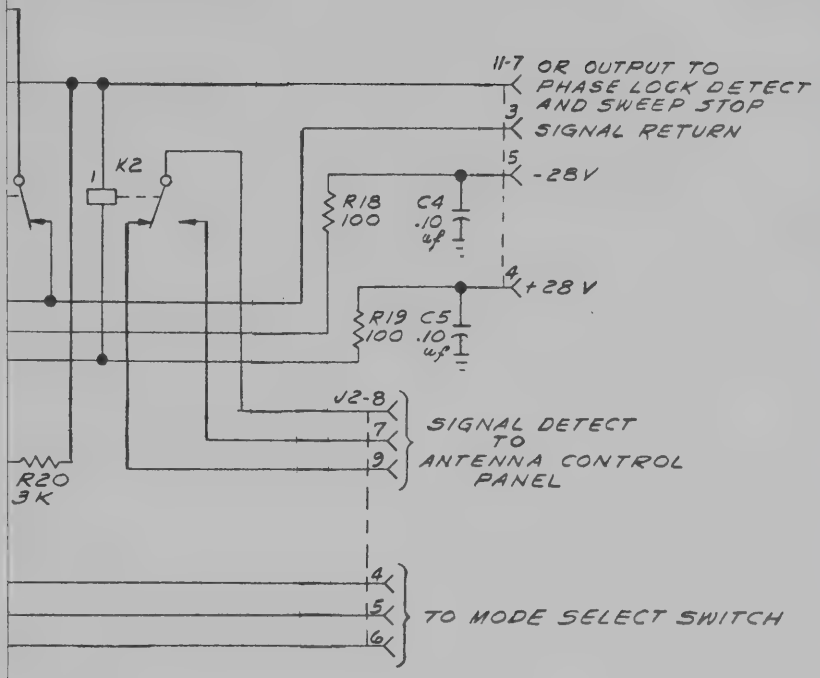
1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, ± 5% TOL, 1/4 W, CAPACITANCE VALUES ARE IN MICRO-FARADS ± 20% TOLERANCE, 100 VDC.
2. R12 IS SELECT-AT-TEST RANGE OF VALUES: 75 TO 130 OHM.
3. R17 AND R18 ARE SELECTED AT-TEST RANGE OF VALUES: 0 TO 47 OHMS.

LAST NO. CHART	
LAST NO	UNUSED NO
J3	
R 24	
C19	C18
T2	
Q4	
L7	



EL2LF101

Figure FO 3-24. 2.8 MHz phase detector A15/A16, schematic diagram.



EL2LF104

hematic diagram.

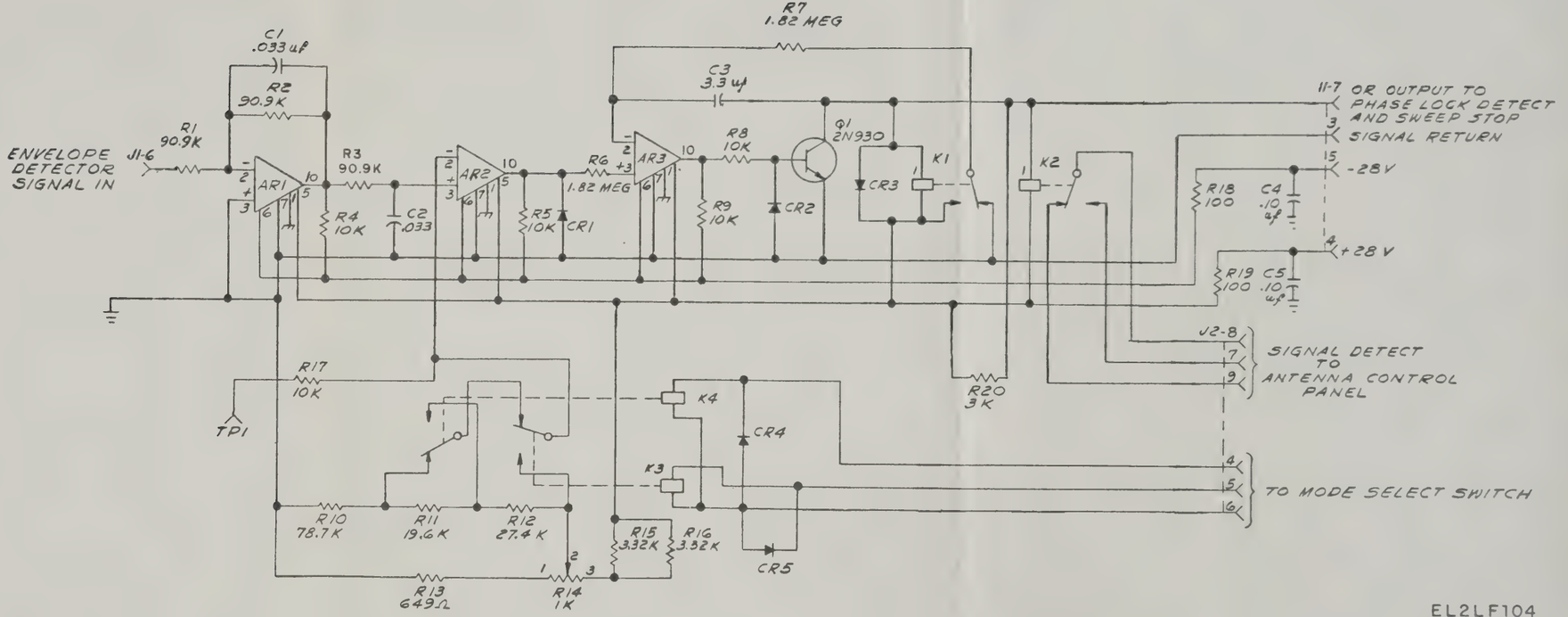
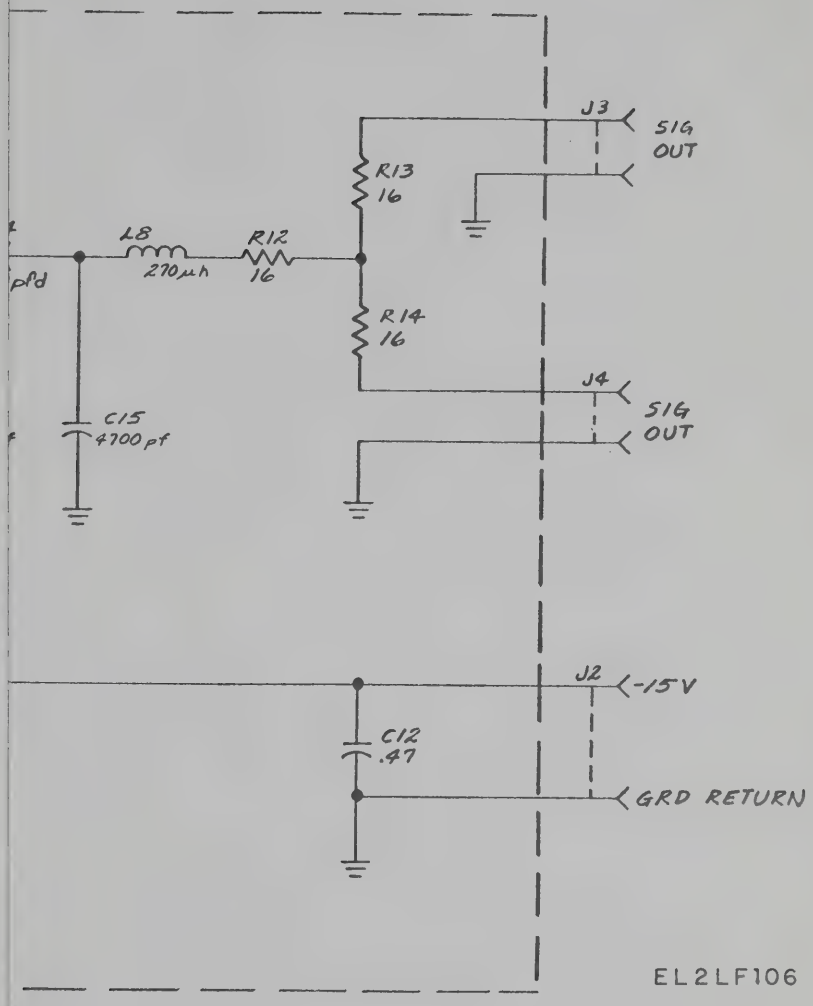


Figure FO 3-25. Signal detect circuit A22, schematic diagram.


J3
SIG
OUT
R13
16
L8
270μh
R12
16
pfd
R14
16
J4
SIG
OUT
C15
4700pf
J2
-15V
C12
.47
GRD RETURN

EL2LF106

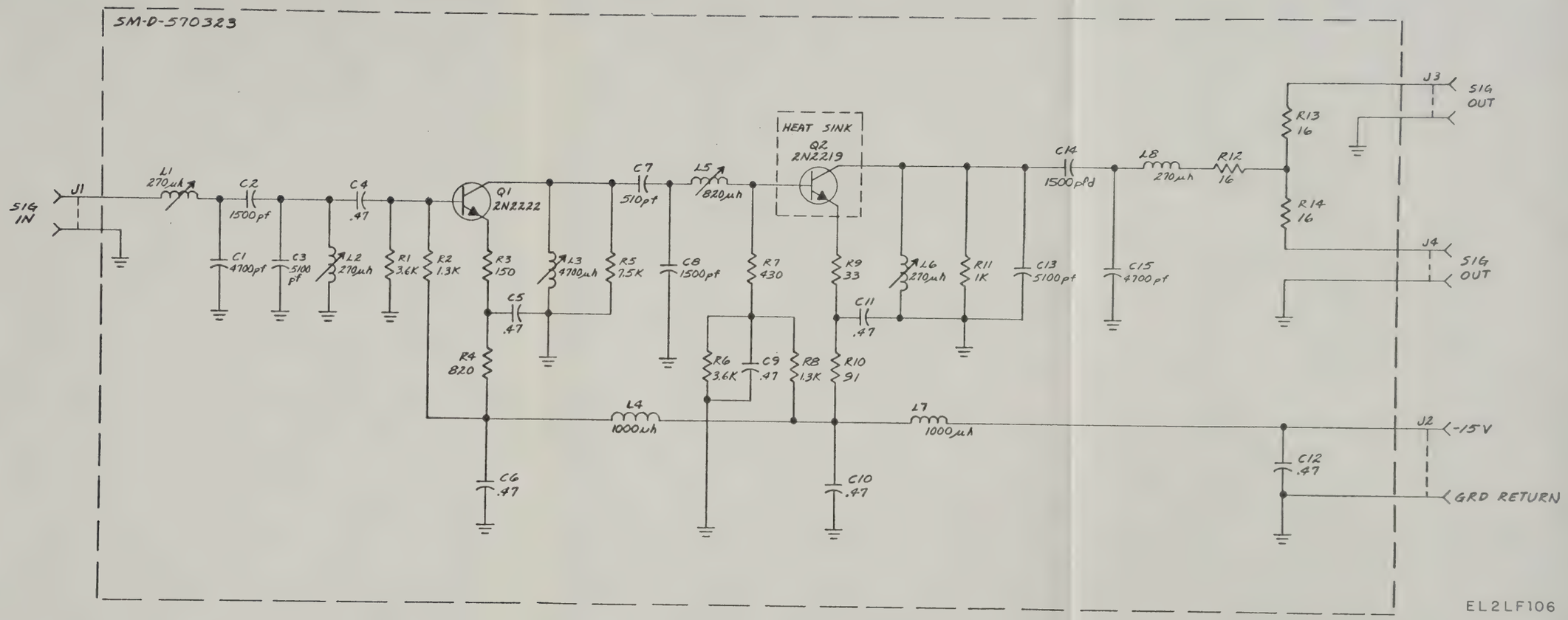
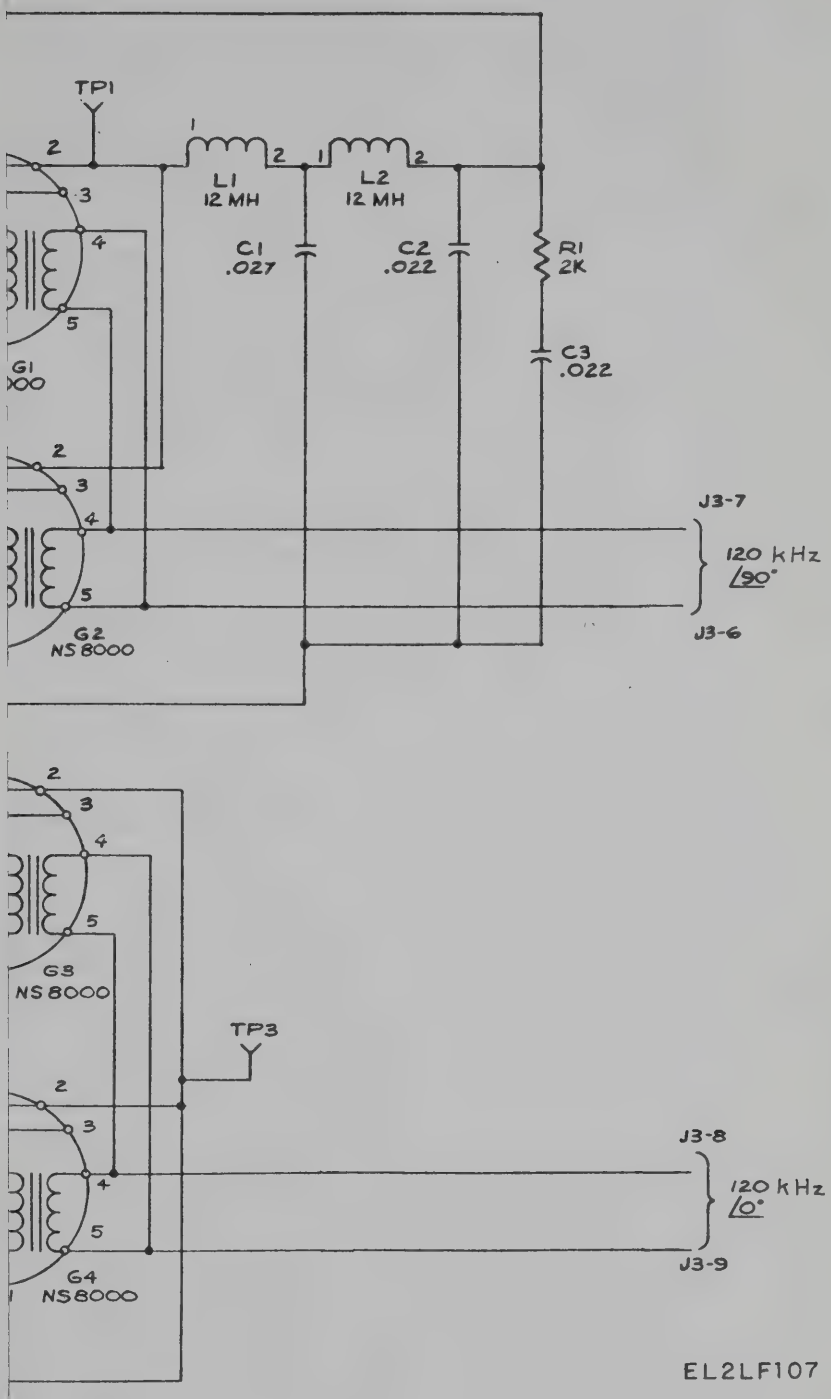


Figure FO 3-26. 120 kHz filter/amplifier A27, schematic diagram.


TP1
L1
12 MH
L2
12 MH
C1
.027
C2
.022
R1
2K
C3
.022
G1
G2
NS8000
J3-7
120 kHz
/90°
J3-6
G3
NS8000
TP3
G4
NS8000
J3-8
120 kHz
/0°
J3-9
EL2LF107

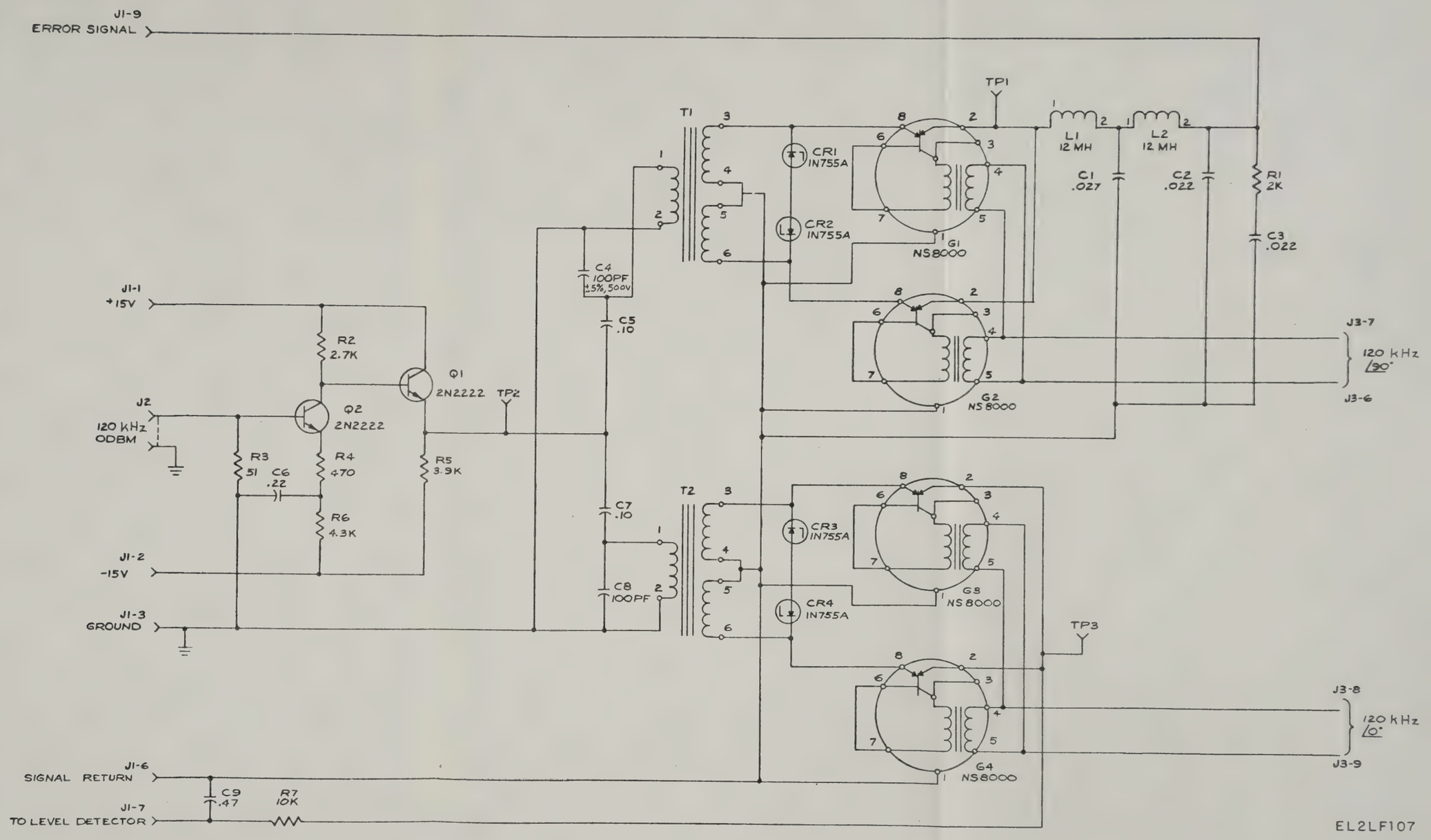
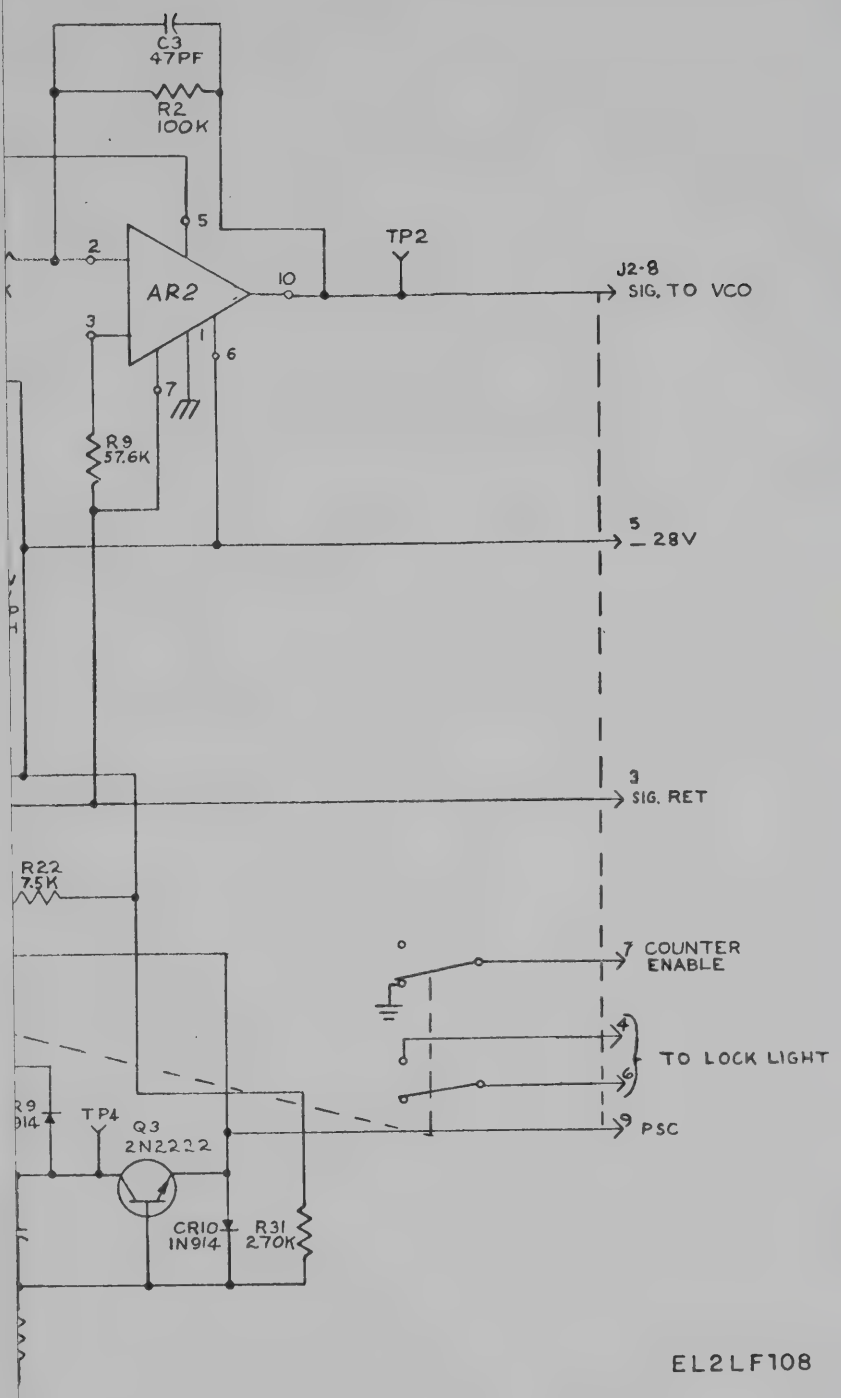


Figure FO 3-27. 120 kHz loop phase detector A28, schematic diagram.


C3
47PF
R2
100K
AR2
TP2
J2-8
SIG. TO VCO
R9
57.6K
5
-28V
3
SIG. RET
R22
7.5K
7
COUNTER
ENABLE
TO LOCK LIGHT
9
PSC
TP4
Q3
2N2222
CR10
IN914
R31
270K
EL2LF108

ram.

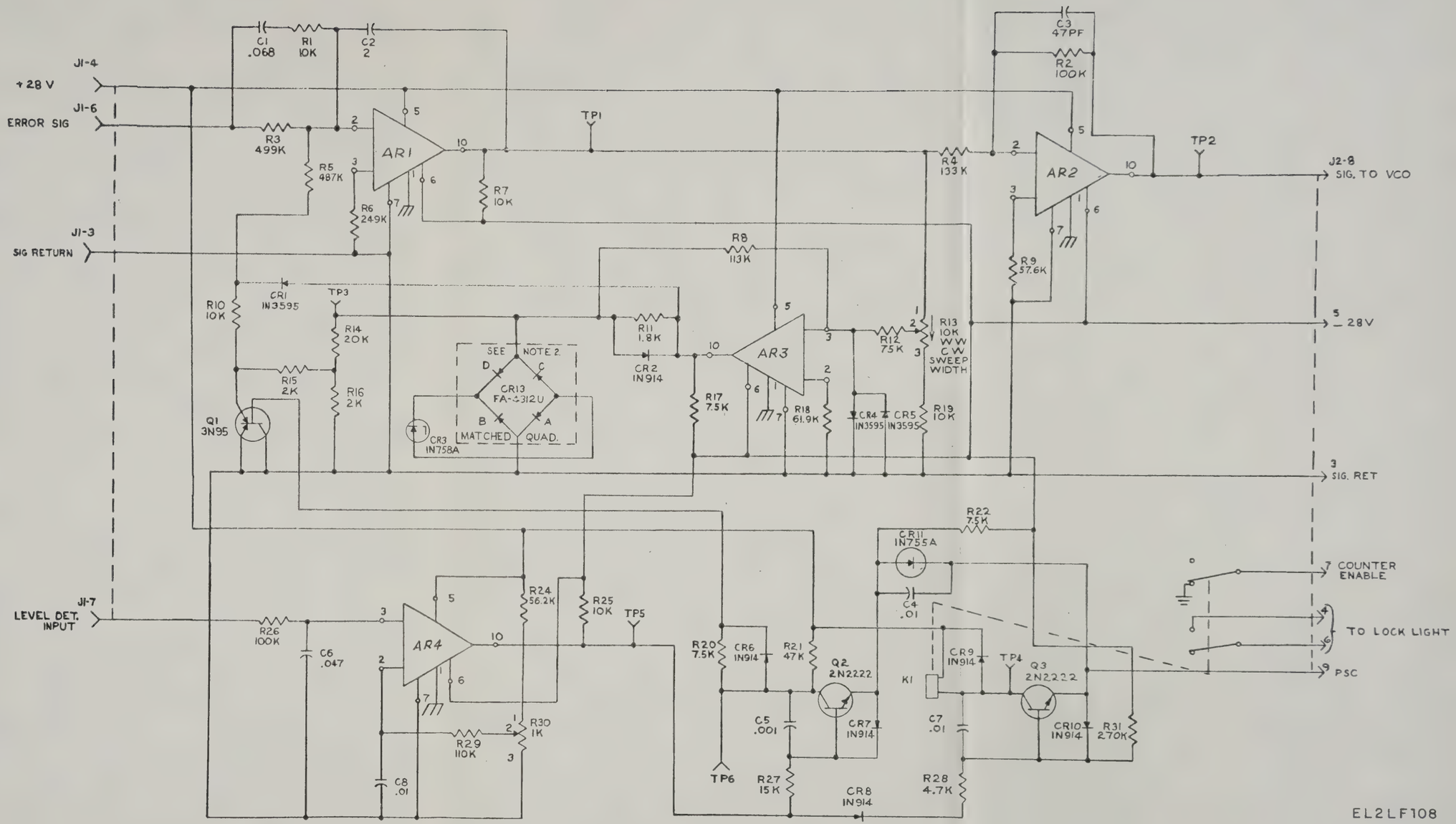
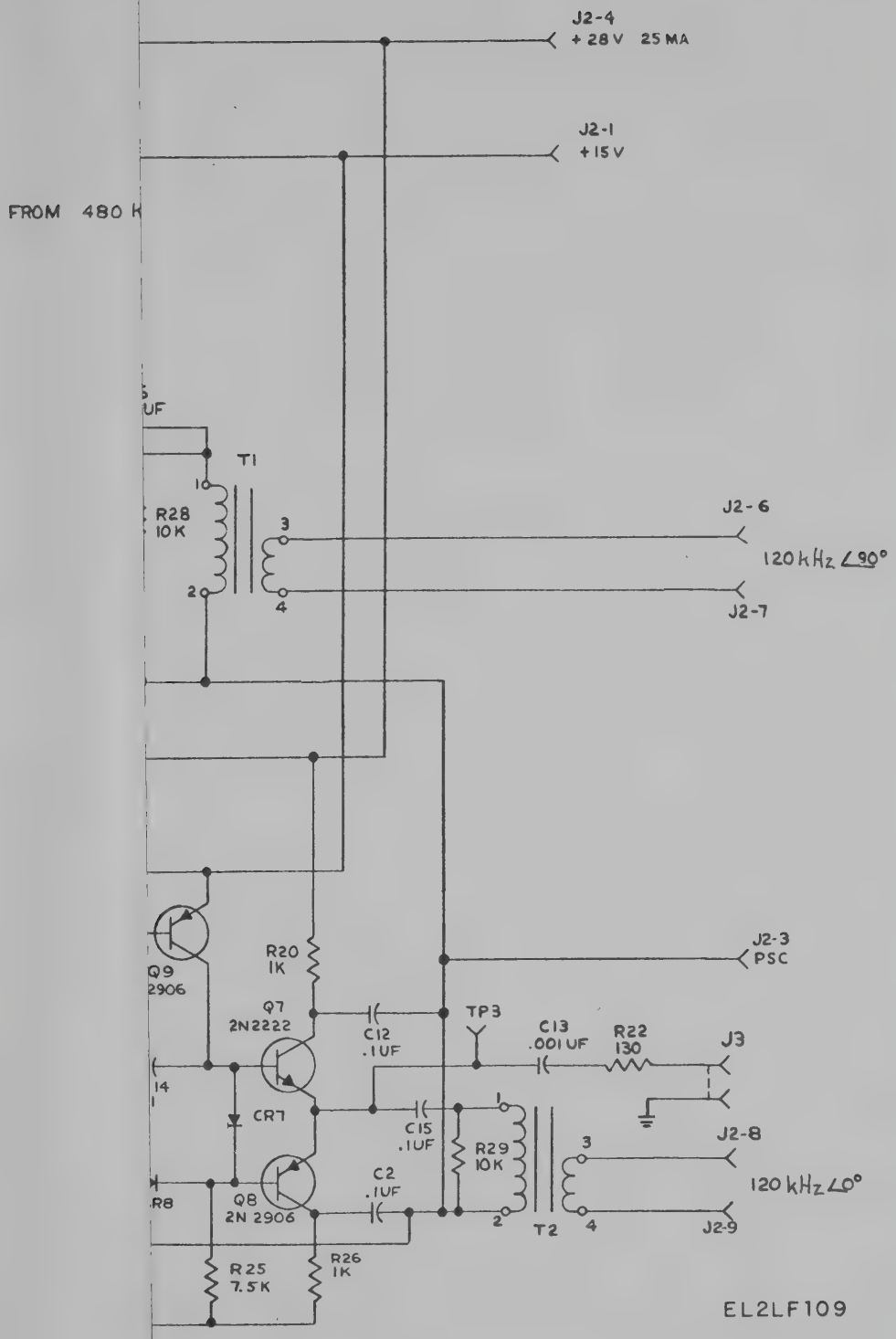


Figure FO 3-28. ID sweep, loop filter, and acquisition circuit A29, schematic diagram.


J2-4
+28V 25MA
J2-1
+15V
FROM 480 K
T1
R28
10K
J2-6
120kHz ∠90°
J2-7
Q9
2906
R20
1K
J2-3
PSC
Q7
2N2222
C12
.1UF
TP3
C13
.001UF
R22
130
J3
CR7
C15
.1UF
R29
10K
J2-8
120kHz ∠0°
C2
.1UF
Q8
2N 2906
T2
J2-9
R25
7.5K
R26
1K
EL2LF109

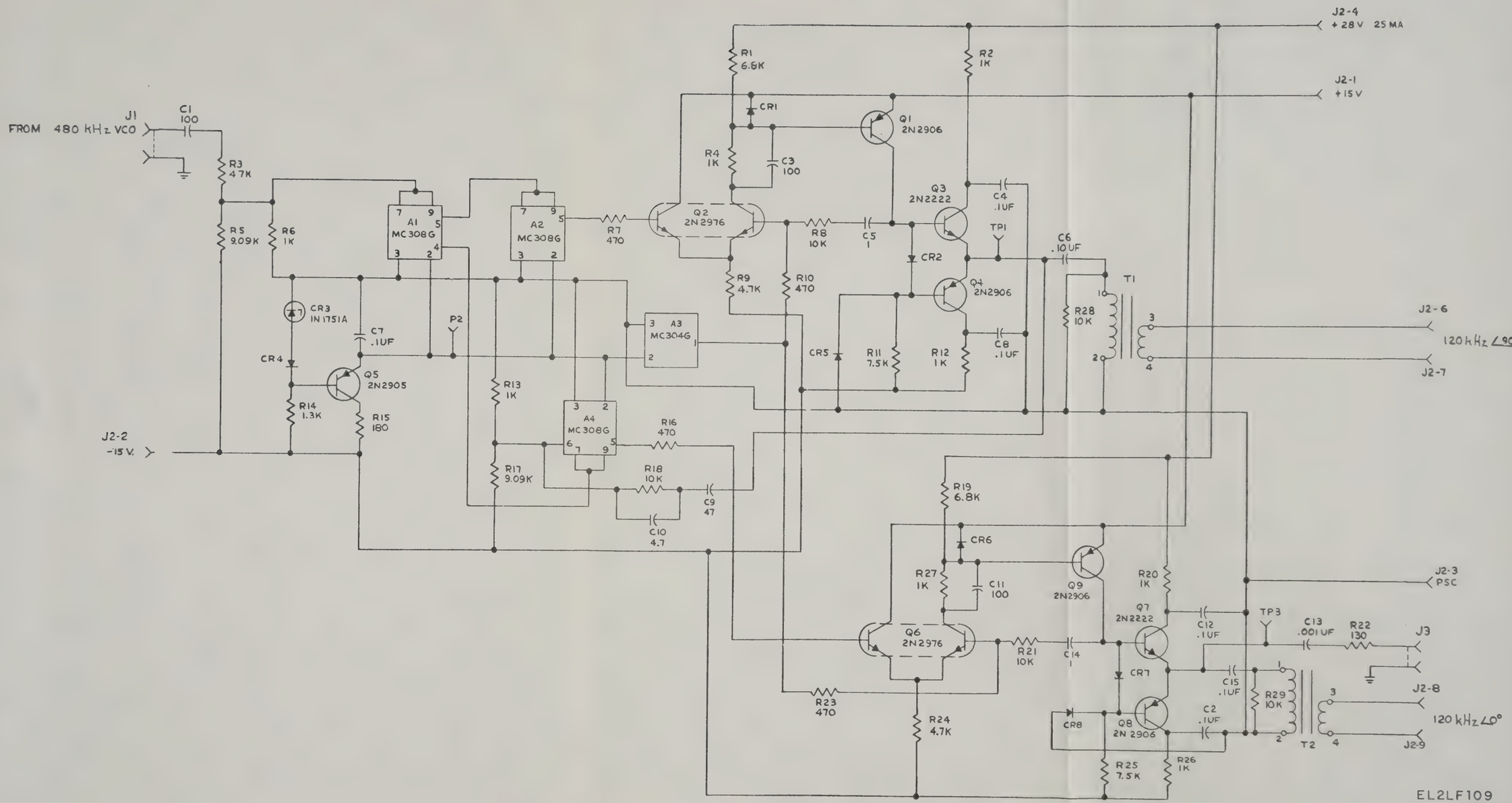


Figure FO 3-29. ID 4-to-1 countdown and quadrature circuit A30, schematic diagram.

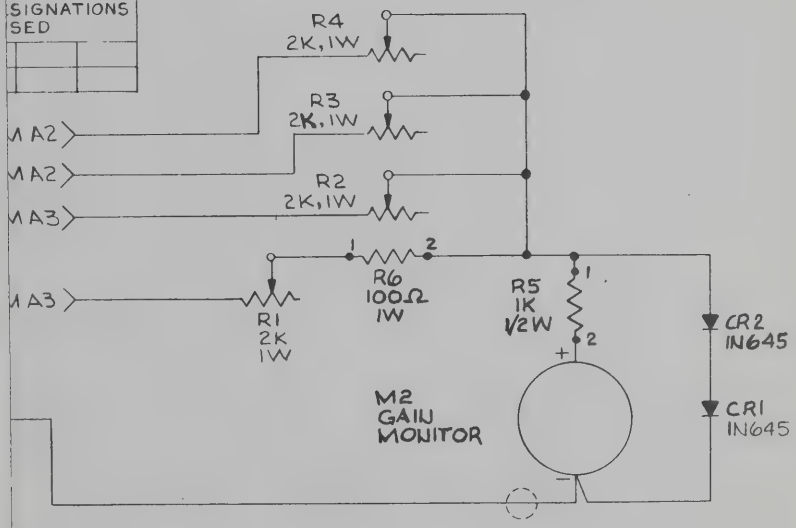
NSLATOR
R CURRENT

OT GENERATOR

NOTES:

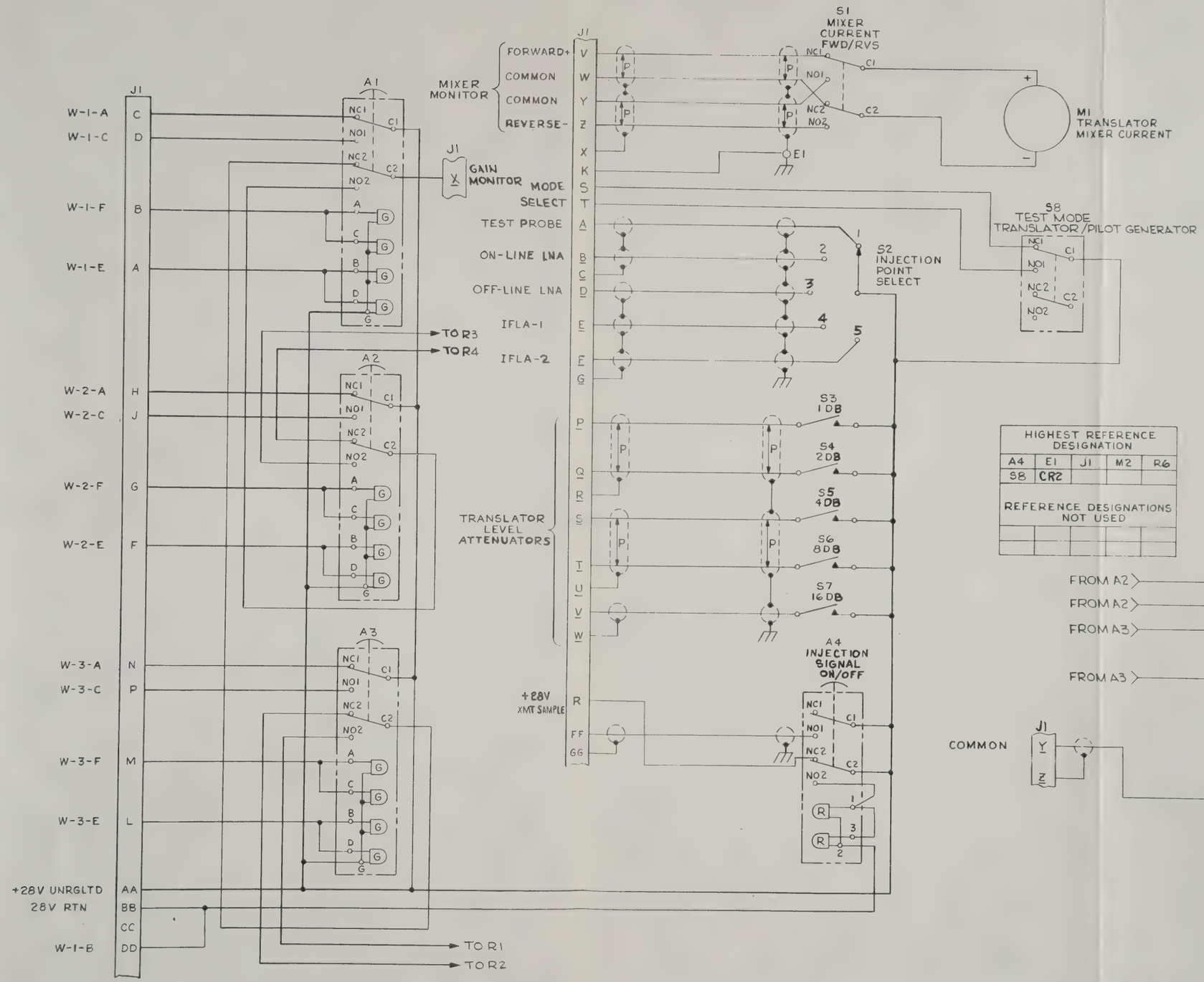
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATIONS.
2. UNDERLINED LETTERS SIGNIFY LOWER-CASE LETTERS.
3. UNLESS OTHERWISE NOTED; ALL WIRE IS AWG 20, WHITE.

FERENCE ATION		
	M2	R6
SIGNATIONS SED		



+28V U
28V

EL2LF115

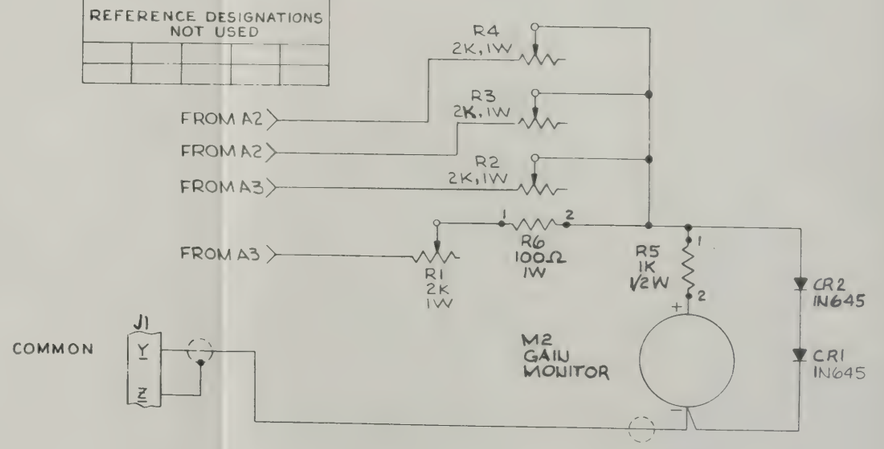


HIGHEST REFERENCE DESIGNATION				
A4	E1	J1	M2	R6
S8	CR2			

REFERENCE DESIGNATIONS NOT USED

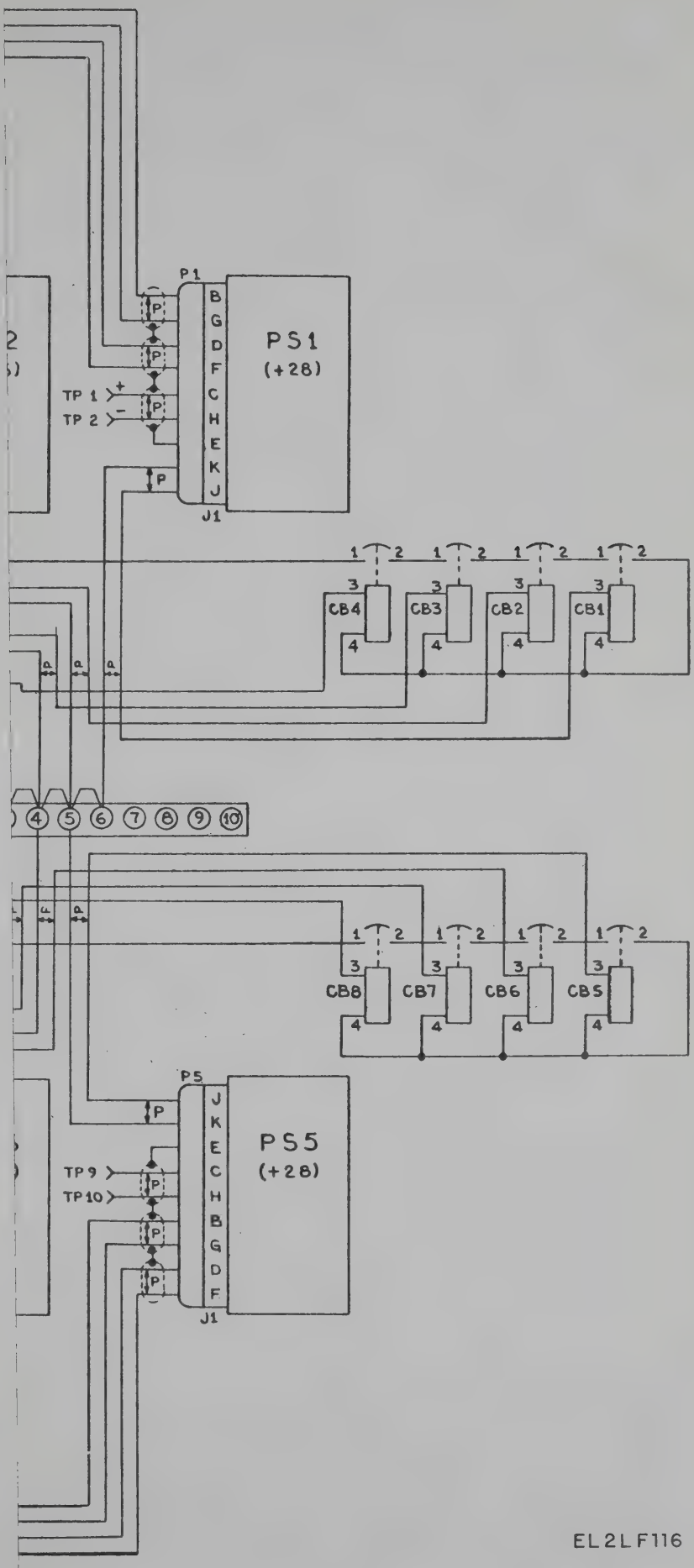
NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATIONS.
2. UNDERLINED LETTERS SIGNIFY LOWER-CASE LETTERS.
3. UNLESS OTHERWISE NOTED; ALL WIRE IS AWG 20, WHITE.



EL2LF115

Figure FO 3-30. Test translator control 1A2A26, schematic diagram.


P1
B
G
D
F
C
H
E
K
J
J1
PS1
(+28)
TP 1
TP 2
+
-
P
CB4
CB3
CB2
CB1
1
2
3
4
4
5
6
7
8
9
10
CB8
CB7
CB6
CB5
P5
J
K
E
C
H
B
G
D
F
J1
PS5
(+28)
TP 9
TP10

EL2LF116

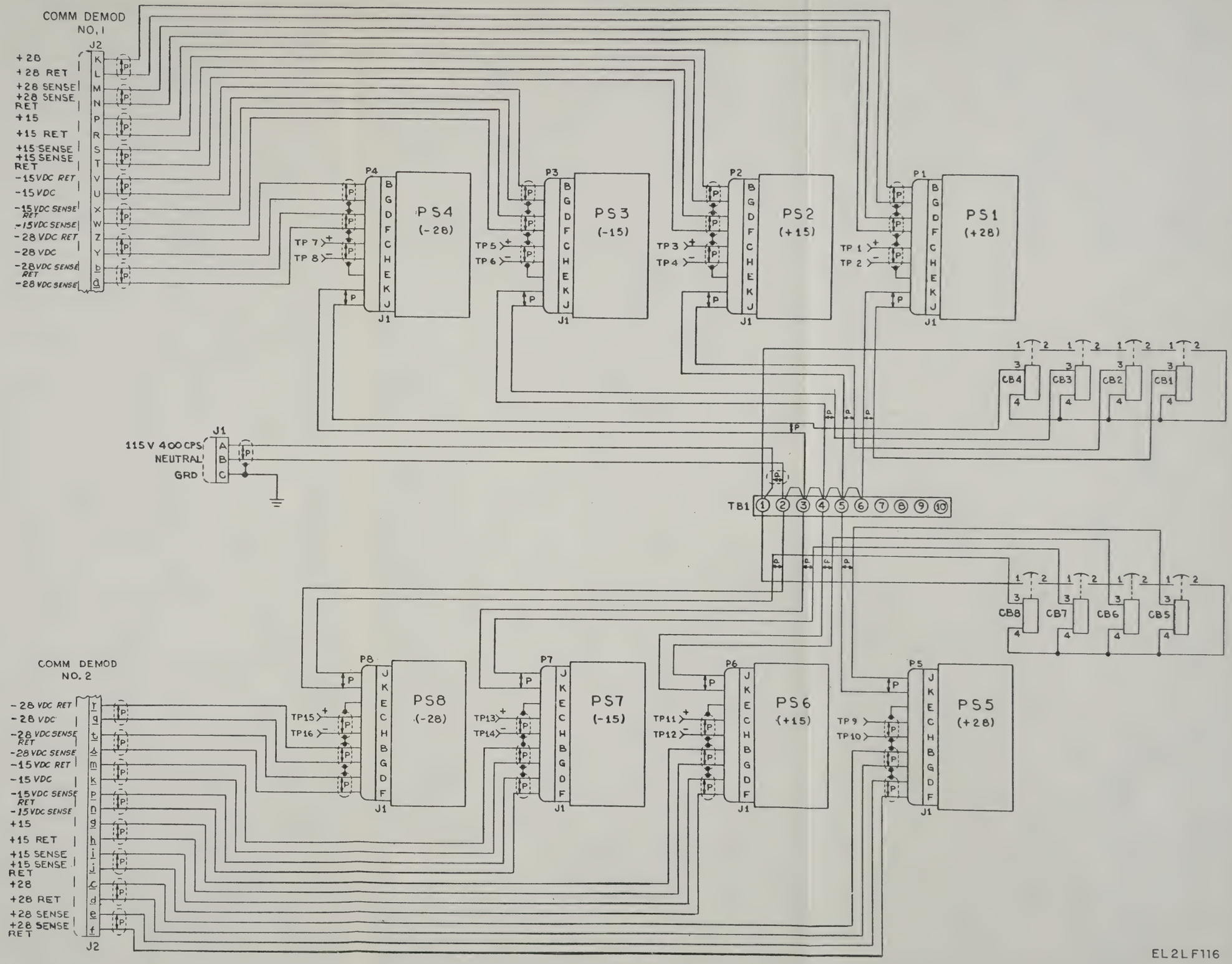
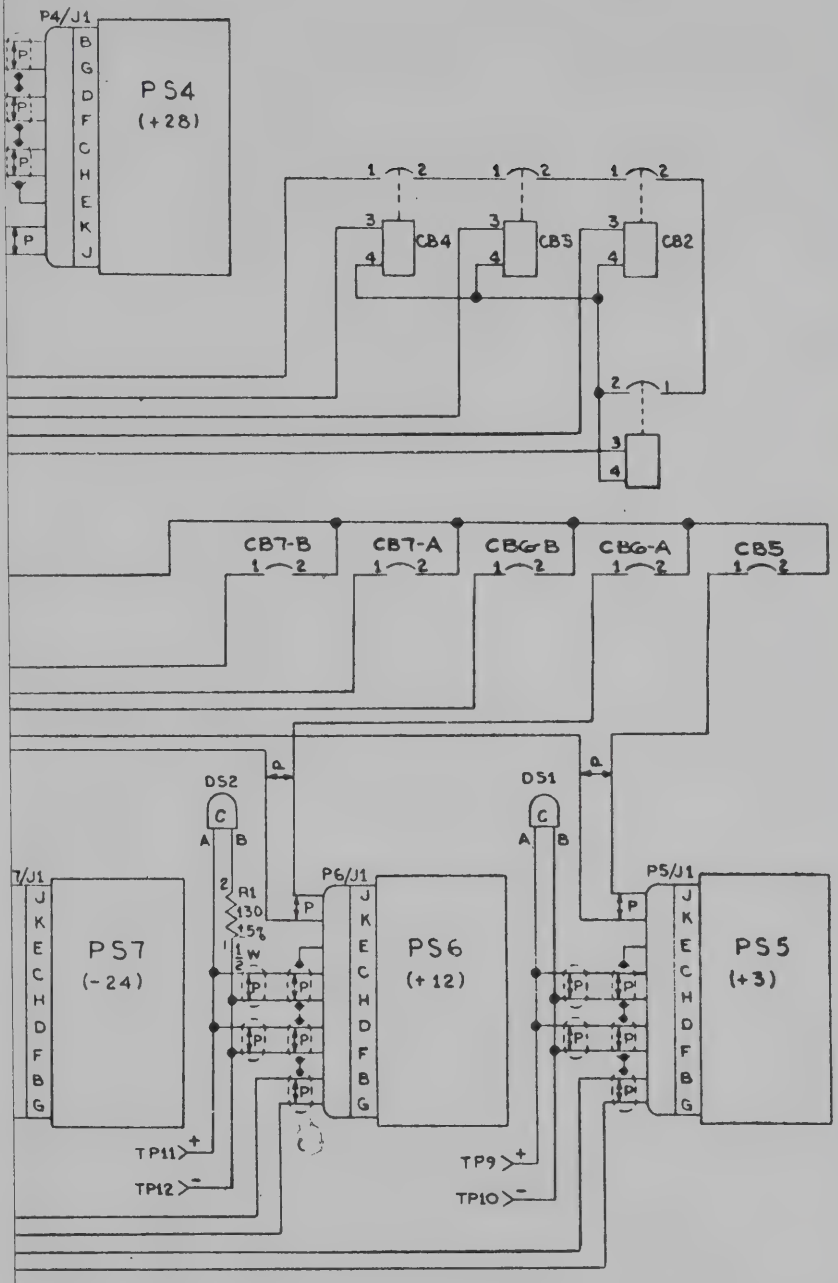


Figure FO 3-31. Comm demod power supplies 1A3A9, wiring diagram.


P4/J1
PS4
(+28)
CB4
CB3
CB2
CB7-B
CB7-A
CB6-B
CB6-A
CB5
DS2
DS1
R1
130
1%
1/2W
P6/J1
P5/J1
PS7
(-24)
PS6
(+12)
PS5
(+3)
TP11
TP12
TP9
TP10

EL2LF117

im.

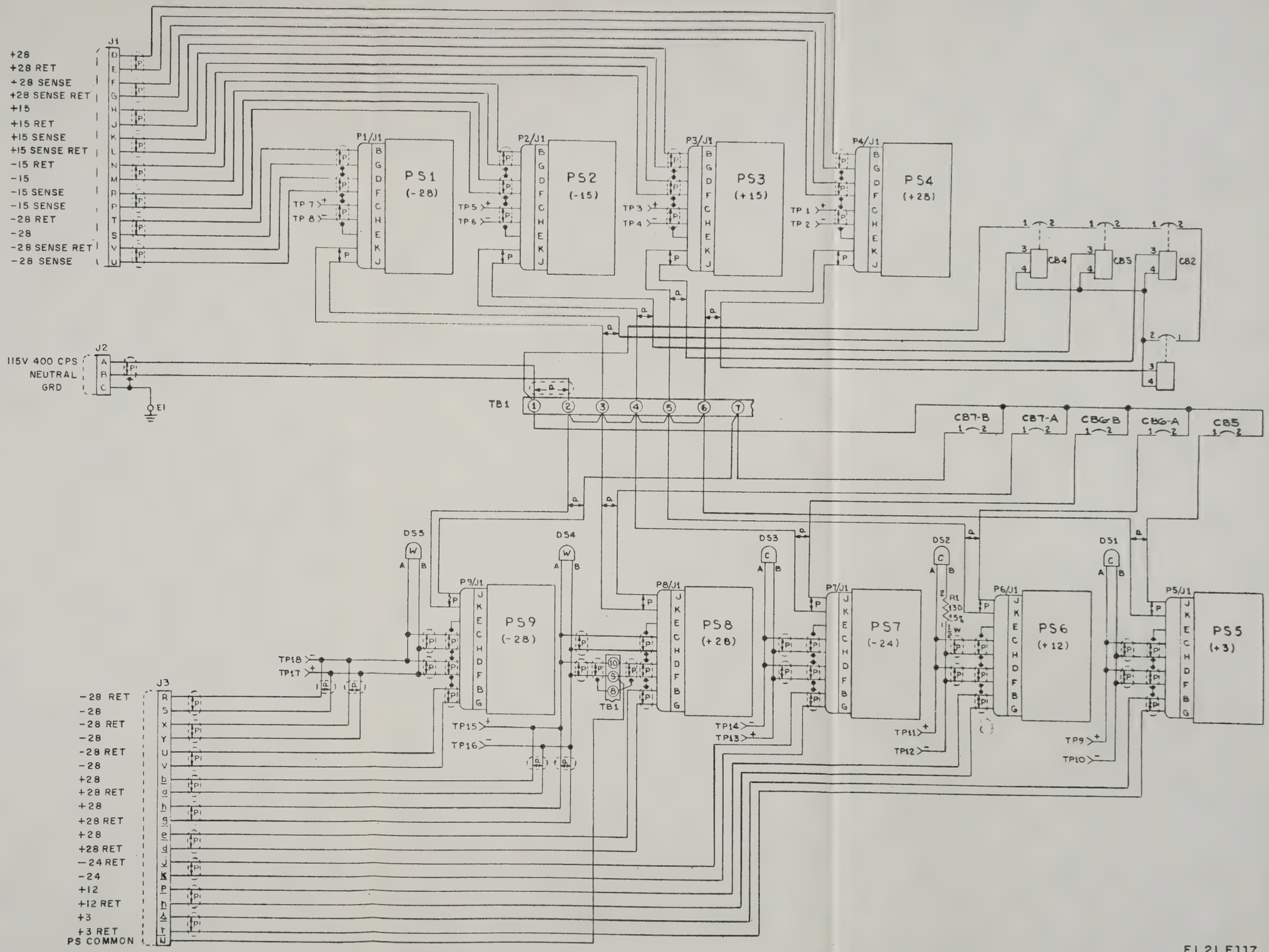


Figure FO 3-32. Beacon demod and baseband power supplies 1A3A10, wiring diagram.

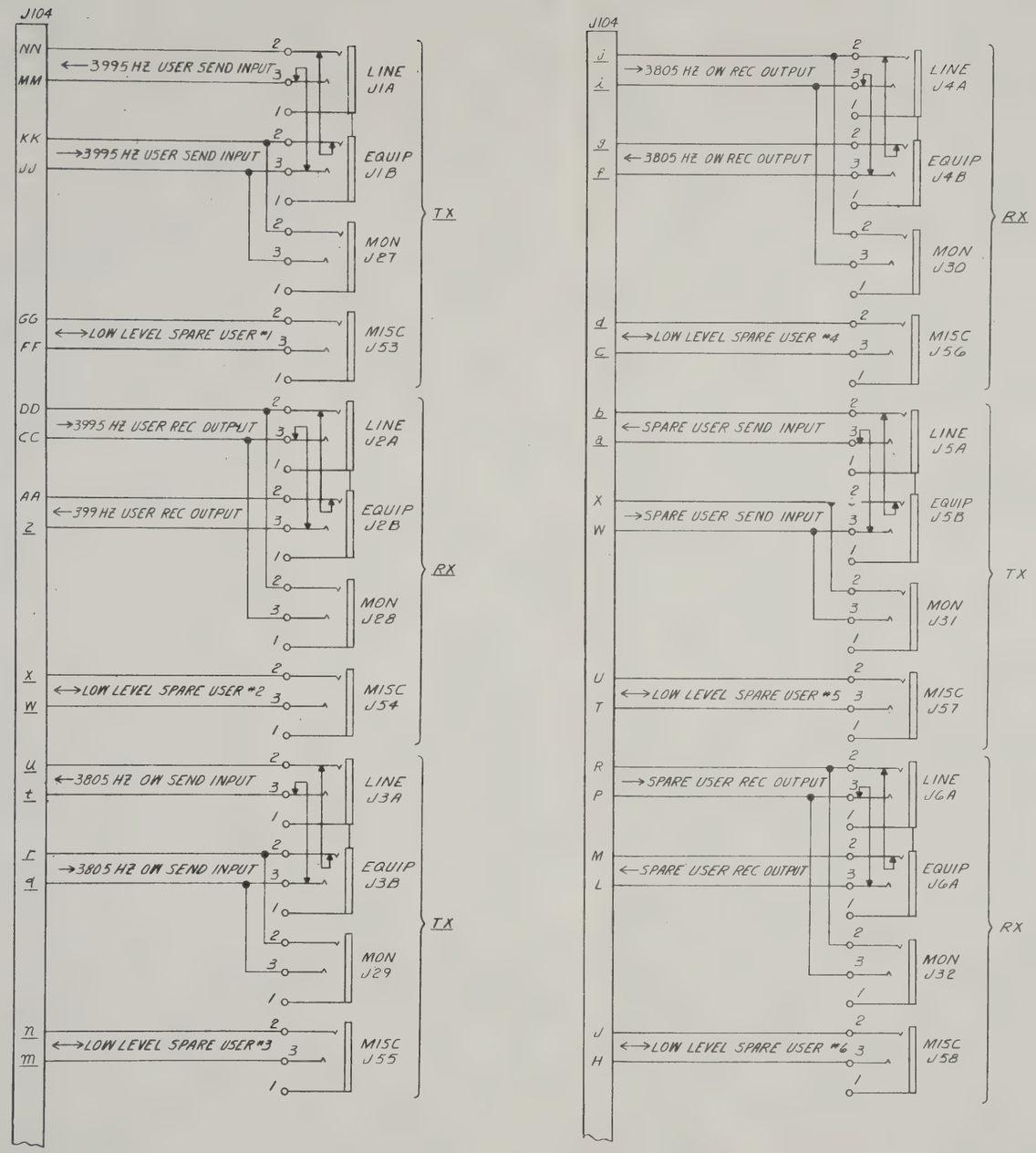
NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATIONS.
2. UNDERLINED LETTERS SIGNIFY LOWER-CASE LETTERS.

IGHEST REFERENCE DESIGNATION				
6	S1	TB3		

FERENCE DESIGNATIONS NOT USED				
03				

EL2LF118



NOTES:

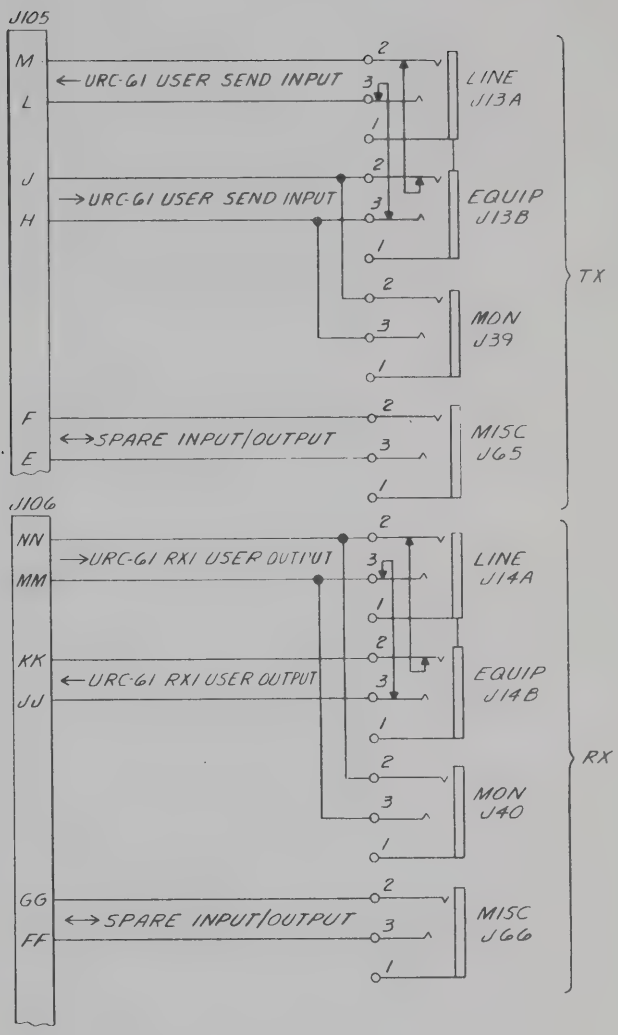
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATIONS.
2. UNDERLINED LETTERS SIGNIFY LOWER-CASE LETTERS.

HIGHEST REFERENCE DESIGNATION				
J106	S1	TB3		

REFERENCE DESIGNATIONS NOT USED				
J78-J103				

EL2LF118

Figure FO 3-33.① Teletypewriter patch panel 1A3A25, wiring diagram (sheet 1 of 4).



EL2LF119

m (sheet 2 of 4).

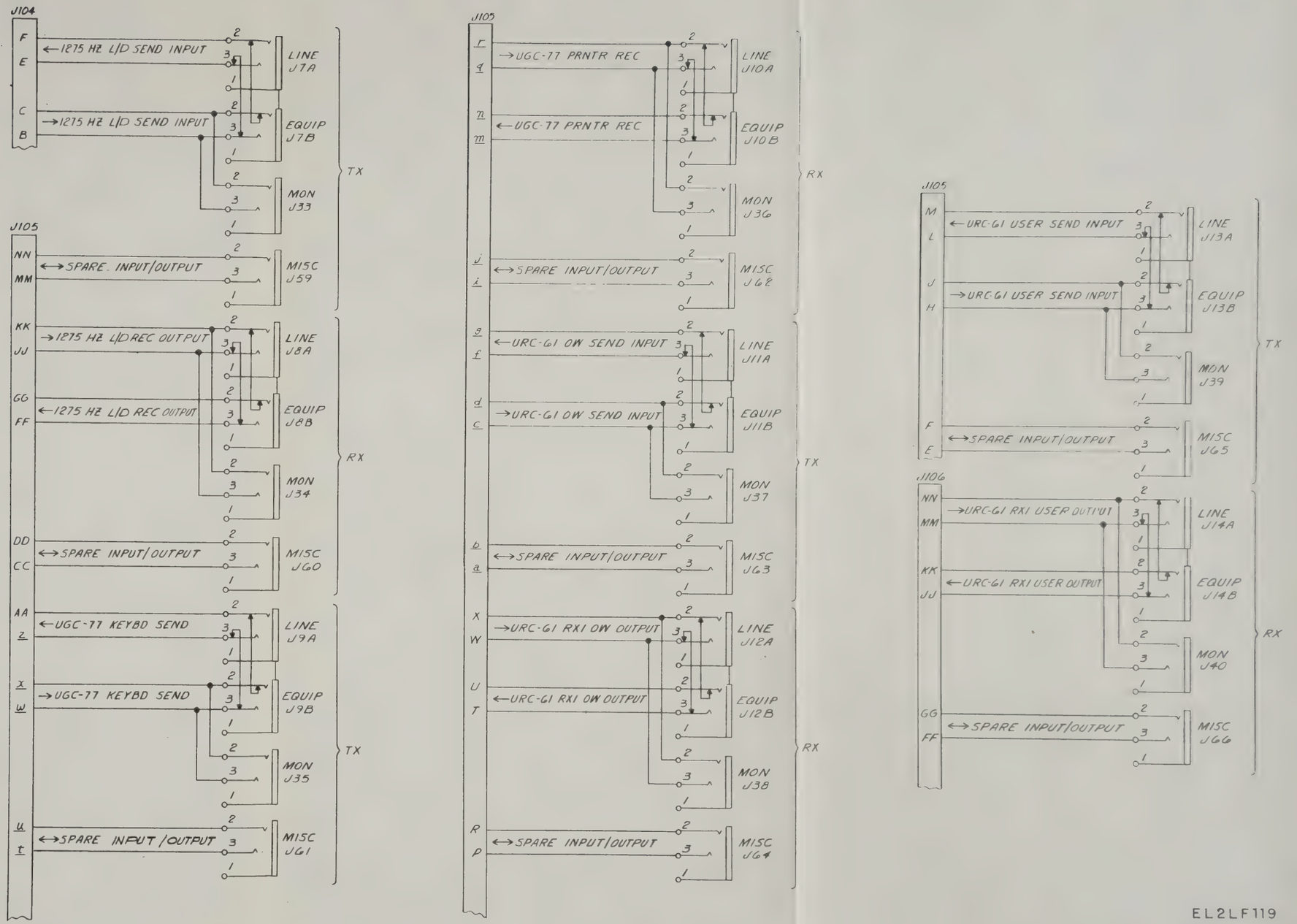
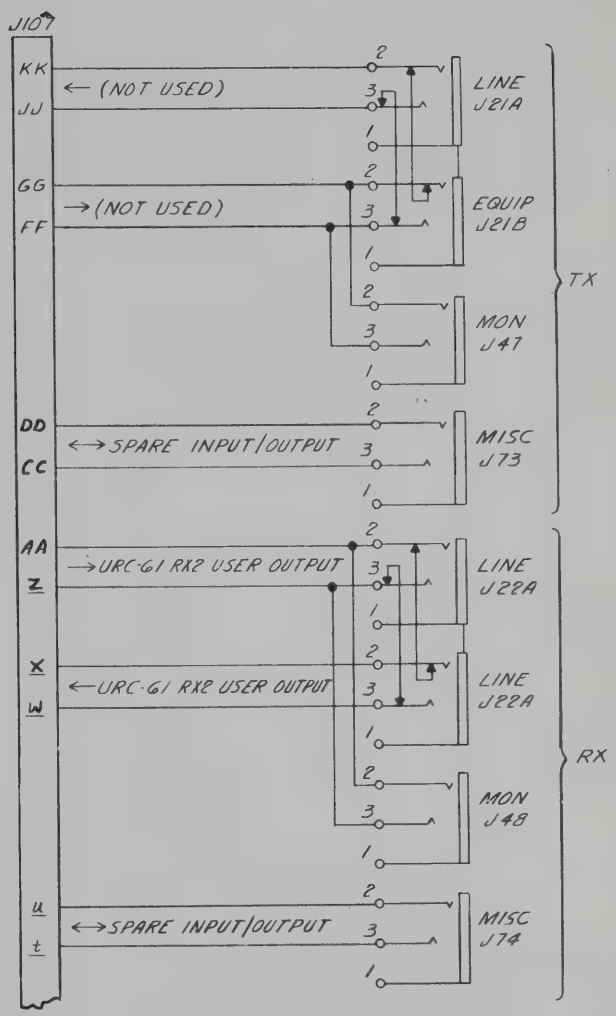


Figure FO 3-33. ②Teletypewriter patch panel 1A3A25, wiring diagram (sheet 2 of 4).

RX

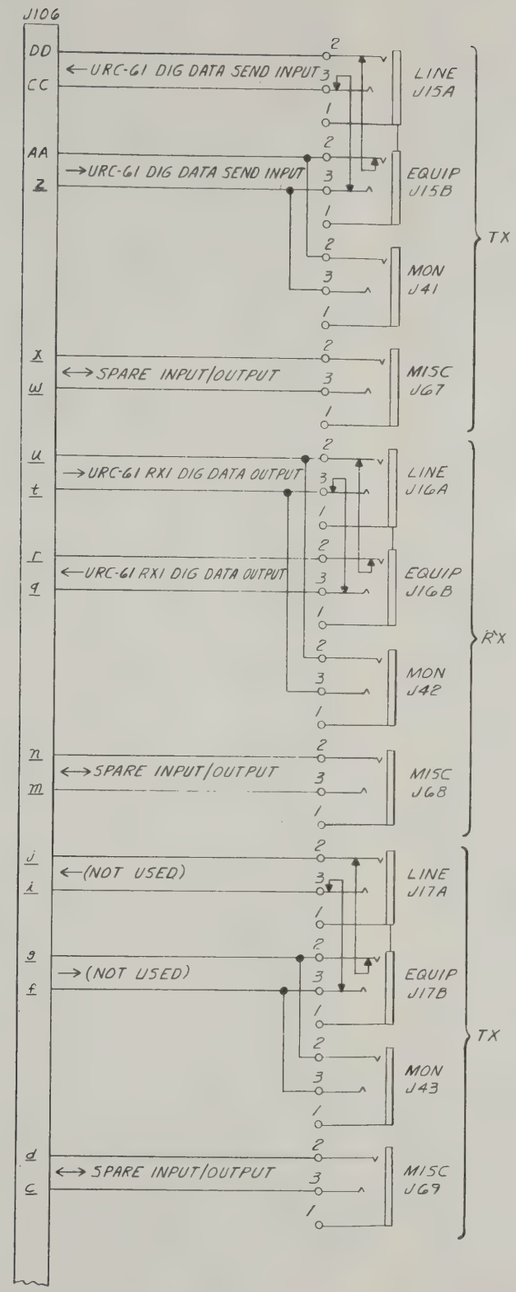
TX

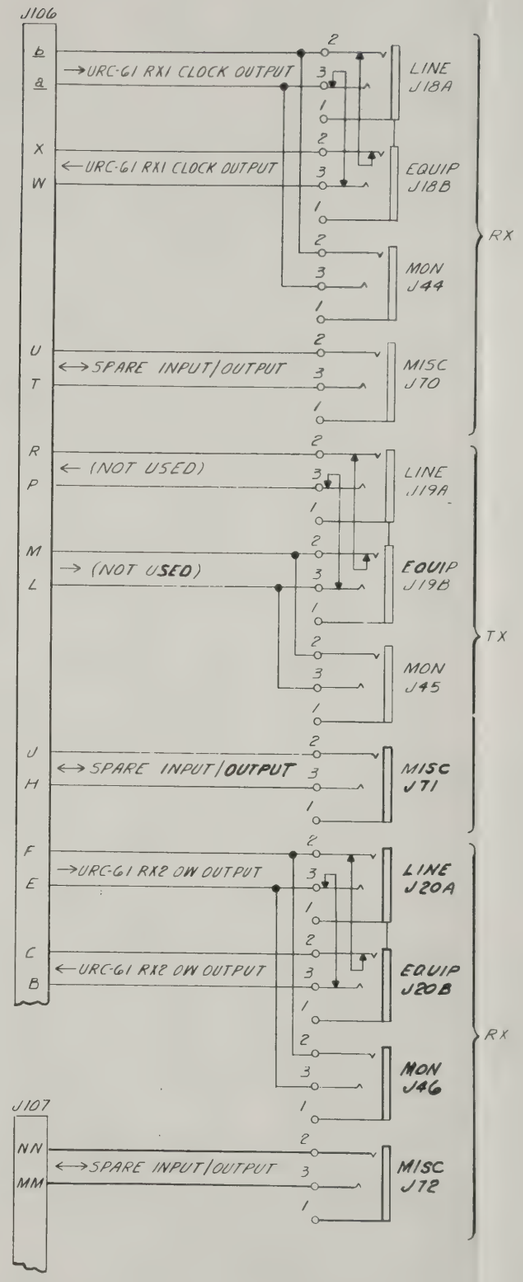
RX

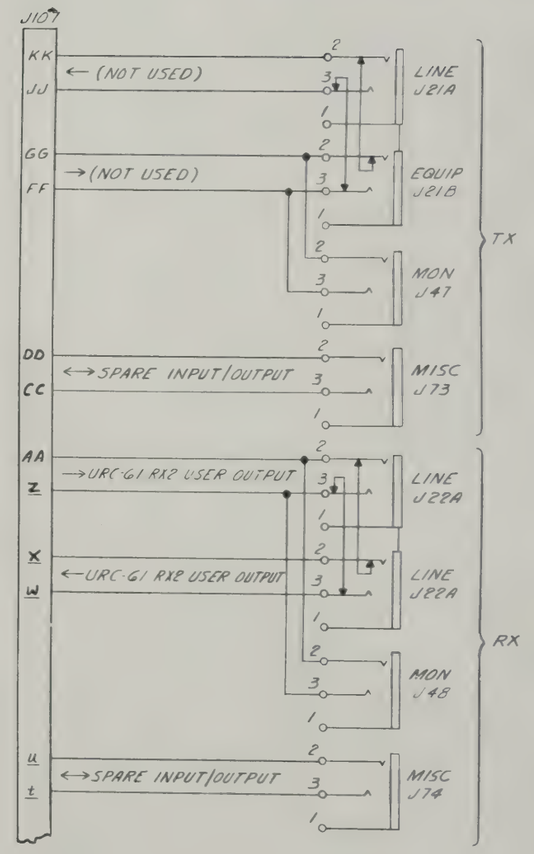


EL2LF120

ram (sheet 3 of 4).

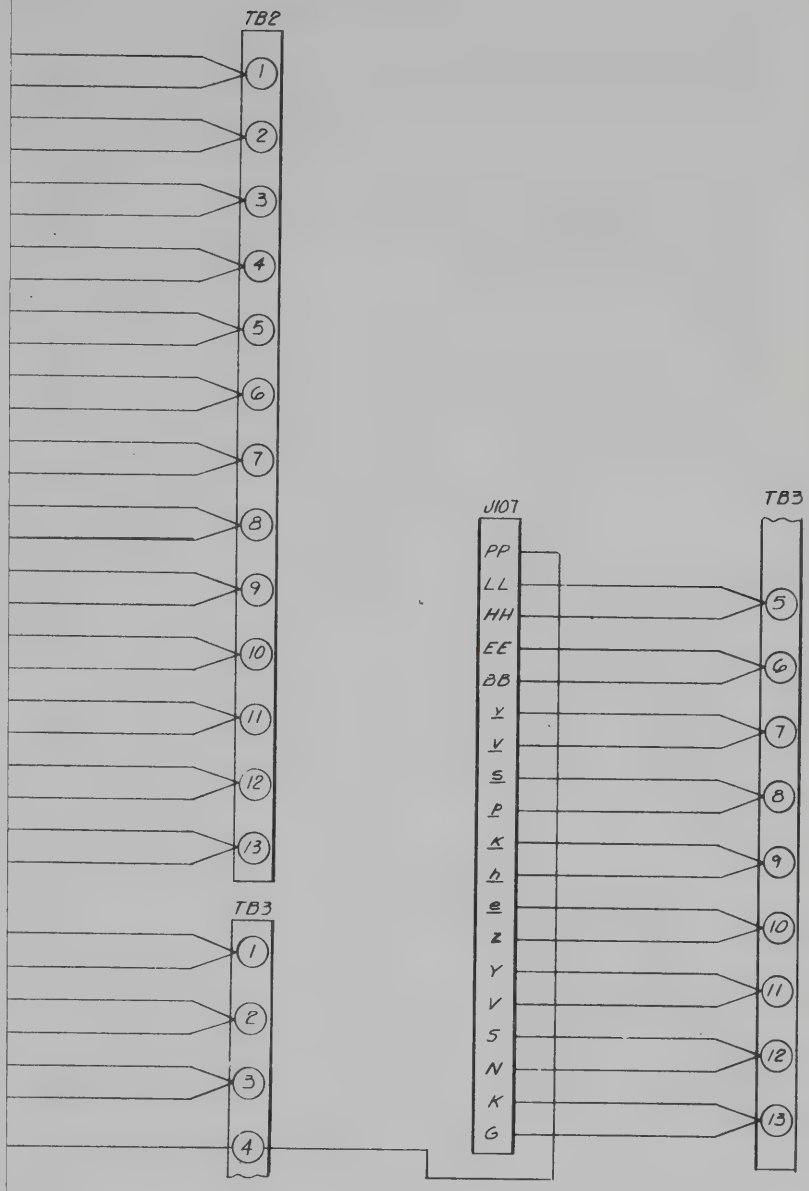






EL2LF120

Figure FO 3-33. ③Teletypewriter patch panel 1A3A25, wiring diagram (sheet 3 of 4).



EL2LF121

eet 4 of 4).

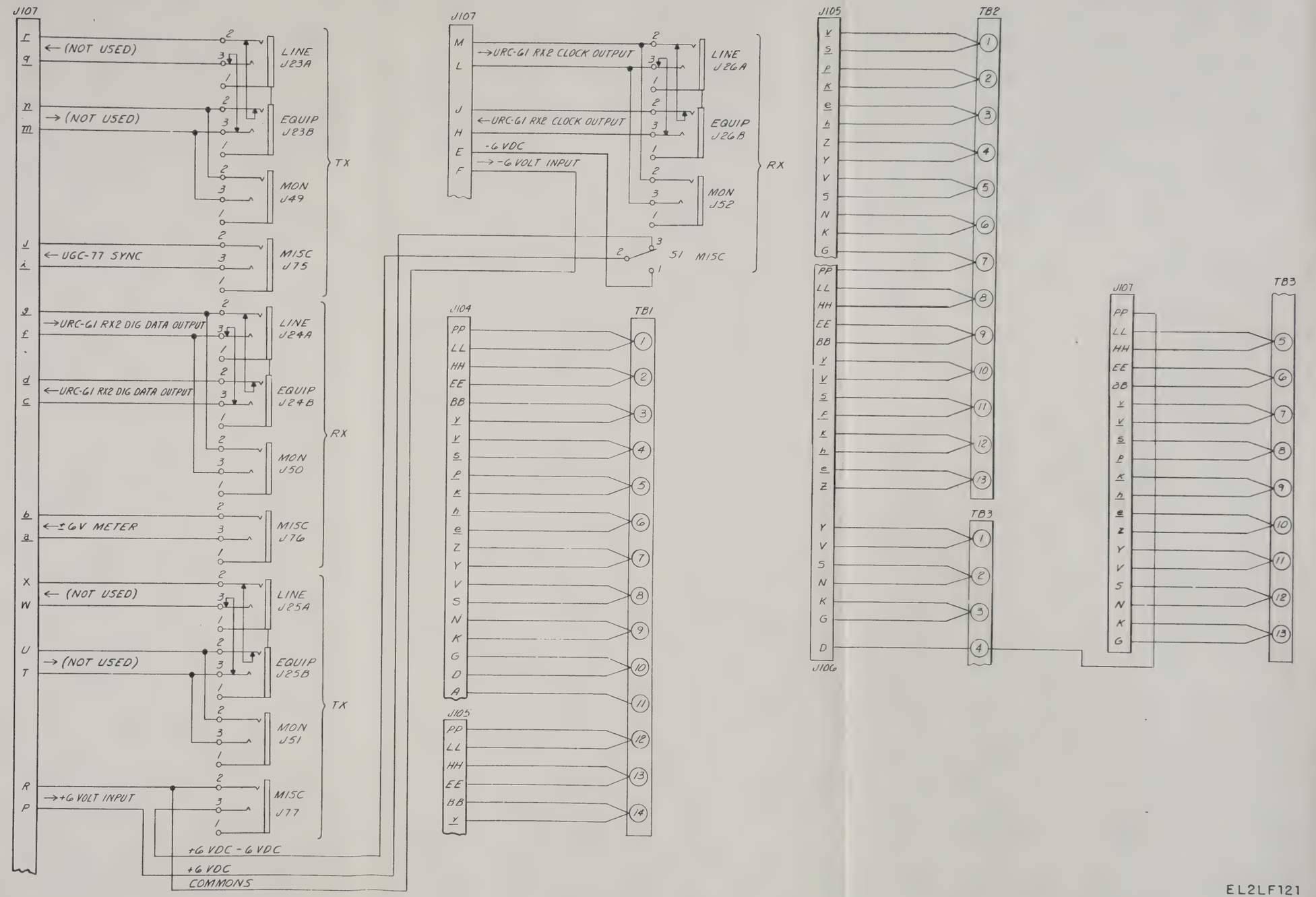
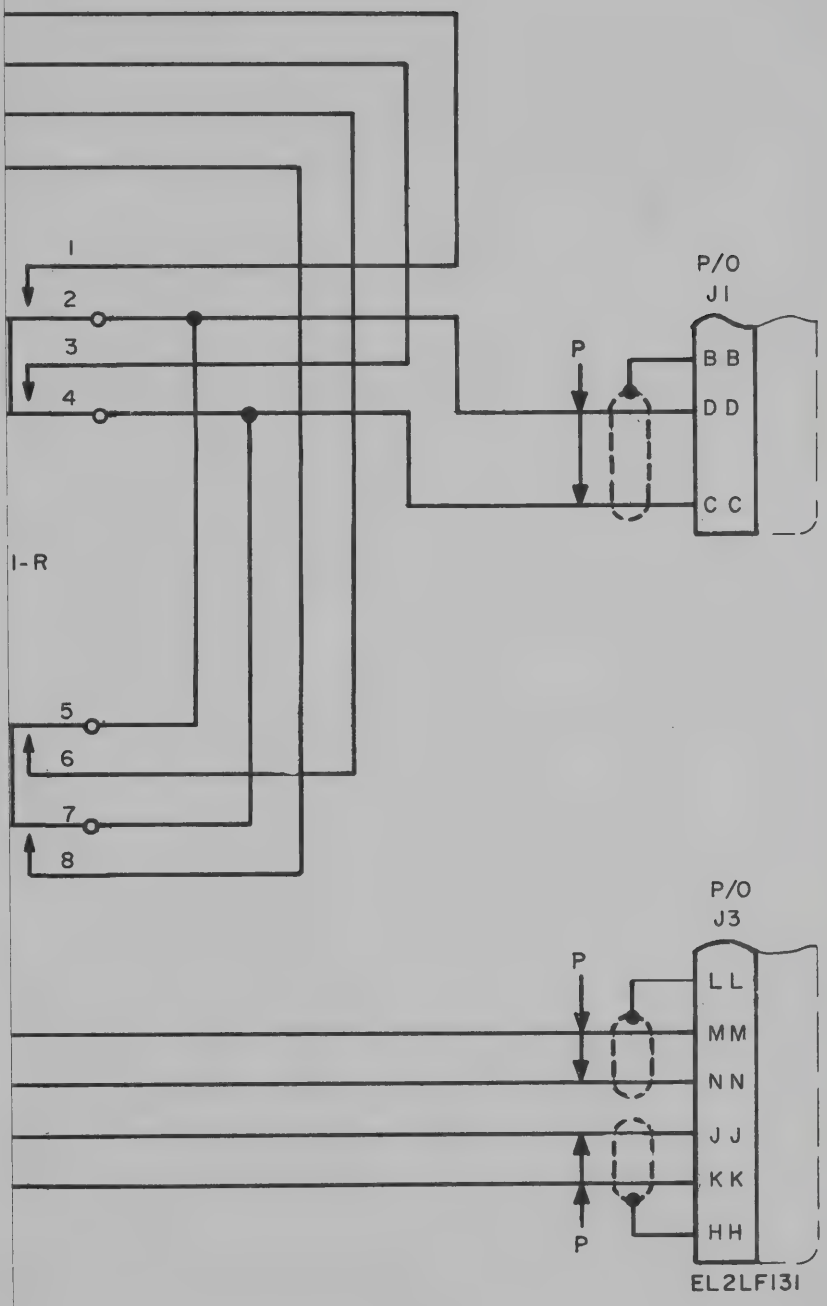


Figure FO 3-33. ④ Teletypewriter patch panel 1A3A25, wiring diagram (sheet 4 of 4).



13, schematic diagram (sheet 1 of 6).

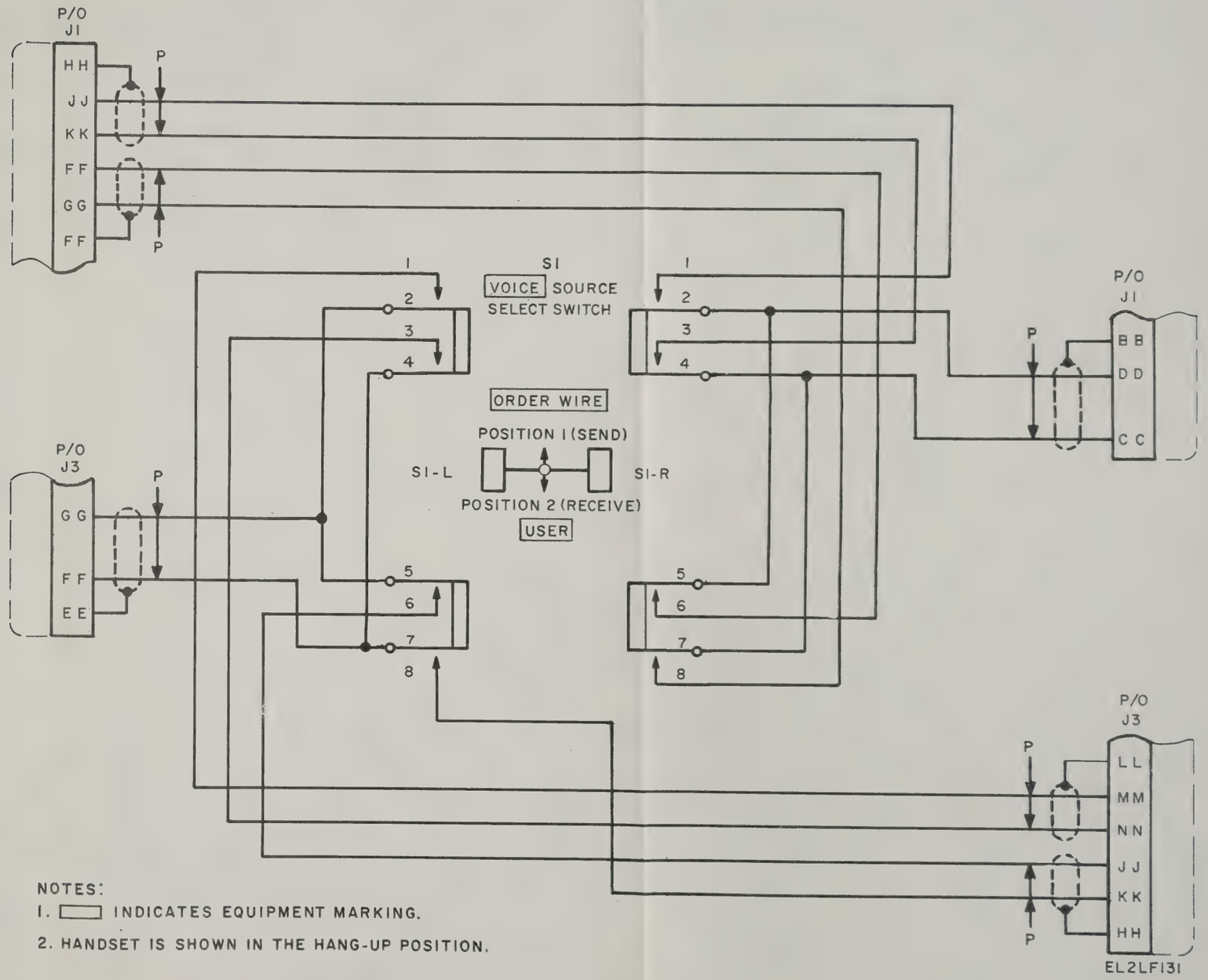
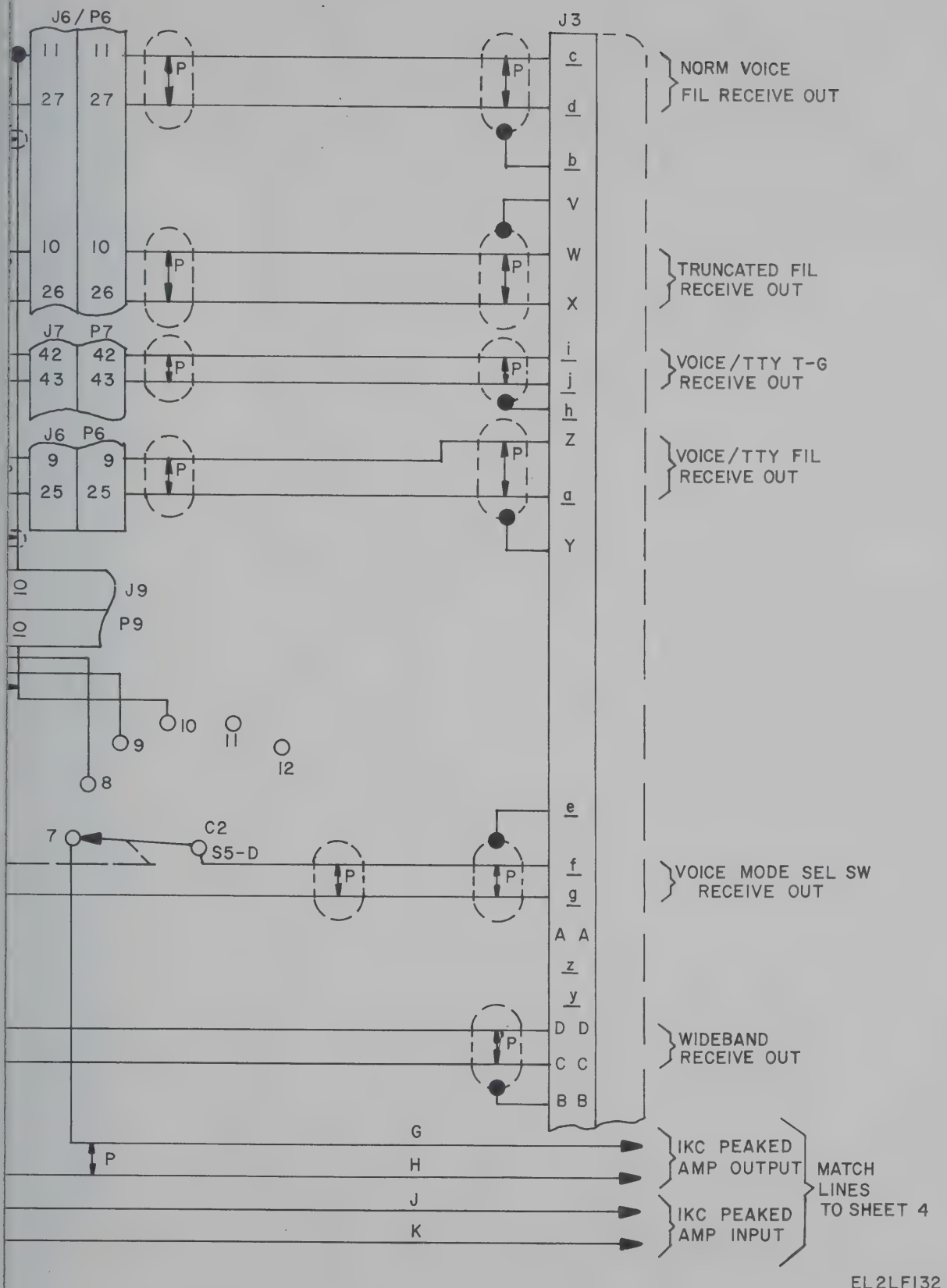
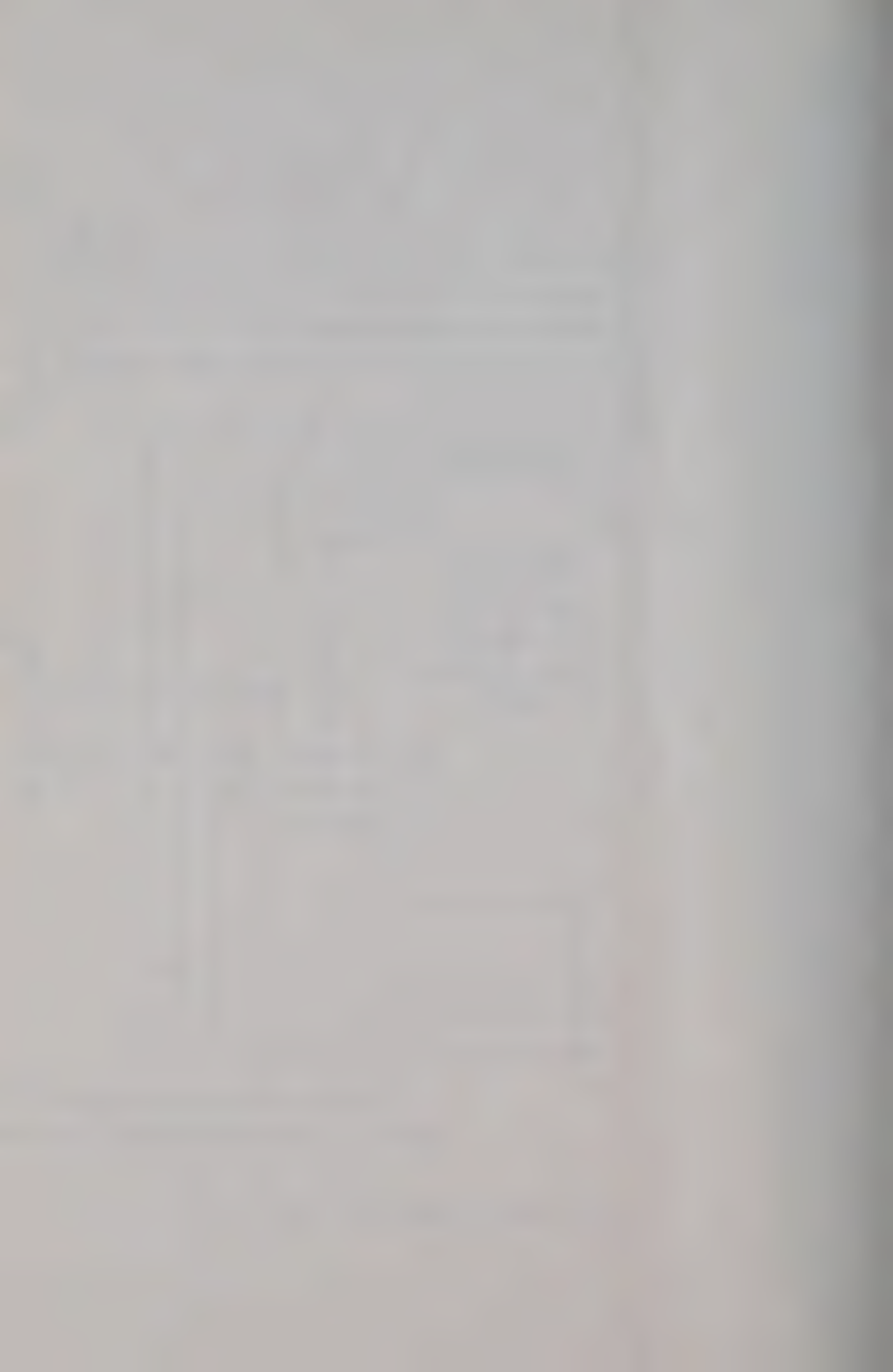


Figure FO 3-34. ①Baseband control panel 1A3A13, schematic diagram (sheet 1 of 6).


J6 / P6
J3
11
27
10
26
J7 P7
42
43
J6 P6
9
25
J9
P9
10
9
8
11
12
C2
S5-D
7
P
c
d
b
V
W
X
i
j
h
Z
a
Y
e
f
g
A A
z
y
D D
C C
B B
G
H
J
K
NORM VOICE
FIL RECEIVE OUT
TRUNCATED FIL
RECEIVE OUT
VOICE/TTY T-G
RECEIVE OUT
VOICE/TTY FIL
RECEIVE OUT
VOICE MODE SEL SW
RECEIVE OUT
WIDEBAND
RECEIVE OUT
IKC PEAKED
AMP OUTPUT
IKC PEAKED
AMP INPUT
MATCH
LINES
TO SHEET 4
EL2LF132



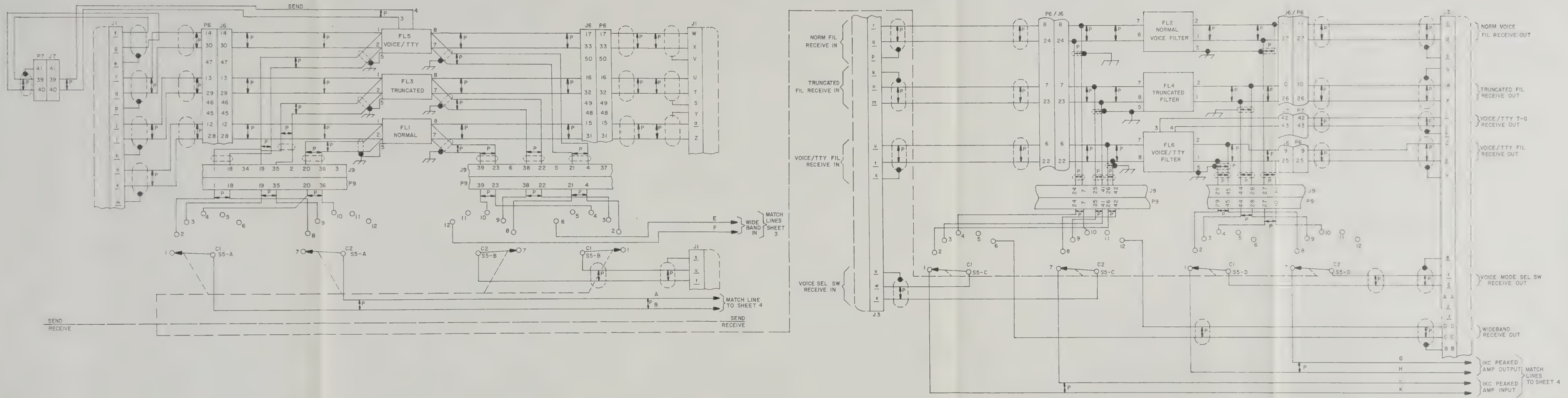
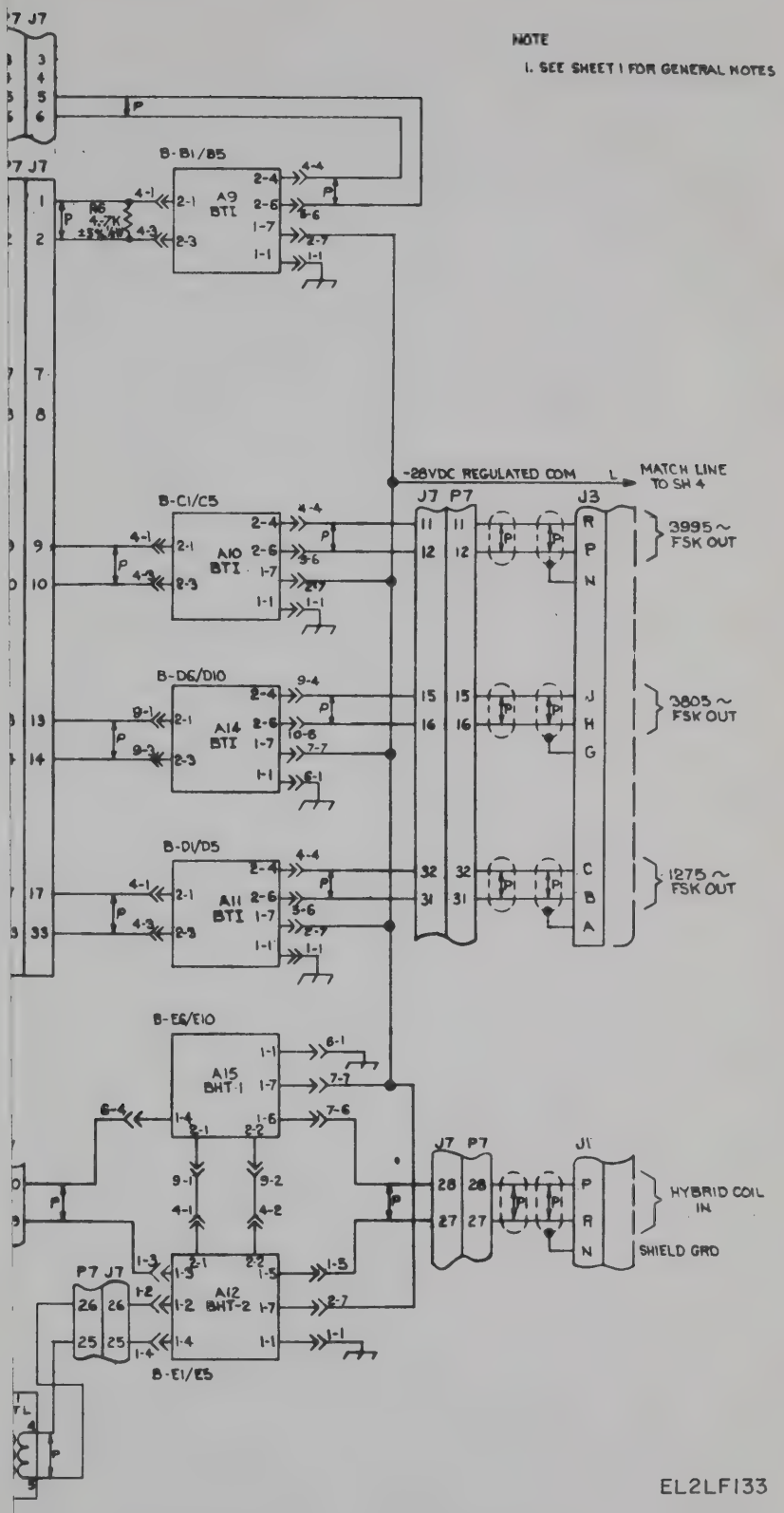


Figure FO 3-34. ①Baseband control panel 1A3A18, schematic diagram (sheet 2 of 6).



nd control panel 1A3A13, schematic diagram (sheet 3 of 6).

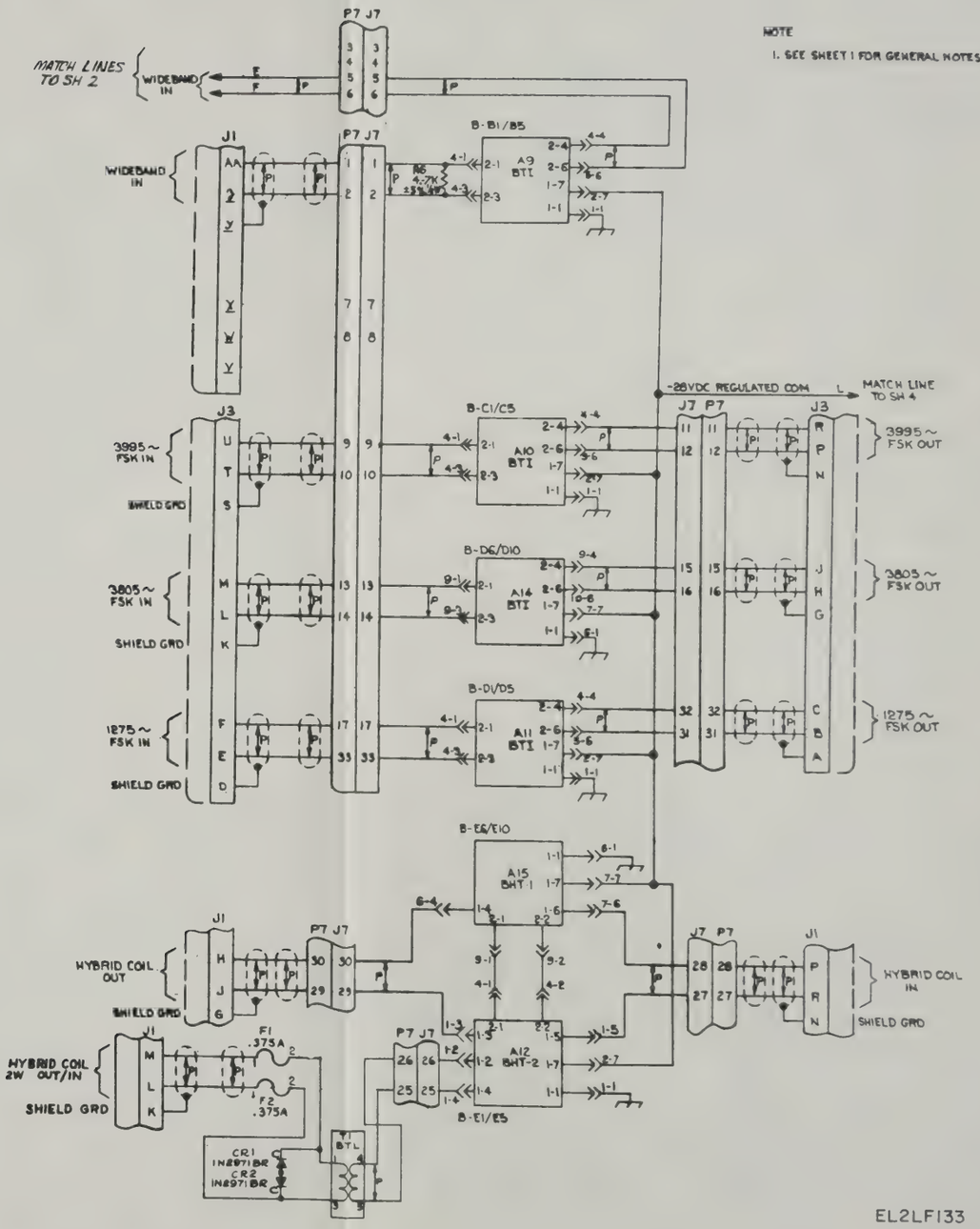
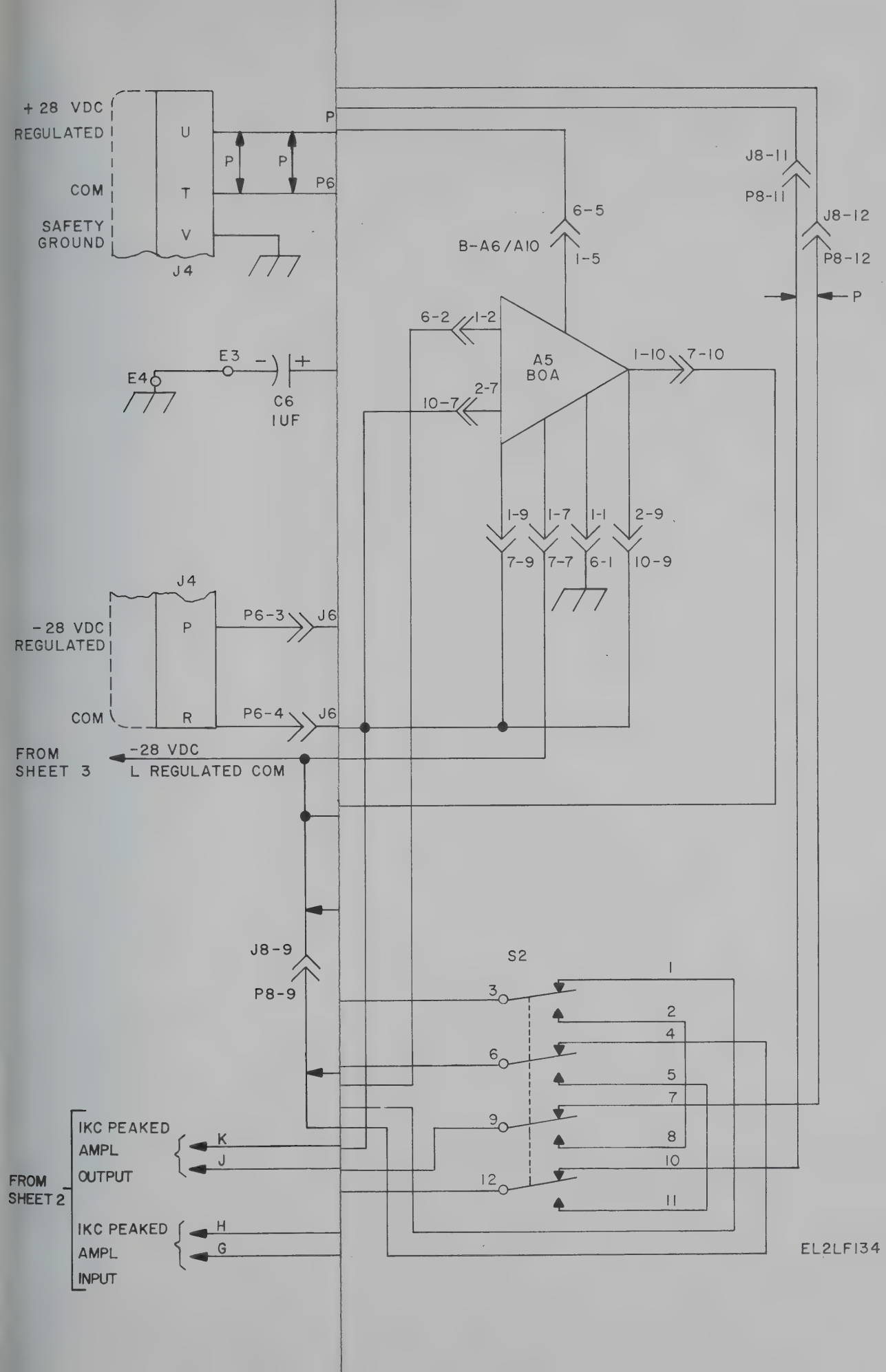


Figure FO 3-34. ③Baseband control panel 1A3A13, schematic diagram (sheet 3 of 6).


+28 VDC REGULATED
COM
SAFETY GROUND
U
T
V
J4
P
P6
P8-11
J8-11
J8-12
P8-12
6-5
B-A6/A10
1-5
6-2
1-2
A5
B0A
1-10
7-10
10-7
2-7
E3
E4
C6
1UF
1-9
1-7
1-1
2-9
7-9
7-7
6-1
10-9
-28 VDC REGULATED
P6-3
J6
P6-4
FROM SHEET 3
-28 VDC
L REGULATED COM
J8-9
P8-9
S2
IKC PEAKED AMPL OUTPUT
K
J
FROM SHEET 2
IKC PEAKED AMPL INPUT
H
G
EL2LF134

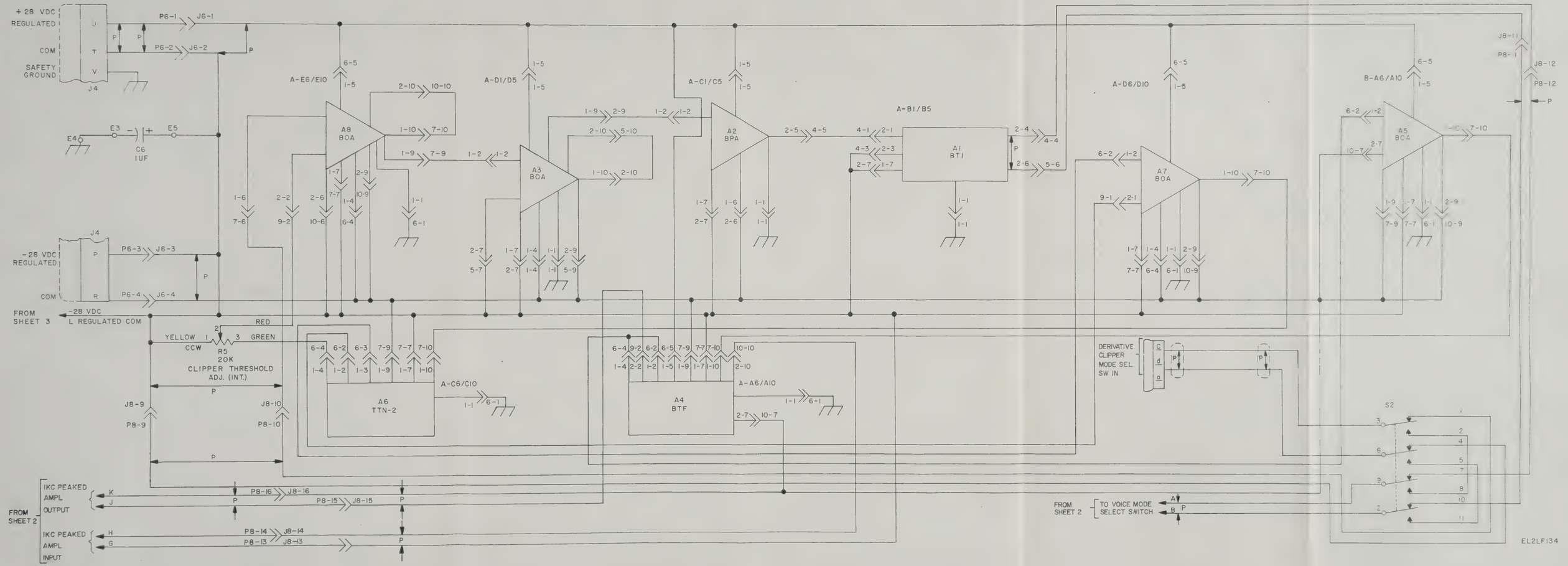
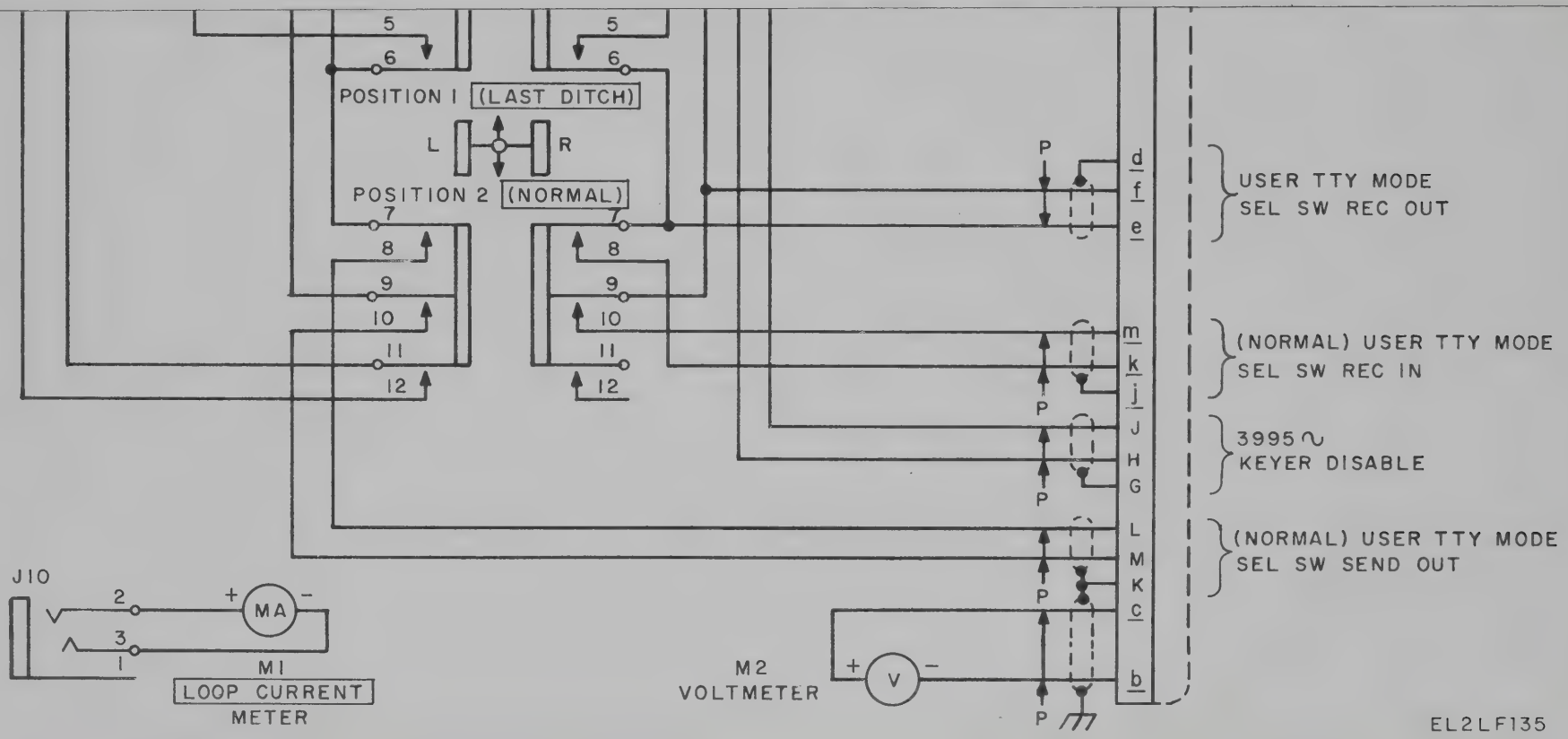


Figure FO 3-34.Ⓒ Baseband control panel 1A3A13, schematic diagram (sheet 4 of 6).

eet 5 of 6).


5
6
POSITION 1 (LAST DITCH)
L
R
POSITION 2 (NORMAL)
7
8
9
10
11
12
P
d
f
e
m
k
j
J
H
G
L
M
K
c
b
USER TTY MODE
SEL SW REC OUT
(NORMAL) USER TTY MODE
SEL SW REC IN
3995 ∿
KEYER DISABLE
(NORMAL) USER TTY MODE
SEL SW SEND OUT
J10
2
3
1
+
MA
−
M1
LOOP CURRENT
METER
M2
VOLTMETER
V
EL2LF135

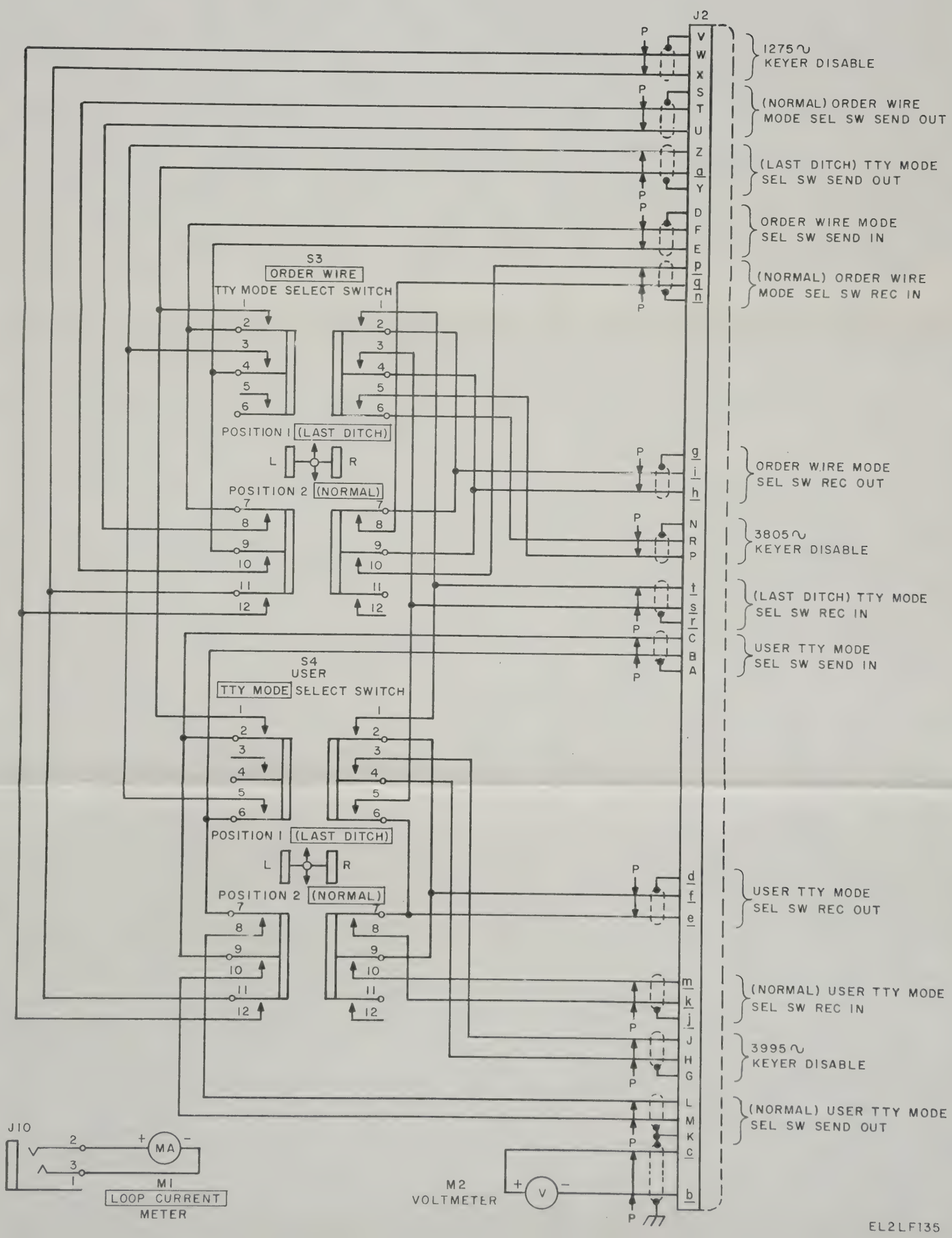
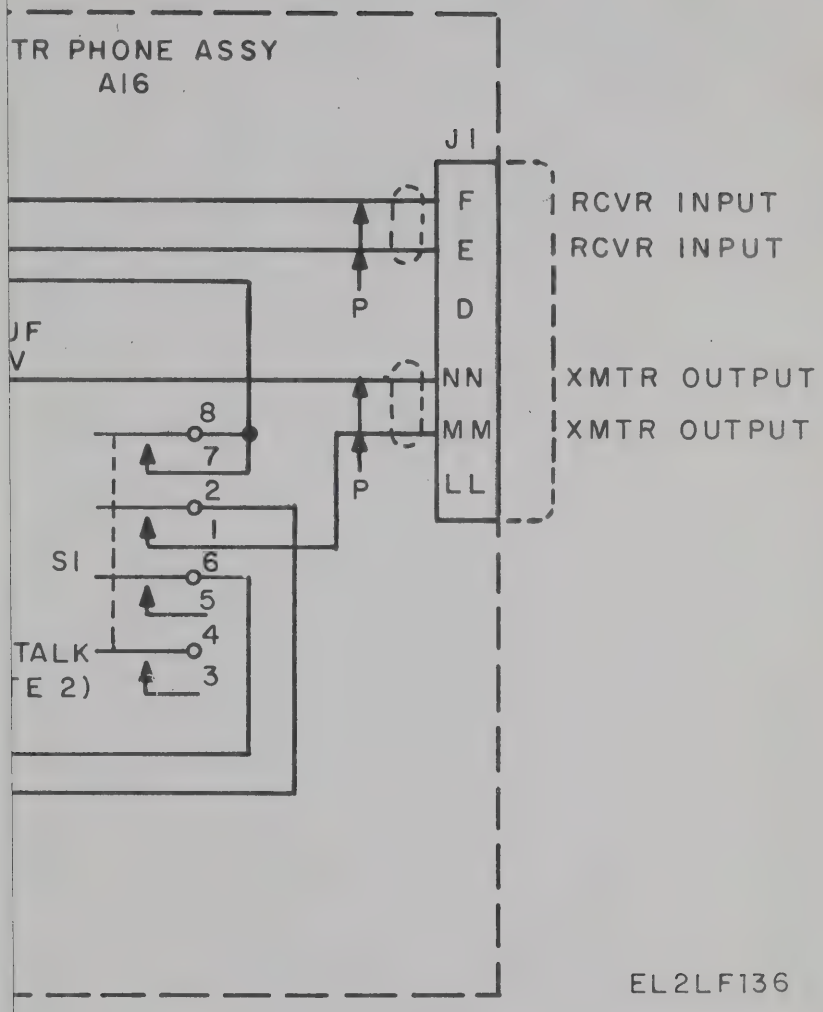


Figure FO 3-34. Baseband control panel 1A9A13, schematic diagram (sheet 5 of 6).



A13, schematic diagram (sheet 6 of 6).

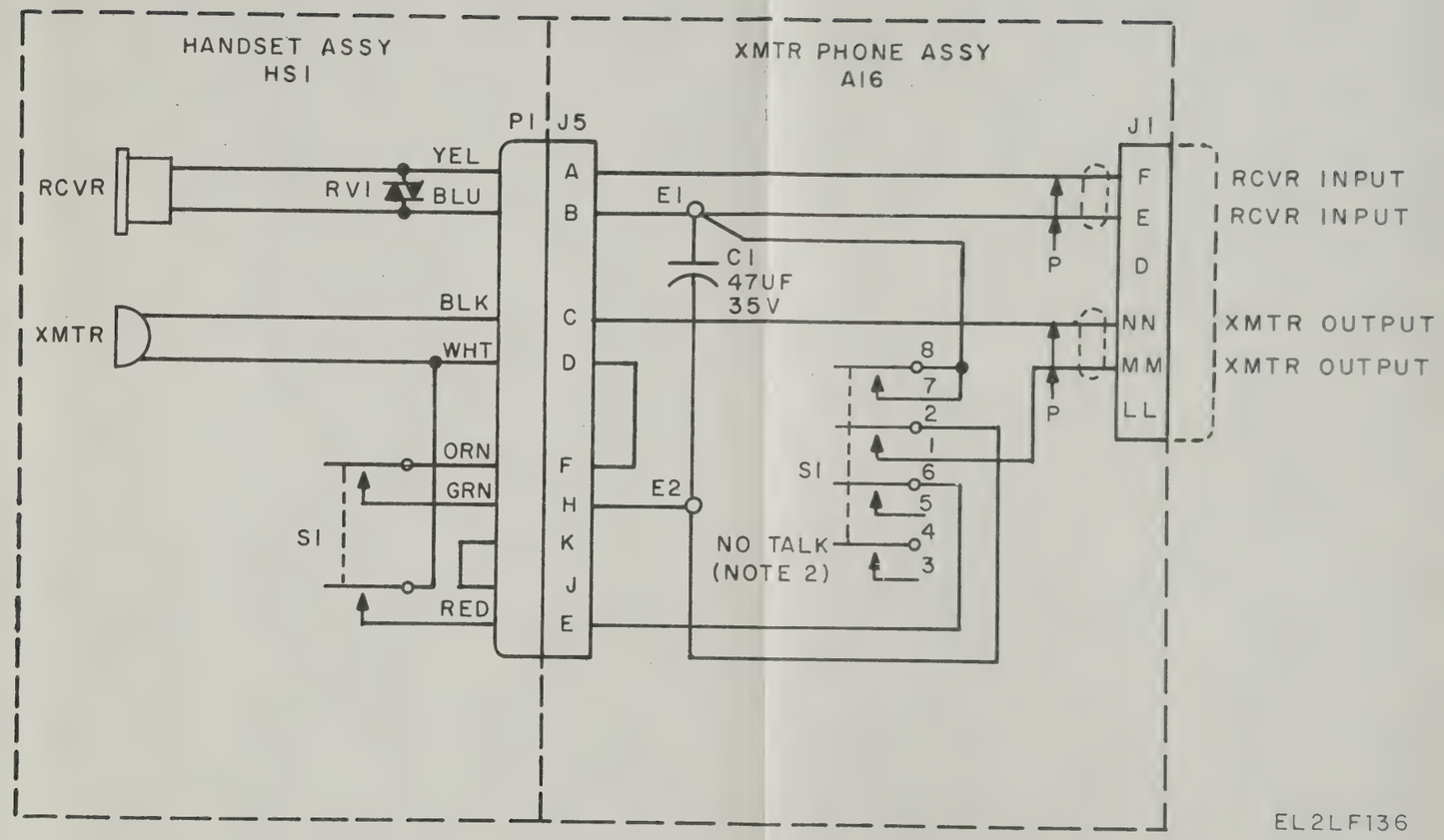
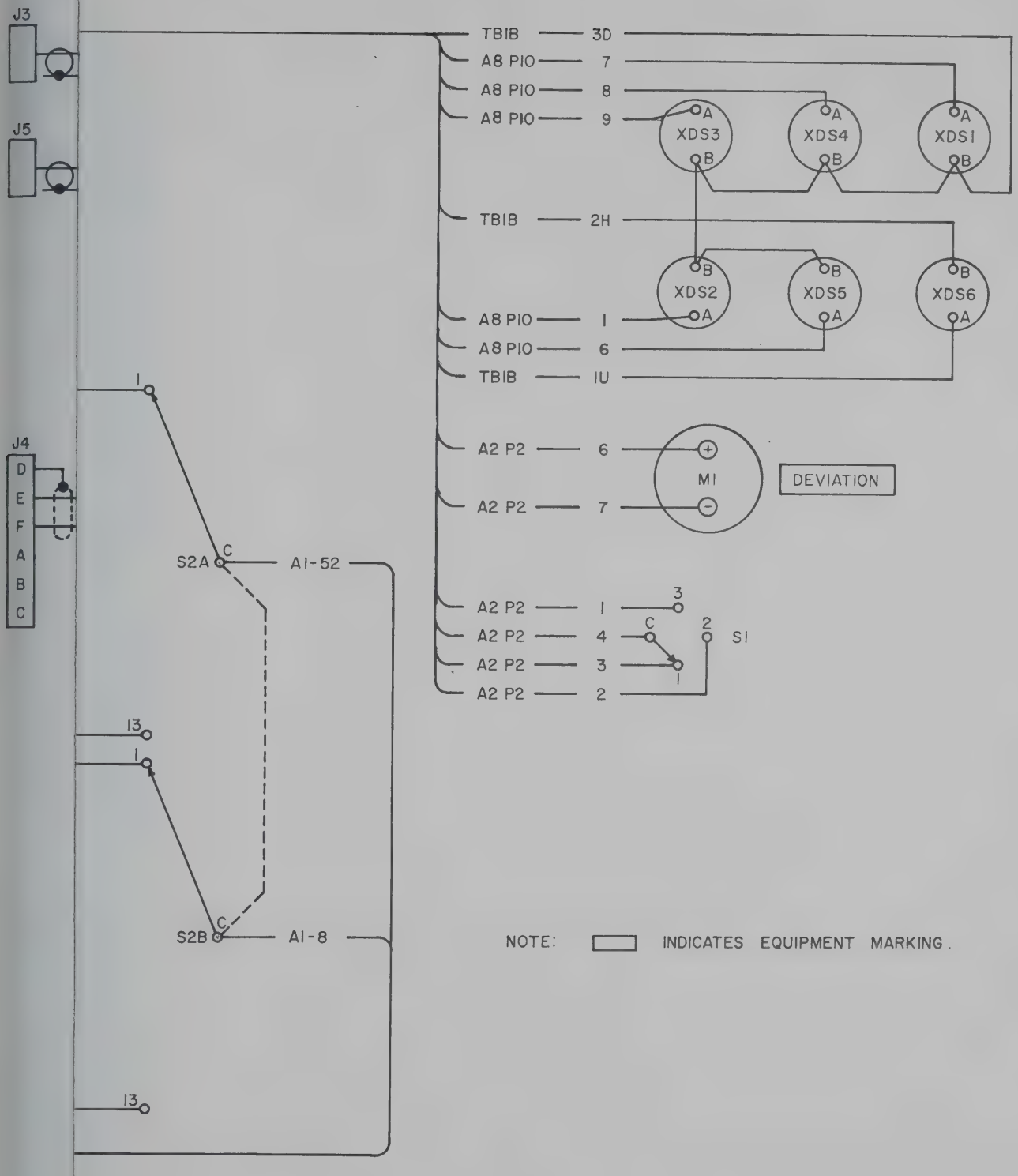


Figure FO 3-34. ⑥Baseband control panel 1A3A13, schematic diagram (sheet 6 of 6).



NOTE: ▭ INDICATES EQUIPMENT MARKING.

EL2LF142

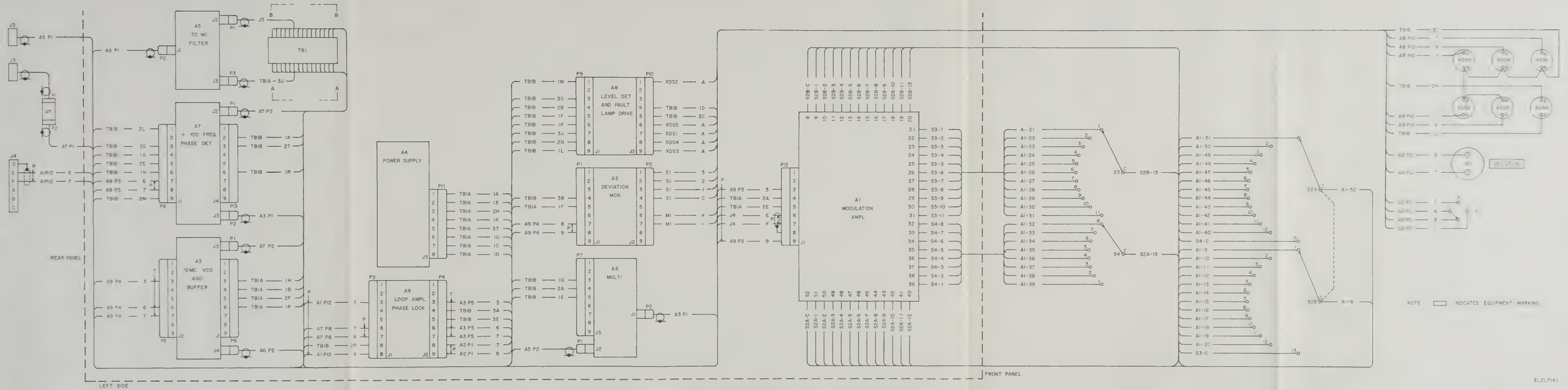
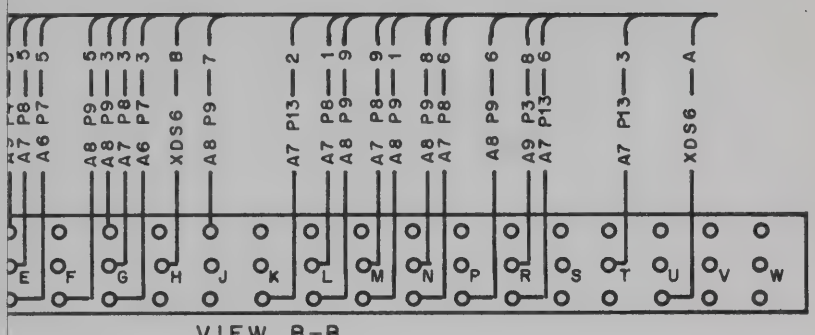
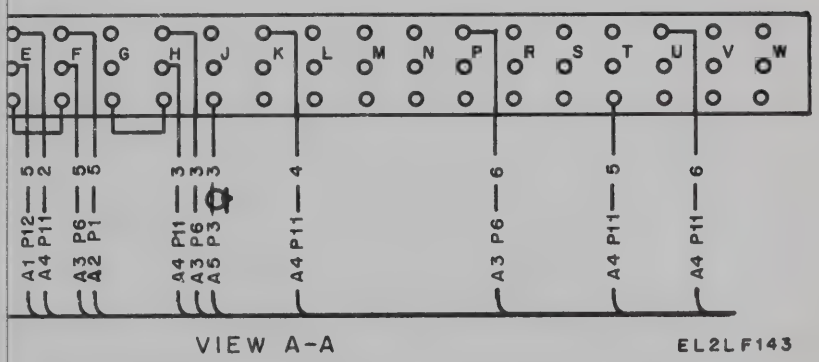


Figure FO 3-35. 1 Modulator 1A5A14, wiring diagram (sheet 1 of 2).



VIEW B-B

S OF TB1A AND TB1B ARE COMMON.
TB1A (1-2-3)A ARE COMMON WITH
-3)A.



VIEW A-A

EL2LF143

e FO 3-35.② Modulator 1A3A14, wiring diagram (sheet 2 of 2).

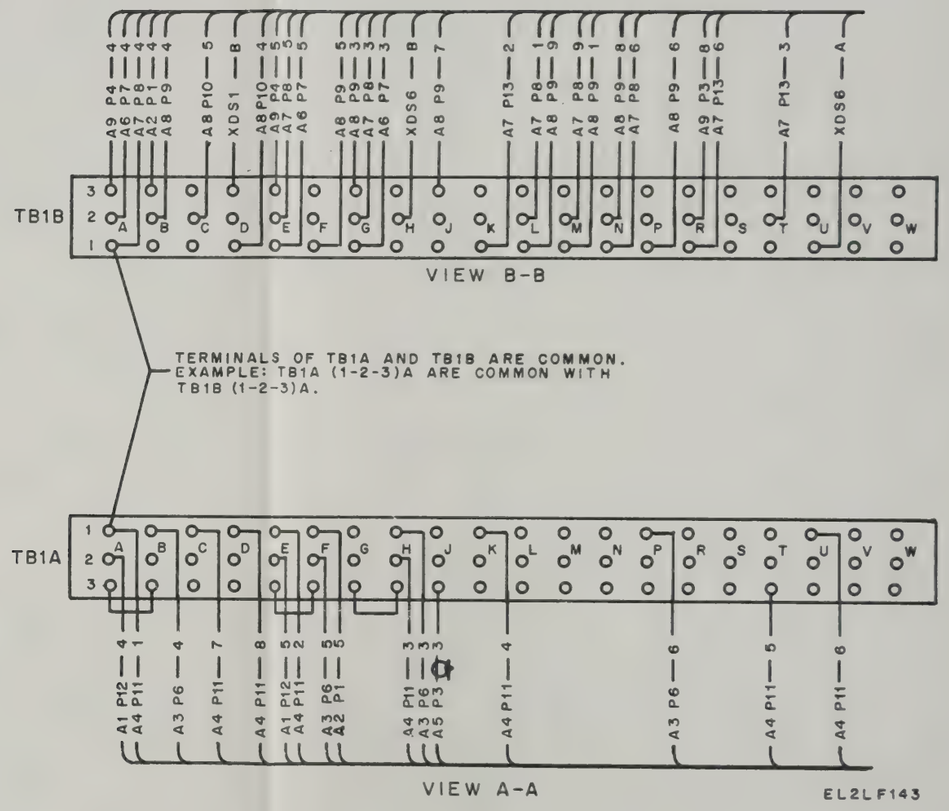
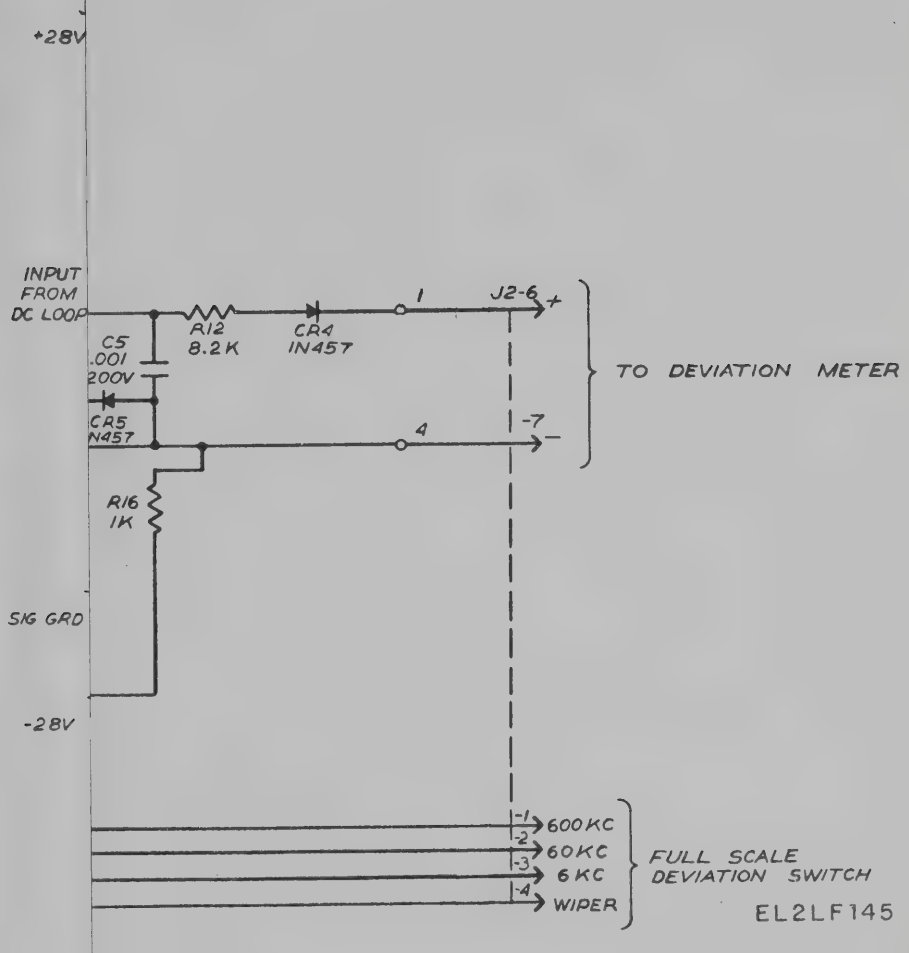


Figure FO 3-35.② Modulator 1A3A14, wiring diagram (sheet 2 of 2).


+28V
INPUT FROM DC LOOP
R12 8.2K
CR4 IN457
1
J2-6
+
C5 .001 200V
CR5 IN457
4
-7
−
TO DEVIATION METER
R16 1K
SIG GRD
-28V
-1
600KC
-2
60KC
-3
6KC
-4
WIPER
FULL SCALE DEVIATION SWITCH

EL2LF145

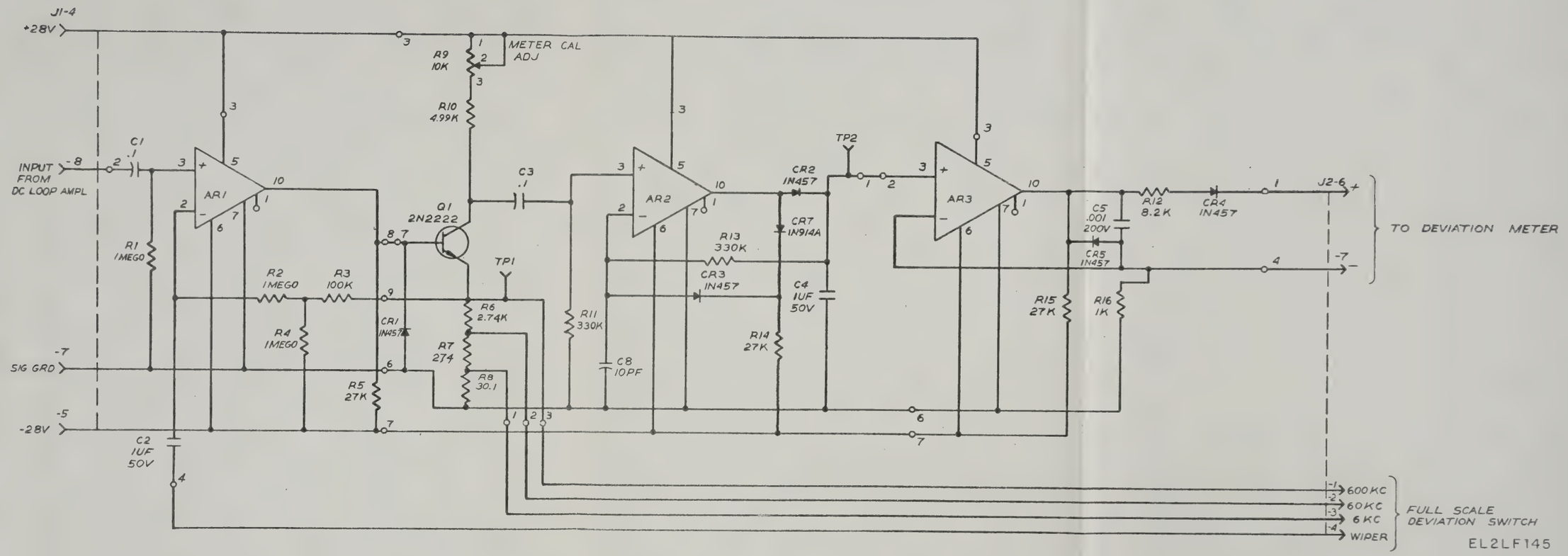
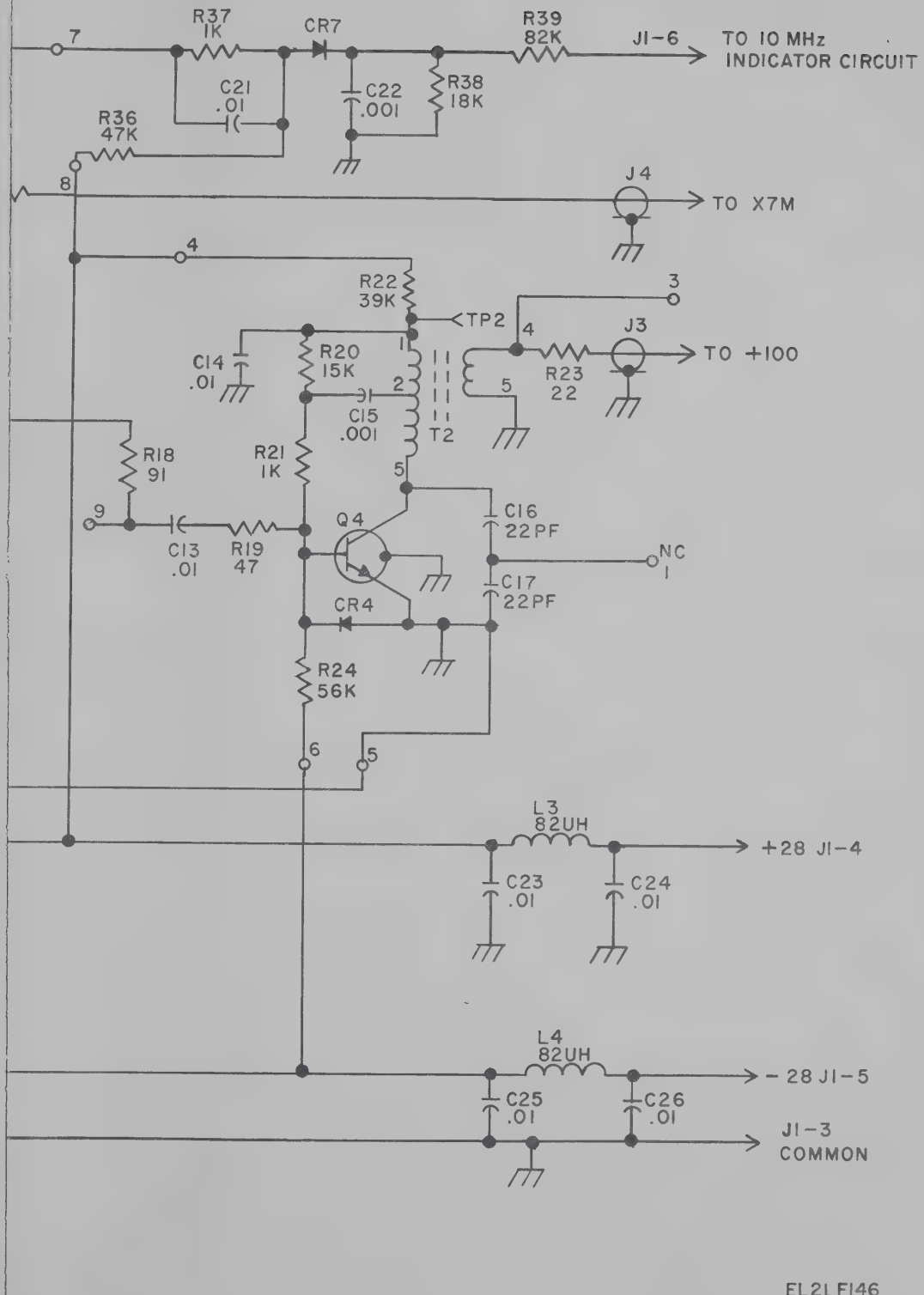


Figure FO 3-36. Deviation monitor A14A2, schematic diagram.

SPECIFIED,
RE IN OHMS.
ARE IN MICROFARADS.



EL2LF146

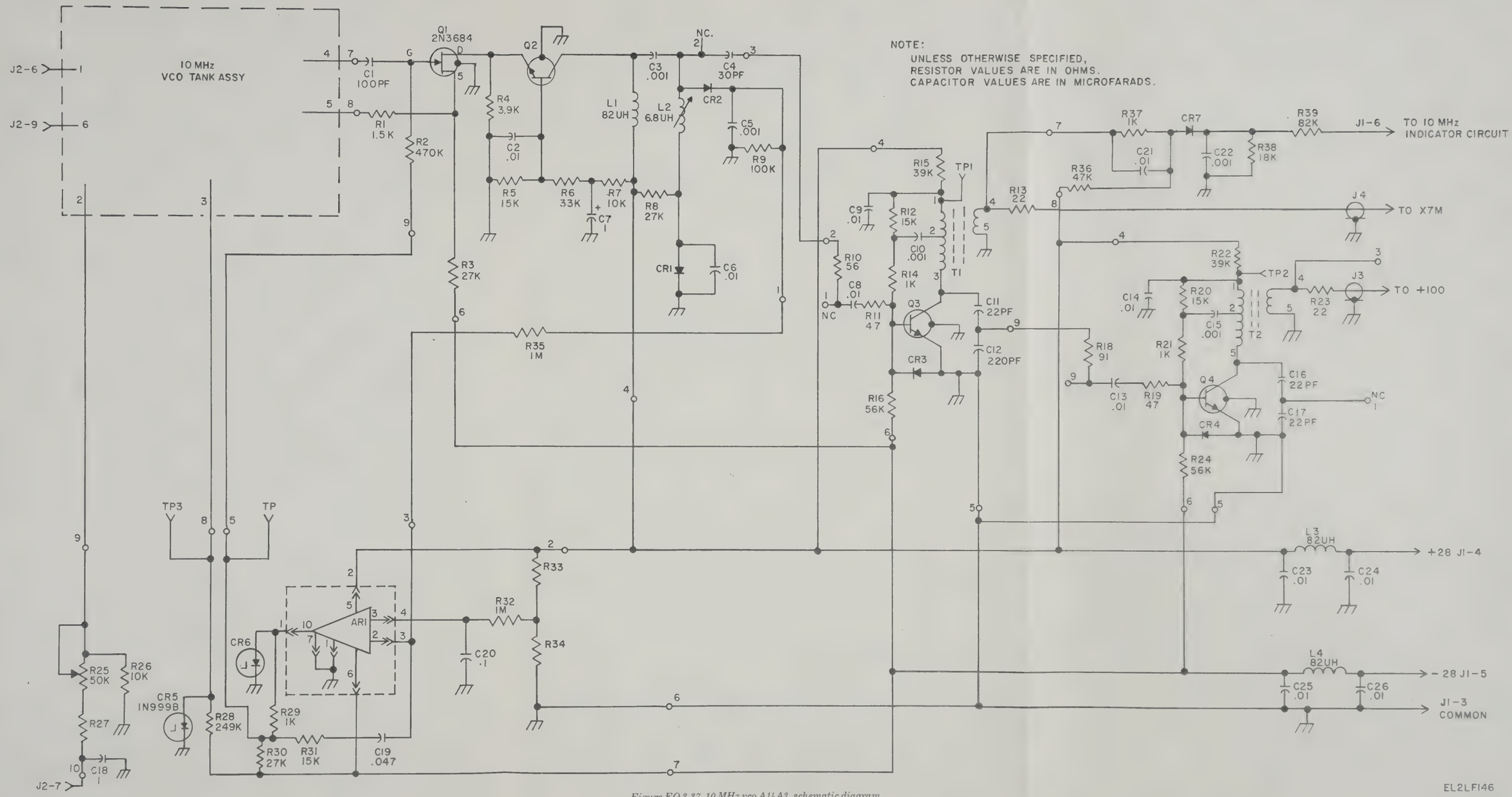
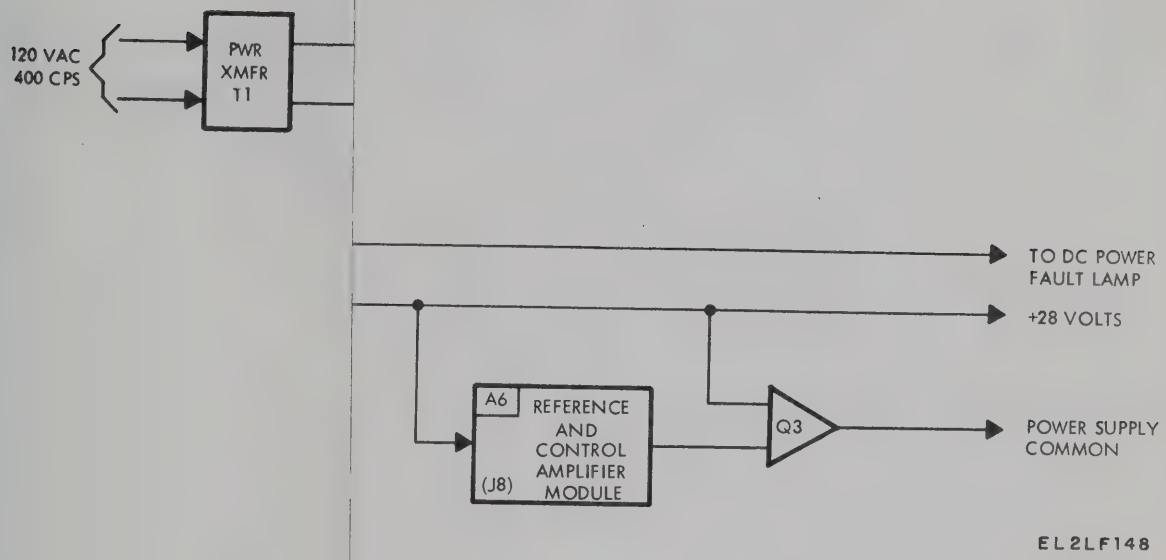


Figure FO 3-37. 10 MHz vco A14A3, schematic diagram.

EL2LF146


120 VAC
400 CPS
PWR
XMFR
T1
TO DC POWER
FAULT LAMP
+28 VOLTS
A6
REFERENCE
AND
CONTROL
AMPLIFIER
MODULE
(J8)
Q3
POWER SUPPLY
COMMON
EL2LF148

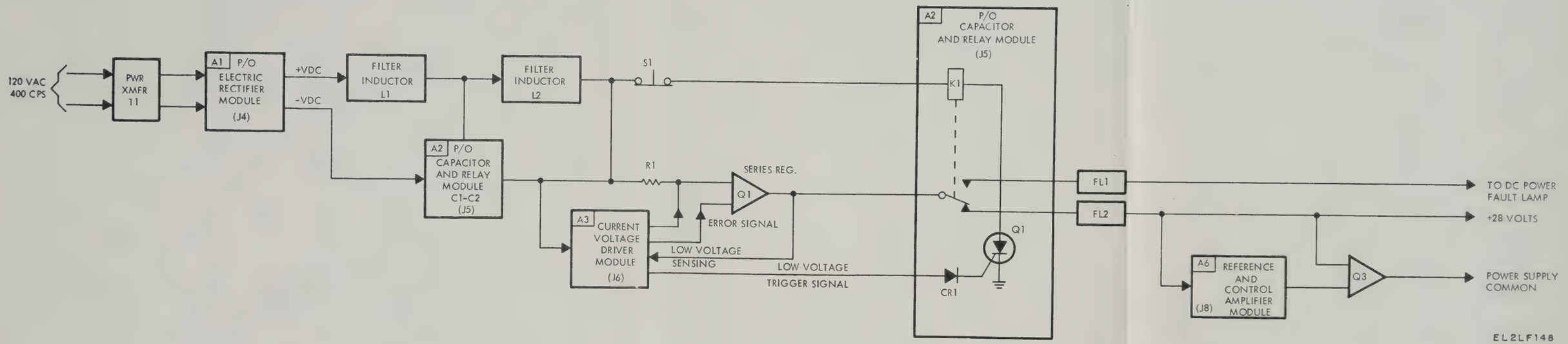
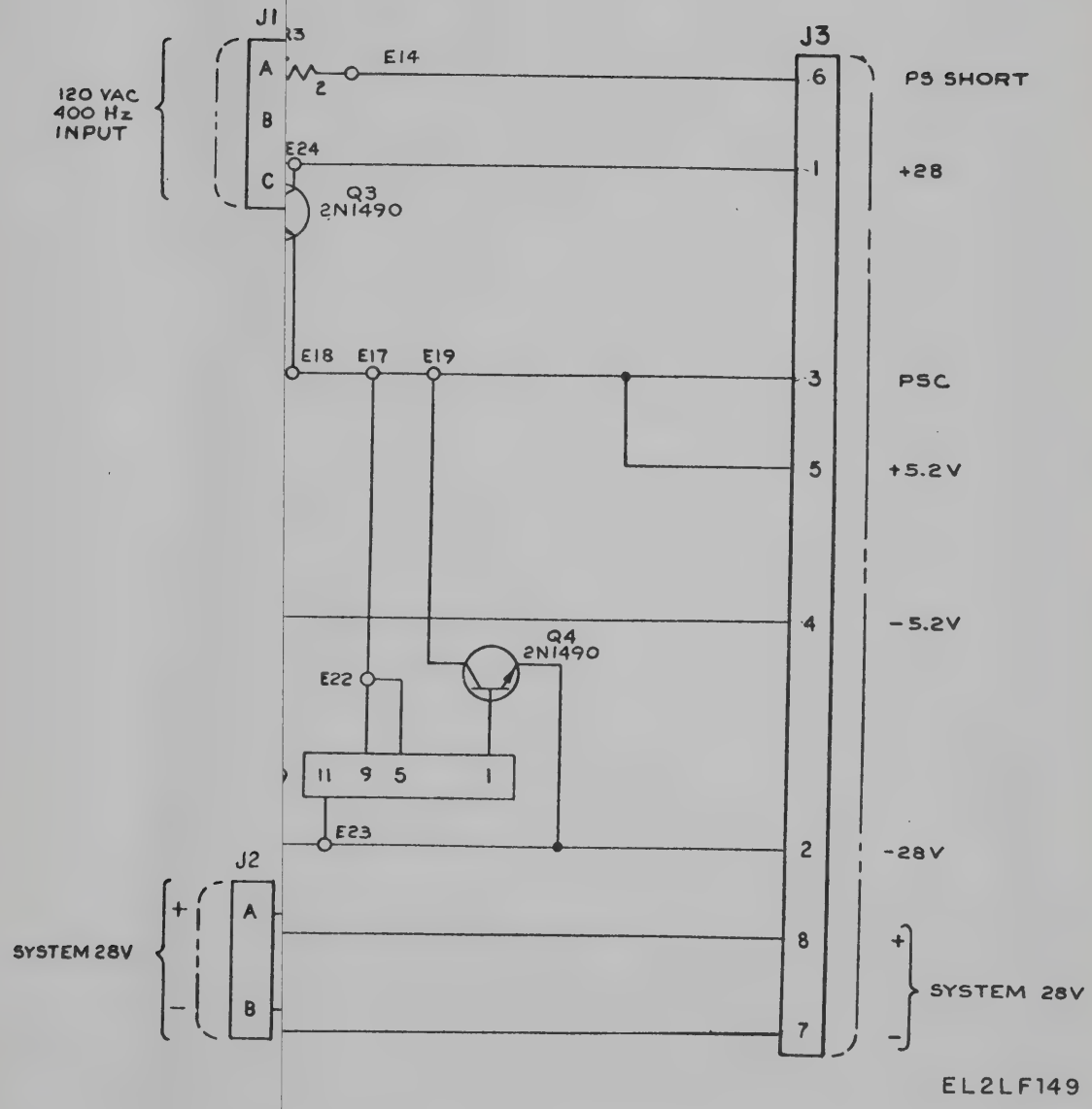


Figure FO 3-38. Power supply A4, block diagram.


J1
J3
120 VAC
400 Hz
INPUT
A
B
C
E14
E24
Q3
2N1490
E18
E17
E19
Q4
2N1490
E22
E23
11 9 5 1
J2
SYSTEM 28V
+
−
PS SHORT
+28
PSC
+5.2V
−5.2V
-28V
SYSTEM 28V
EL2LF149

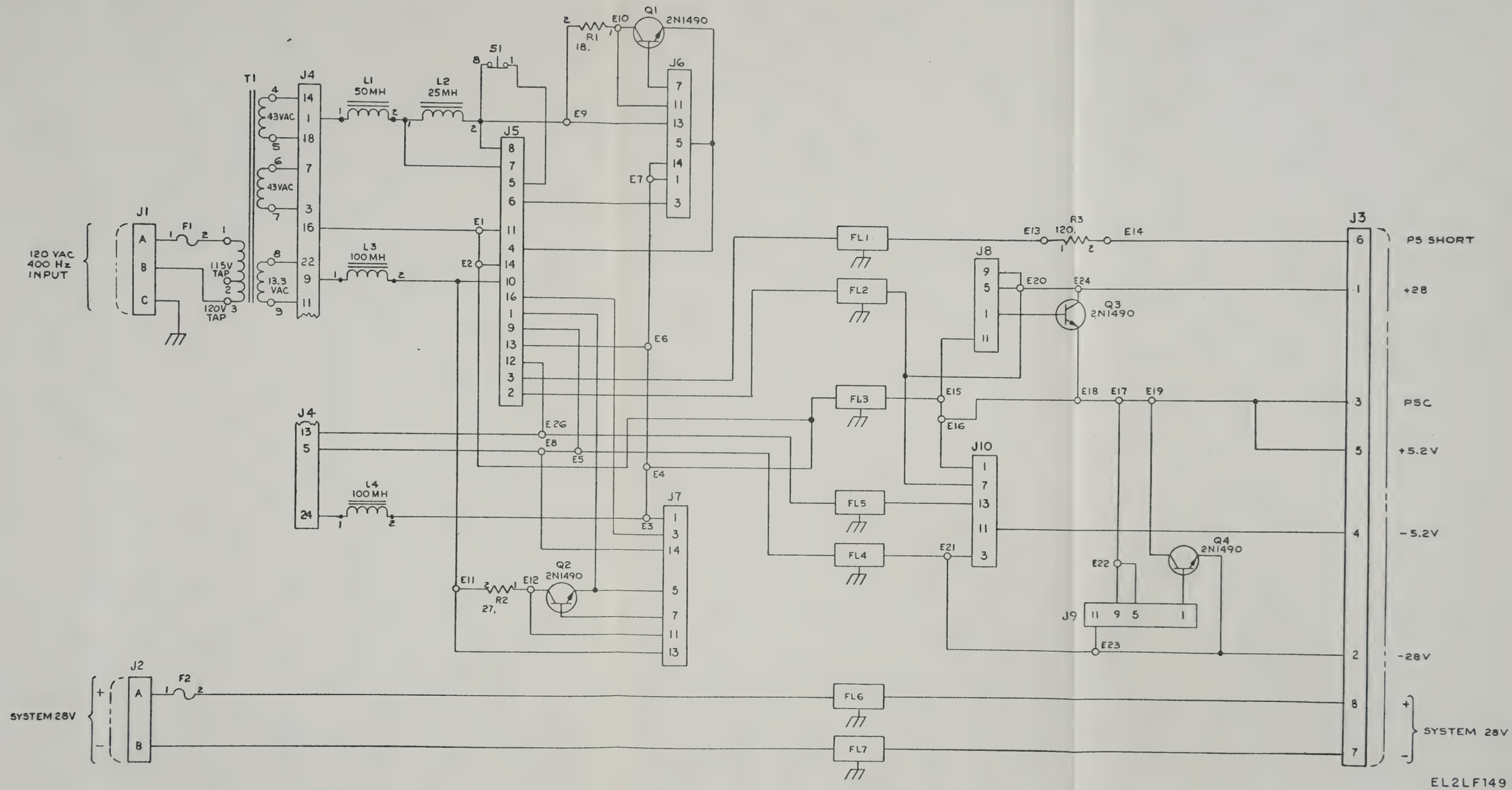
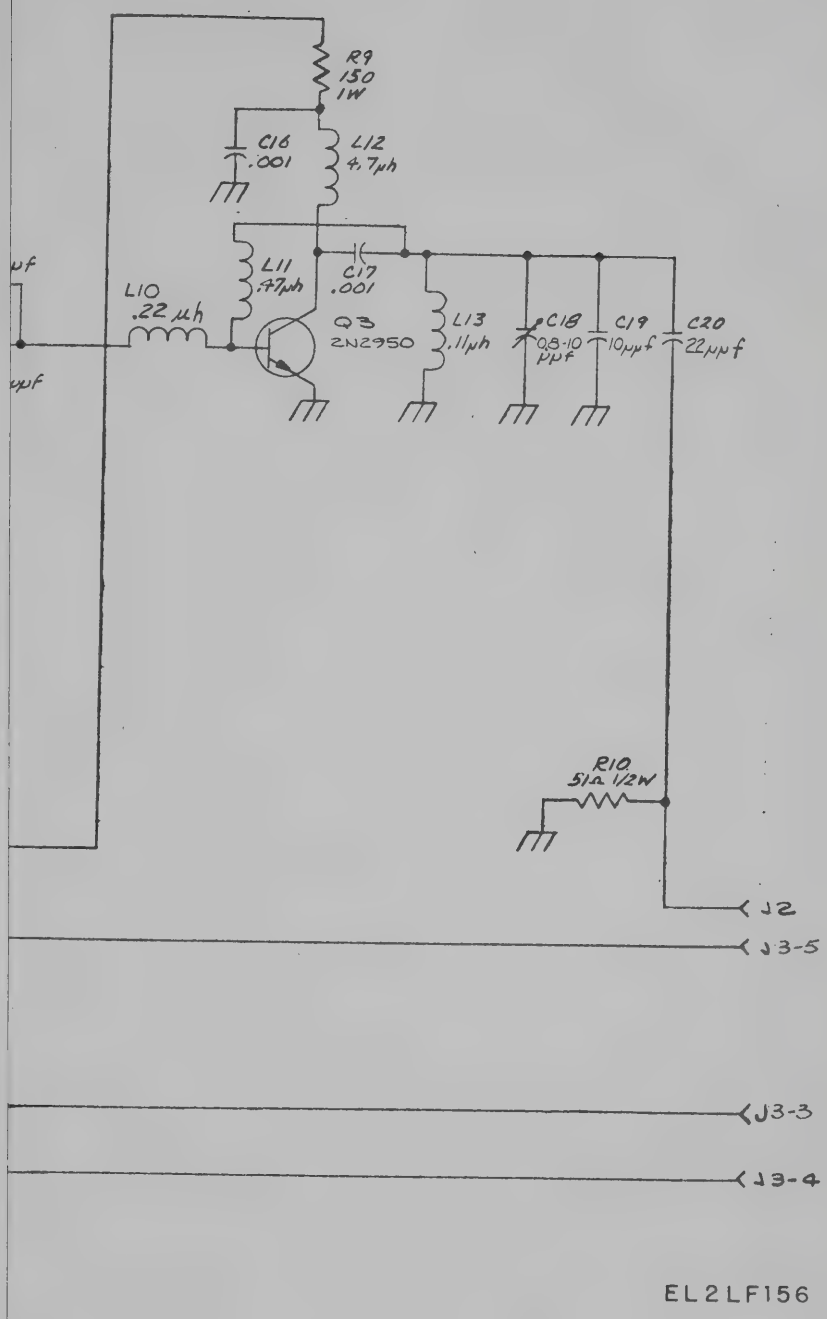


Figure FO 3-39. Power supply A4, schematic diagram.


R9
150
1W
C16
.001
L12
4.7μh
L11
.47μh
C17
.001
L10
.22 μh
Q3
2N2950
L13
.11μh
C18
0.8-10
μμf
C19
10μμf
C20
22μμf
R10
51Ω 1/2W
J2
J3-5
J3-3
J3-4

EL2LF156

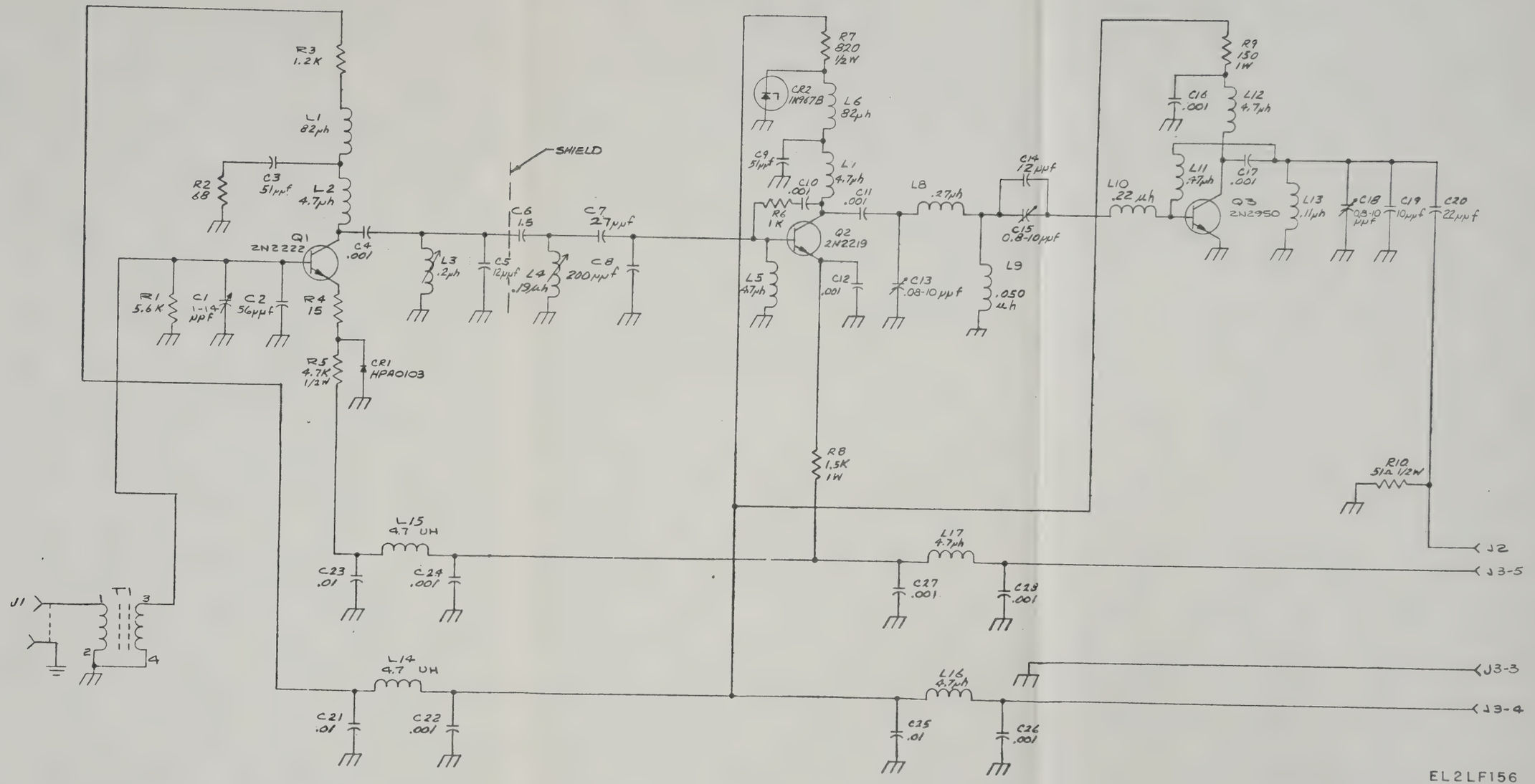
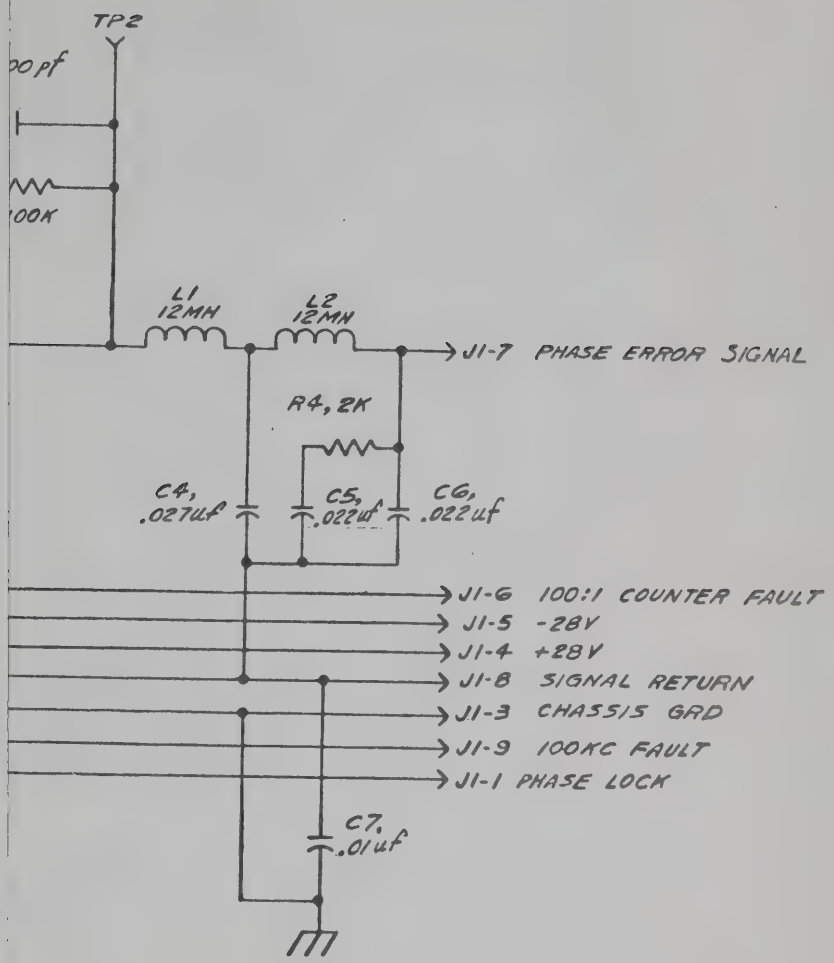
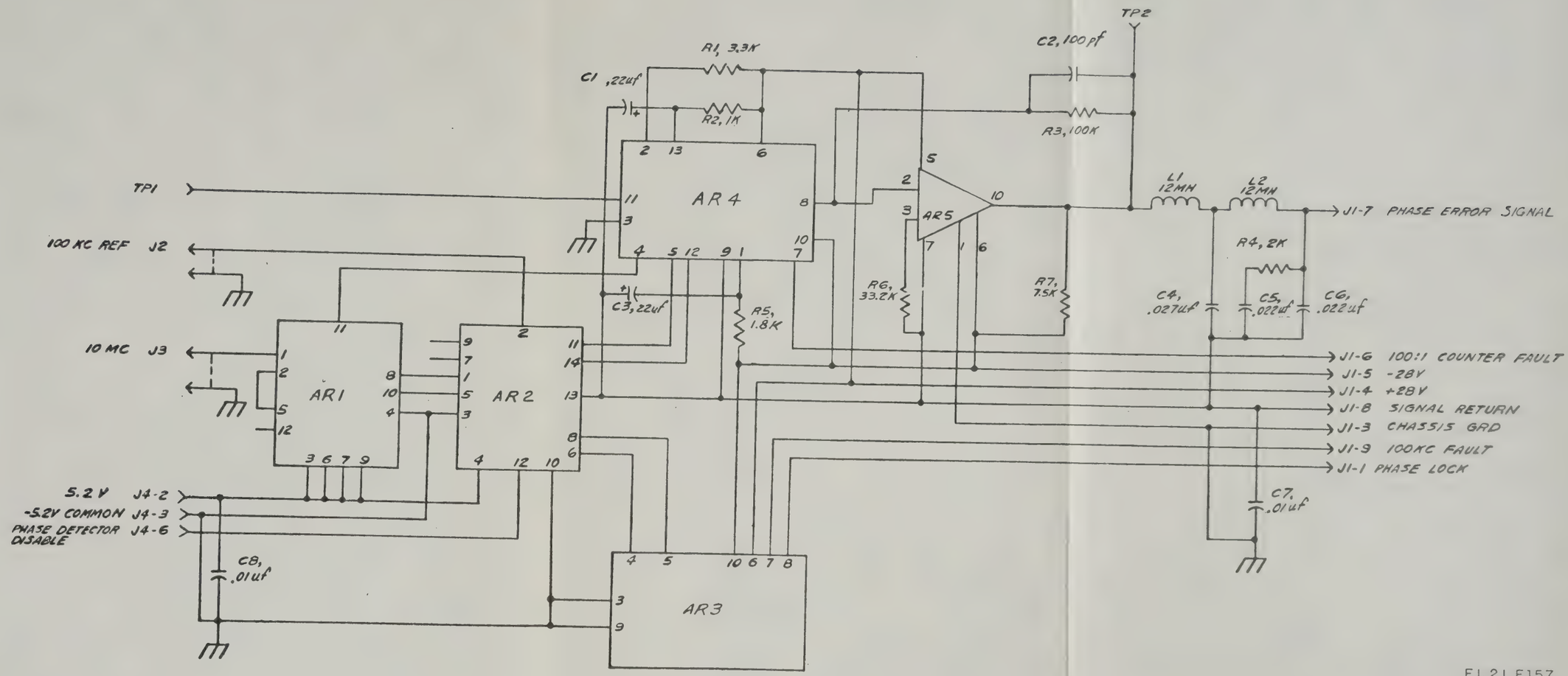


Figure FO 3-40. X7 frequency multiplier A6, schematic diagram.

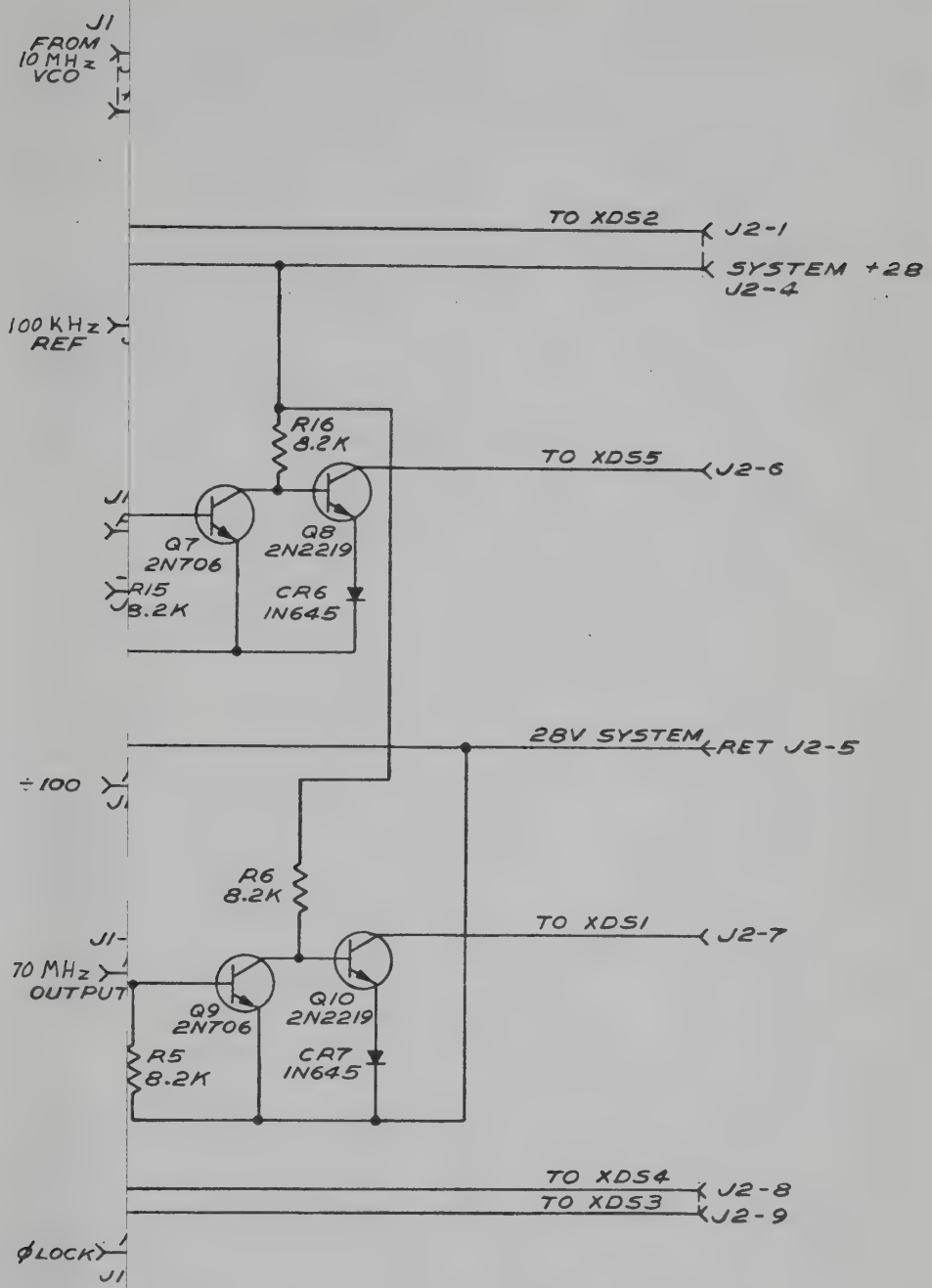

TP2
00 pf
100K
L1
12MH
L2
12MH
J1-7 PHASE ERROR SIGNAL
R4, 2K
C4,
.027uf
C5,
.022uf
C6,
.022uf
J1-6 100:1 COUNTER FAULT
J1-5 -28V
J1-4 +28V
J1-8 SIGNAL RETURN
J1-3 CHASSIS GRD
J1-9 100KC FAULT
J1-1 PHASE LOCK
C7,
.01uf

EL2LF157



EL2LF157

Figure FO 3-41. Divide by 100 frequency and phase detector circuit, schematic diagram.


J1
FROM
10 MHz
VCO
TO XDS2
J2-1
SYSTEM +28
J2-4
100 KHz
REF
R16
8.2K
TO XDS5
J2-6
Q7
2N706
Q8
2N2219
R15
8.2K
CR6
IN645
28V SYSTEM RET J2-5
÷100
R6
8.2K
TO XDS1
J2-7
J1-
70 MHz
OUTPUT
Q9
2N706
Q10
2N2219
R5
8.2K
CR7
IN645
TO XDS4
J2-8
TO XDS3
J2-9
ϕLOCK
J1

EL2LF163

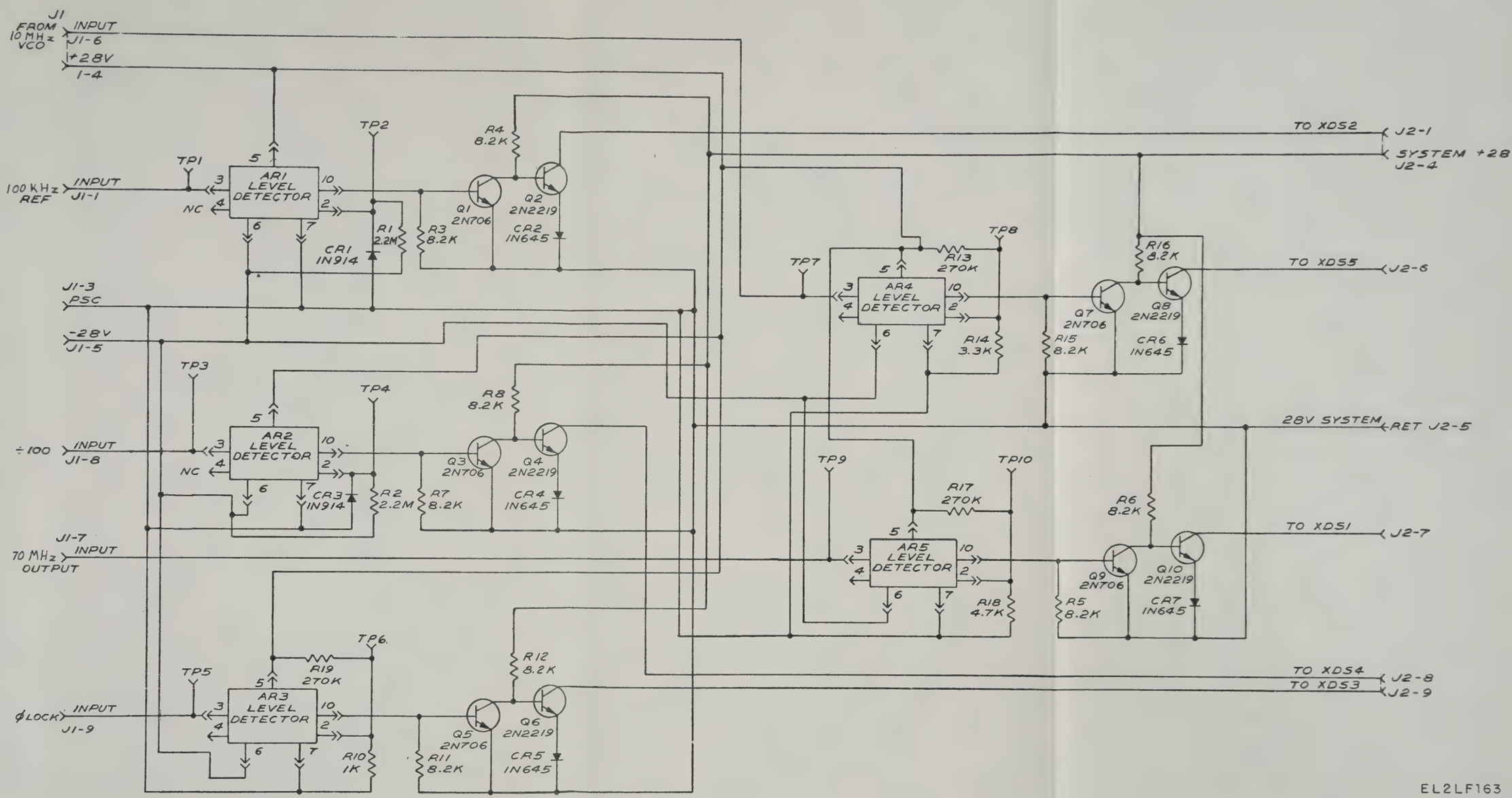
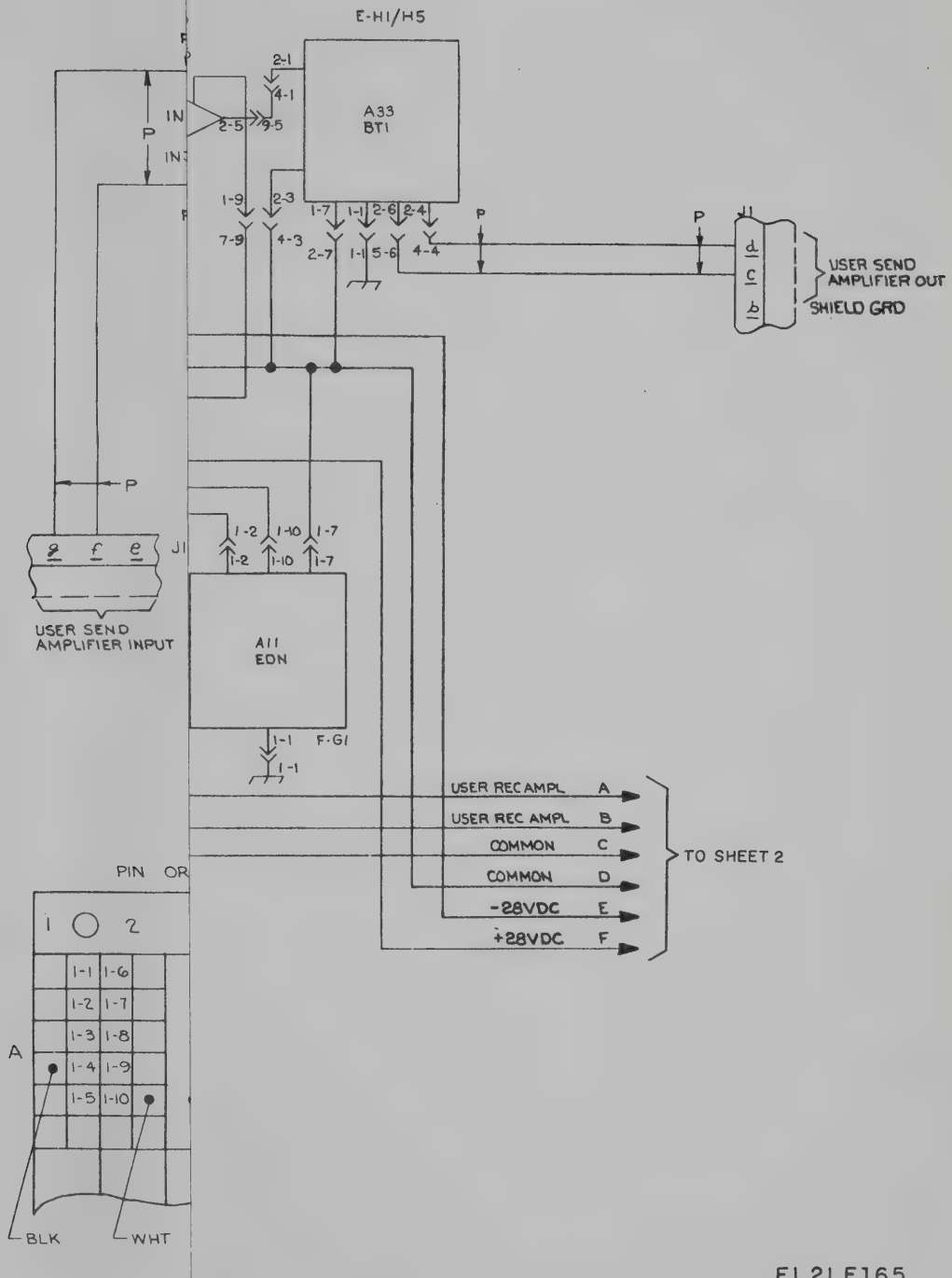


Figure FO 3-42. Level detector and fault lamp driver circuit A8, schematic diagram.

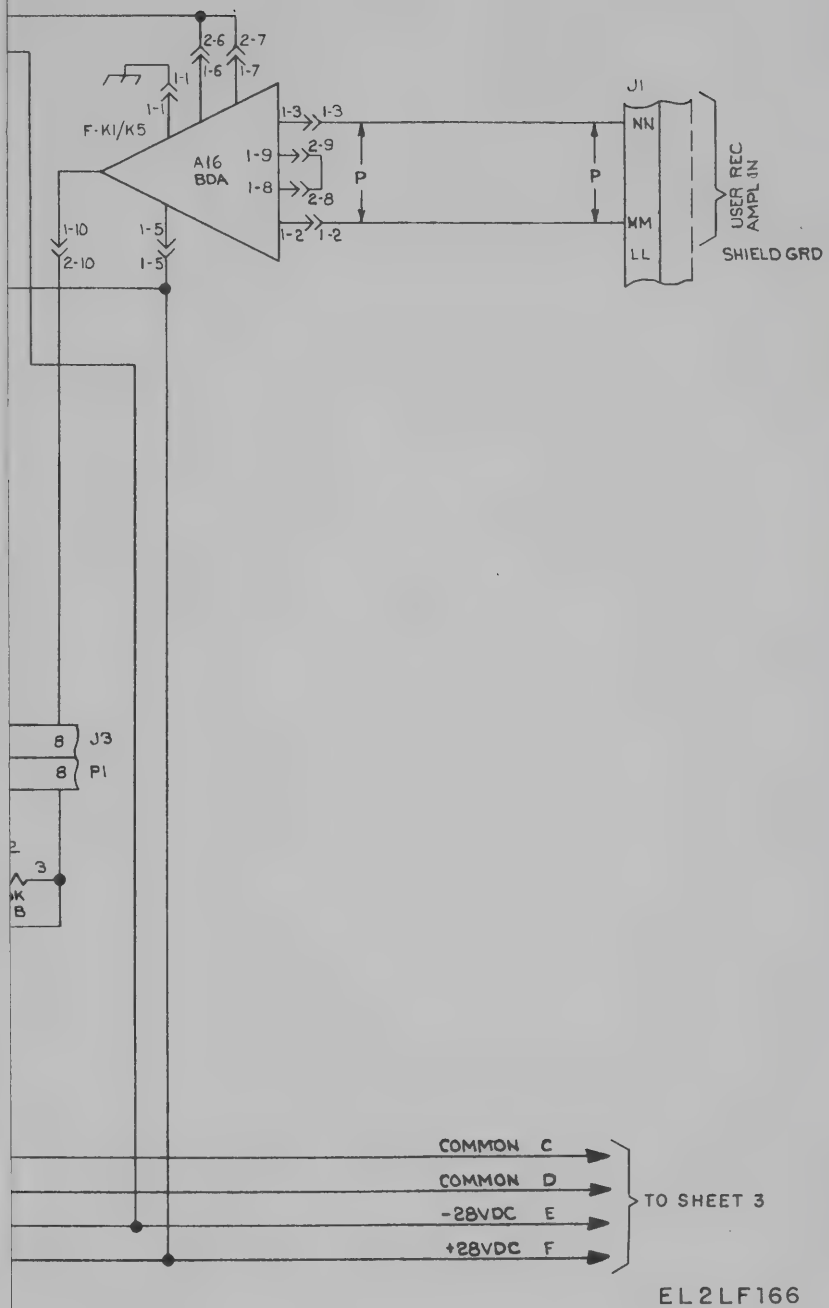

E-H1/H5
A33
BT1
2-1
4-1
2-5
9-5
IN
P
1-9
2-3
7-9
4-3
1-7
1-1
2-6
2-4
2-7
1-1
5-6
4-4
P
P
J1
USER SEND
AMPLIFIER OUT
SHIELD GRD
P
USER SEND
AMPLIFIER INPUT
J1
1-2
1-10
1-7
A11
EDN
1-1
F.G1
1-1
USER REC AMPL
A
USER REC AMPL
B
COMMON
C
COMMON
D
-28VDC
E
+28VDC
F
TO SHEET 2
PIN OR
1
2
1-1
1-6
1-2
1-7
1-3
1-8
1-4
1-9
1-5
1-10
A
BLK
WHT

EL2LF165

F1 3/8AMP
F2 3/8AMP
CR1 IN3994A
CR2 IN3994A
R35 3.9K ±5% 1/4W
T1
BTL
E7
E1
J5/P3
P1/J3
R16A
R16 10K±10% 1W LEVEL CONTROL
R16B
CCW
F-F6/F10
A17 BOA-2
F-H1/H5
A14 BOA
F-H6/H10
A19 BPA
E-H1/H5
A33 BT1
J1
USER SEND AMPLIFIER OUT
SHIELD GRD
R1 20K±5%,3/4W METER CALIBRATE
R2 20K±5%,3/4W METER CALIBRATE
GRN
YEL
RED
P2/J4
USER SEND AMPLIFIER INPUT
VU M1
A13 MCN
A18 BOA
F-G6/G10
F-G5
A11 EDN
F-G1
S1 METER SELECT
USER REC AMPL A
USER REC AMPL B
COMMON C
COMMON D
-28VDC E
+28VDC F
TO SHEET 2
PIN ORIENTATION
BLK
WHT
BLK
WHT
BLK

EL2LF165

Figure FO 3-43. (C) Baseband amplifier 1A3A15, schematic diagram (sheet 1 of 8).


2-6
2-7
1-6
1-7
1-1
1-1
F-K1/K5
A16
BDA
1-3
1-3
1-9
2-9
1-8
2-8
1-2
1-2
P
P
J1
NN
MM
LL
USER REC
AMPL IN
SHIELD GRD
1-10
2-10
1-5
1-5
8
J3
8
P1
3
COMMON C
COMMON D
-28VDC E
+28VDC F
TO SHEET 3

EL2LF166

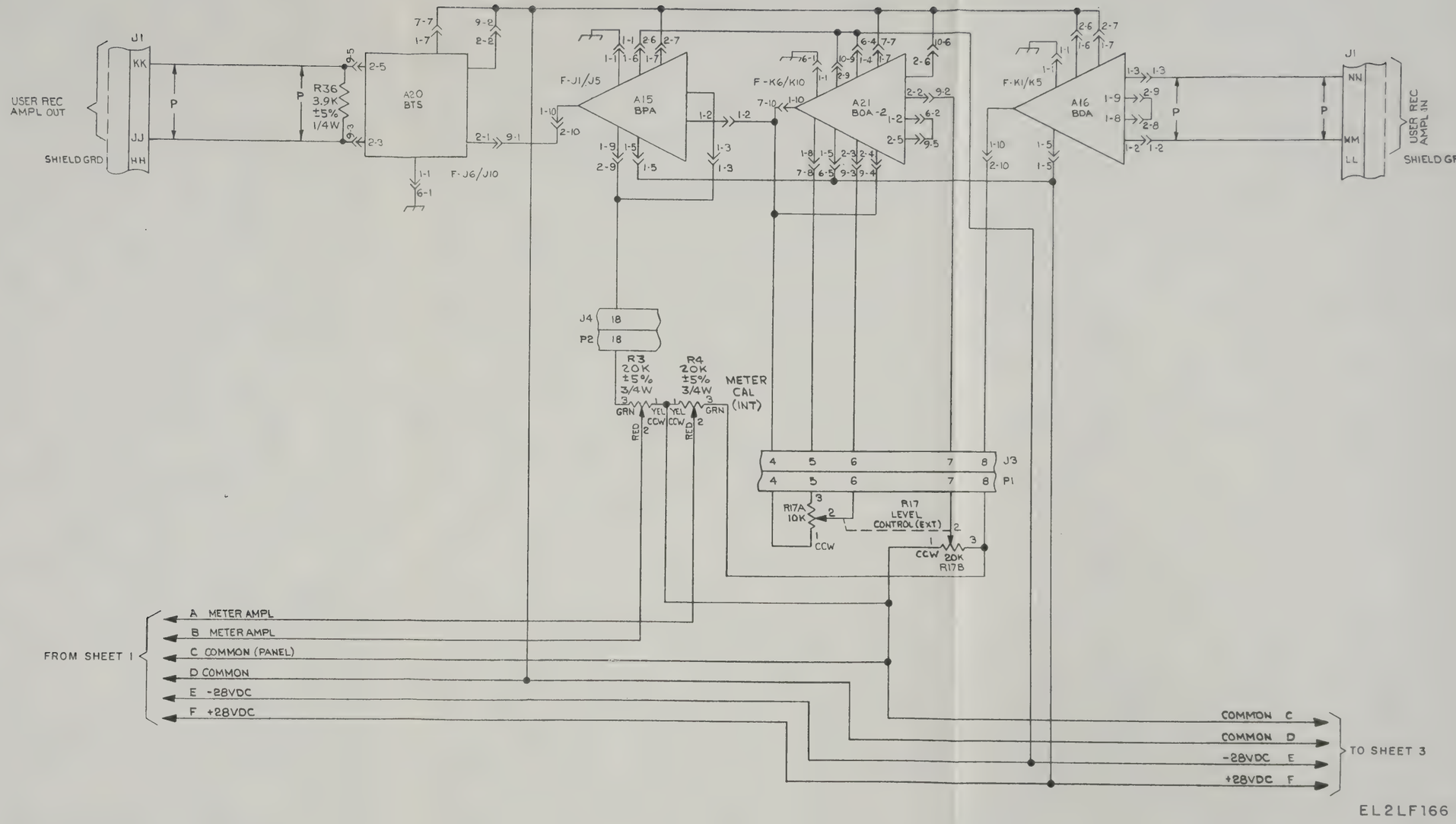
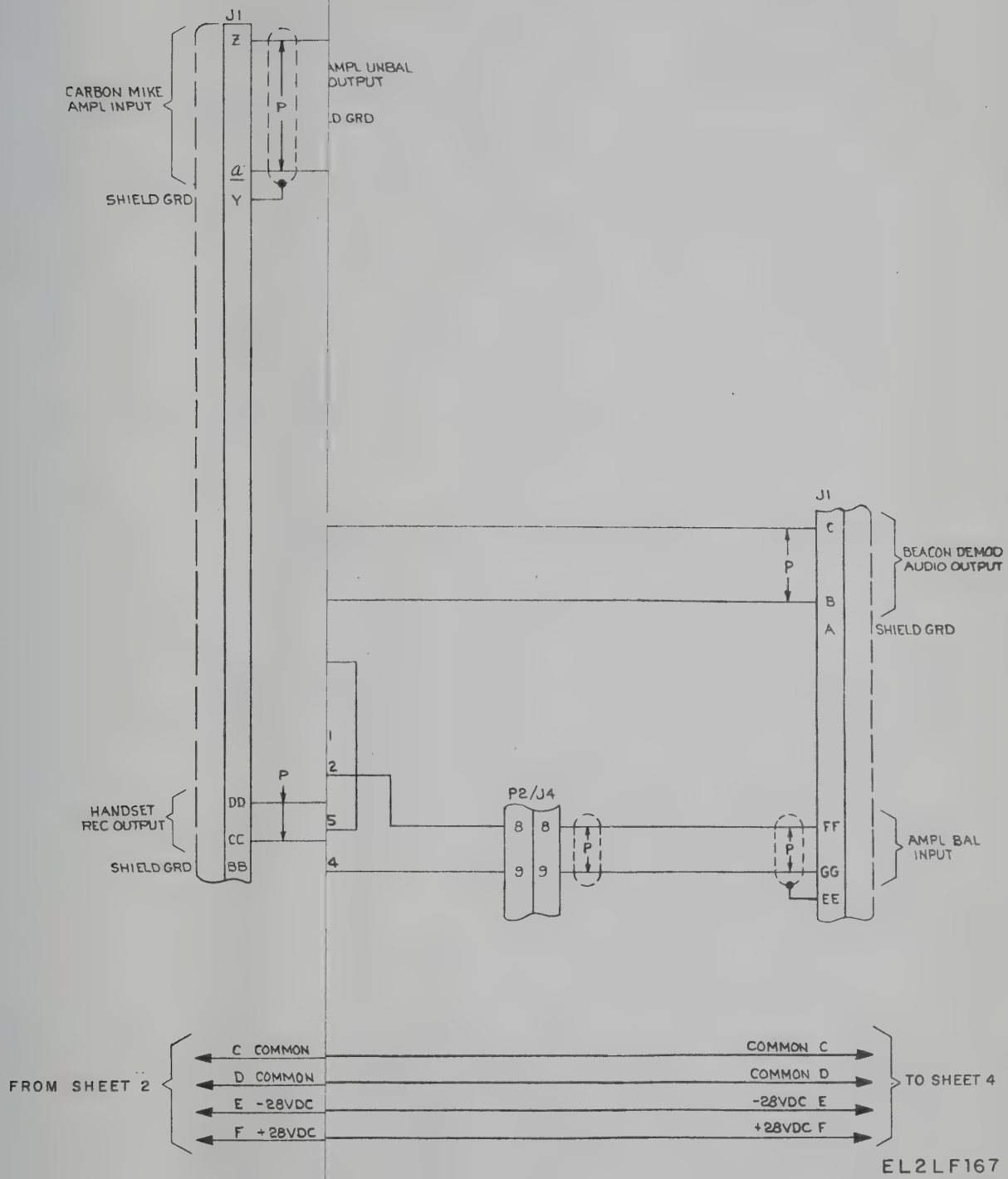


Figure FO 3-43.②Baseband amplifier 1A3A15, schematic diagram (sheet 2 of 8).


J1
Z
a
Y
CARBON MIKE AMPL INPUT
SHIELD GRD
P
AMPL UNBAL OUTPUT
LD GRD
J1
C
B
A
BEACON DEMOD AUDIO OUTPUT
SHIELD GRD
P
1
2
5
4
P
HANDSET REC OUTPUT
SHIELD GRD
DD
CC
BB
P2/J4
8
8
9
9
P
P
FF
GG
EE
AMPL BAL INPUT
FROM SHEET 2
C COMMON
D COMMON
E -28VDC
F +28VDC
COMMON C
COMMON D
-28VDC E
+28VDC F
TO SHEET 4

EL2LF167

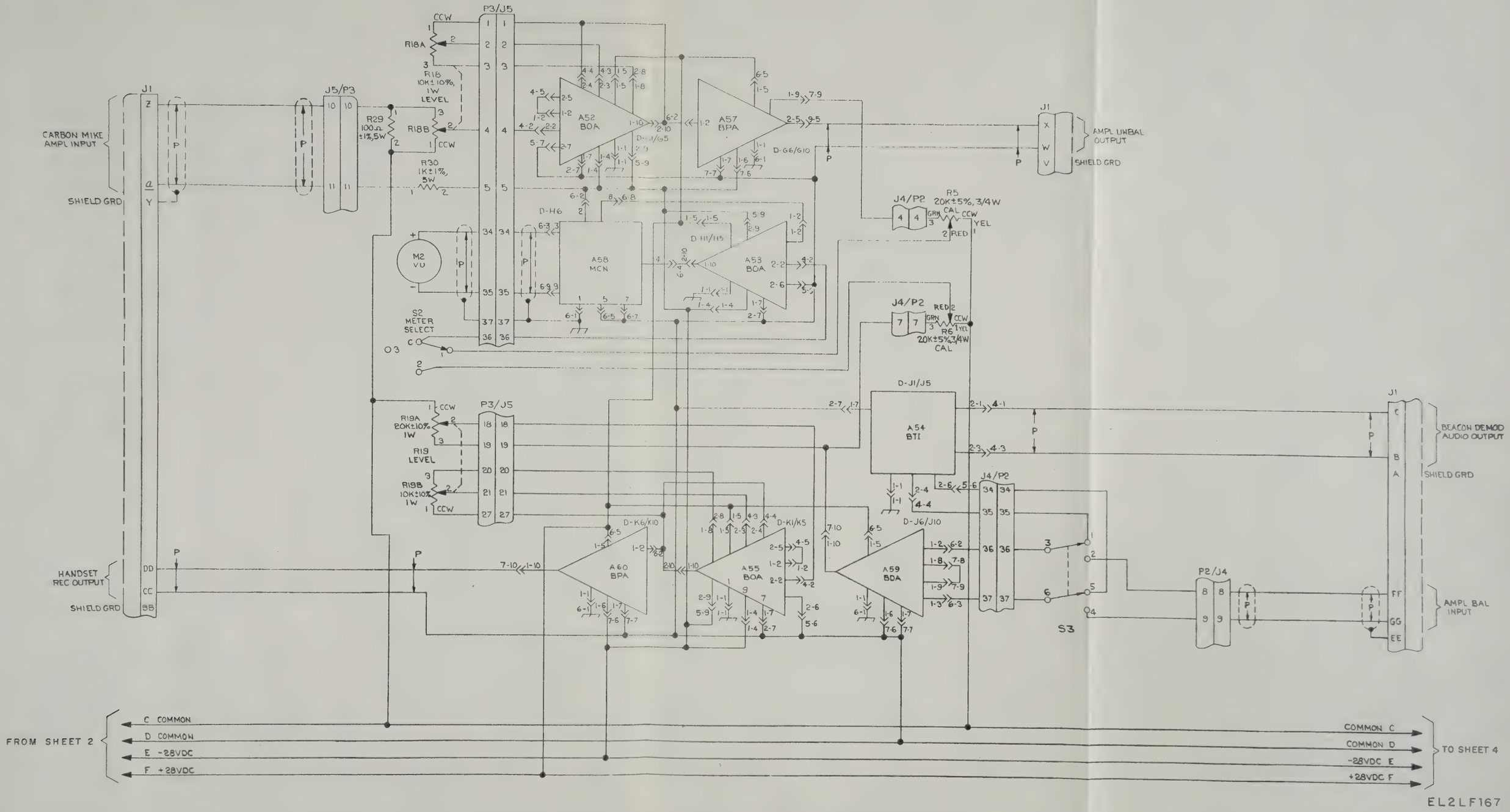
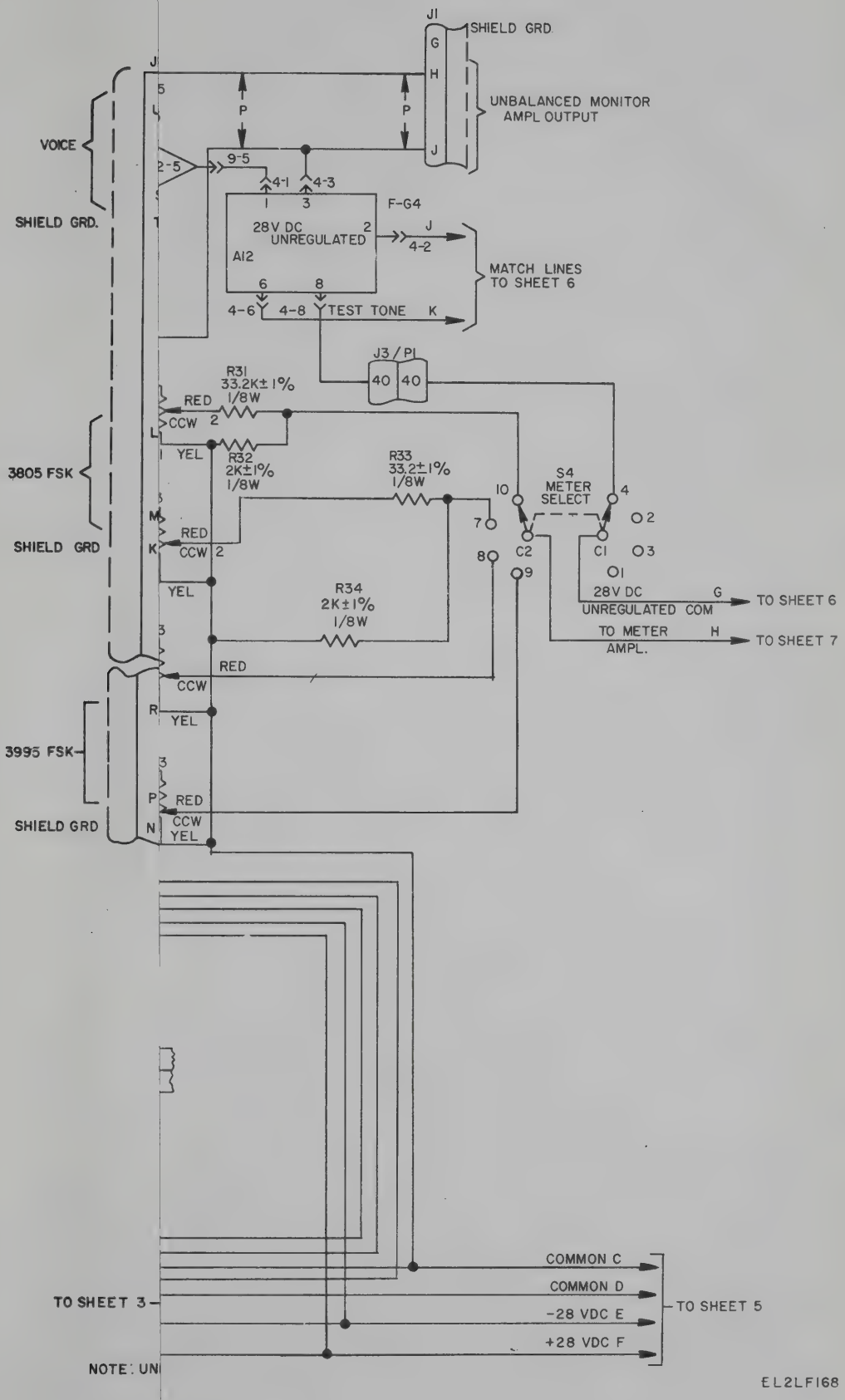


Figure FO 3-43.③ Baseband amplifier 1A3A15, schematic diagram (sheet 3 of 8).


J1
SHIELD GRD
G
H
J
UNBALANCED MONITOR AMPL OUTPUT
VOICE
SHIELD GRD.
P
P
9-5
4-1
4-3
F-G4
28V DC UNREGULATED
AI2
4-2
MATCH LINES TO SHEET 6
4-6
4-8
TEST TONE
J3 / P1
R31 33.2K±1% 1/8W
R32 2K±1% 1/8W
R33 33.2±1% 1/8W
R34 2K±1% 1/8W
RED
CCW
YEL
3805 FSK
SHIELD GRD
3995 FSK
SHIELD GRD
S4 METER SELECT
28V DC UNREGULATED COM
TO SHEET 6
TO METER AMPL.
TO SHEET 7
COMMON C
COMMON D
-28 VDC E
+28 VDC F
TO SHEET 3
TO SHEET 5
NOTE: UN
EL2LF168

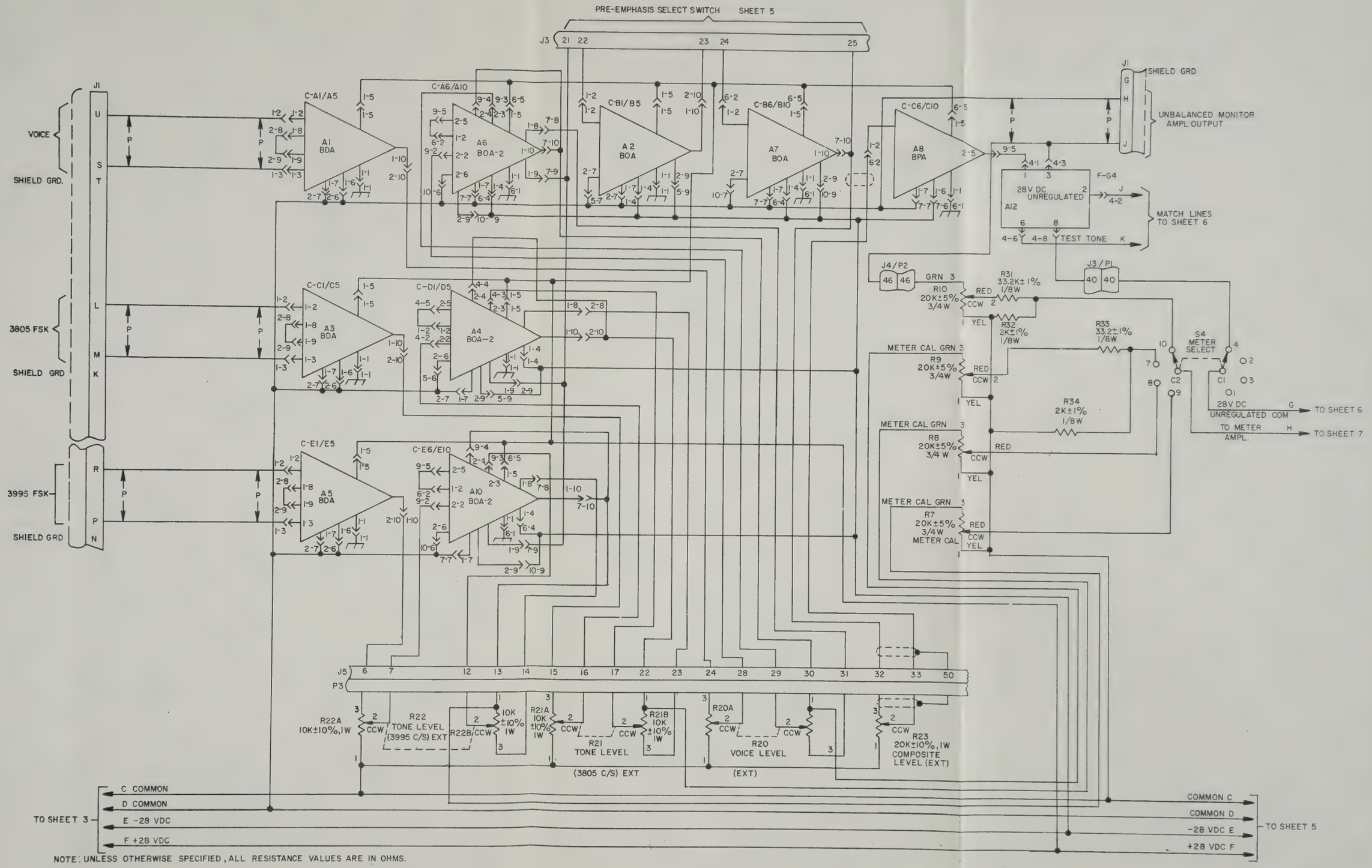
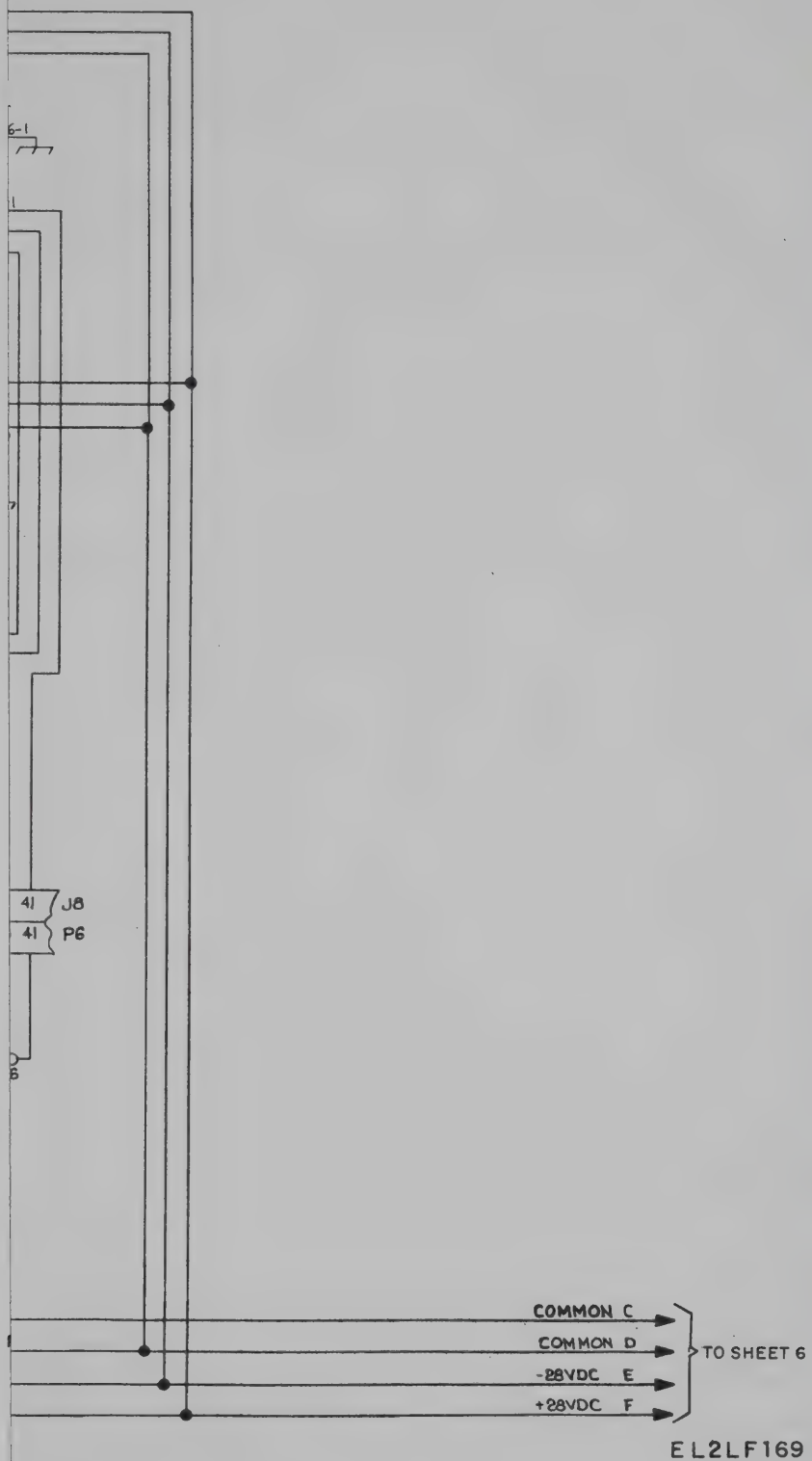


Figure FO 3-43. ④Baseband amplifier, 1A3A15, schematic diagram (sheet 4 of 8).



EL2LF169

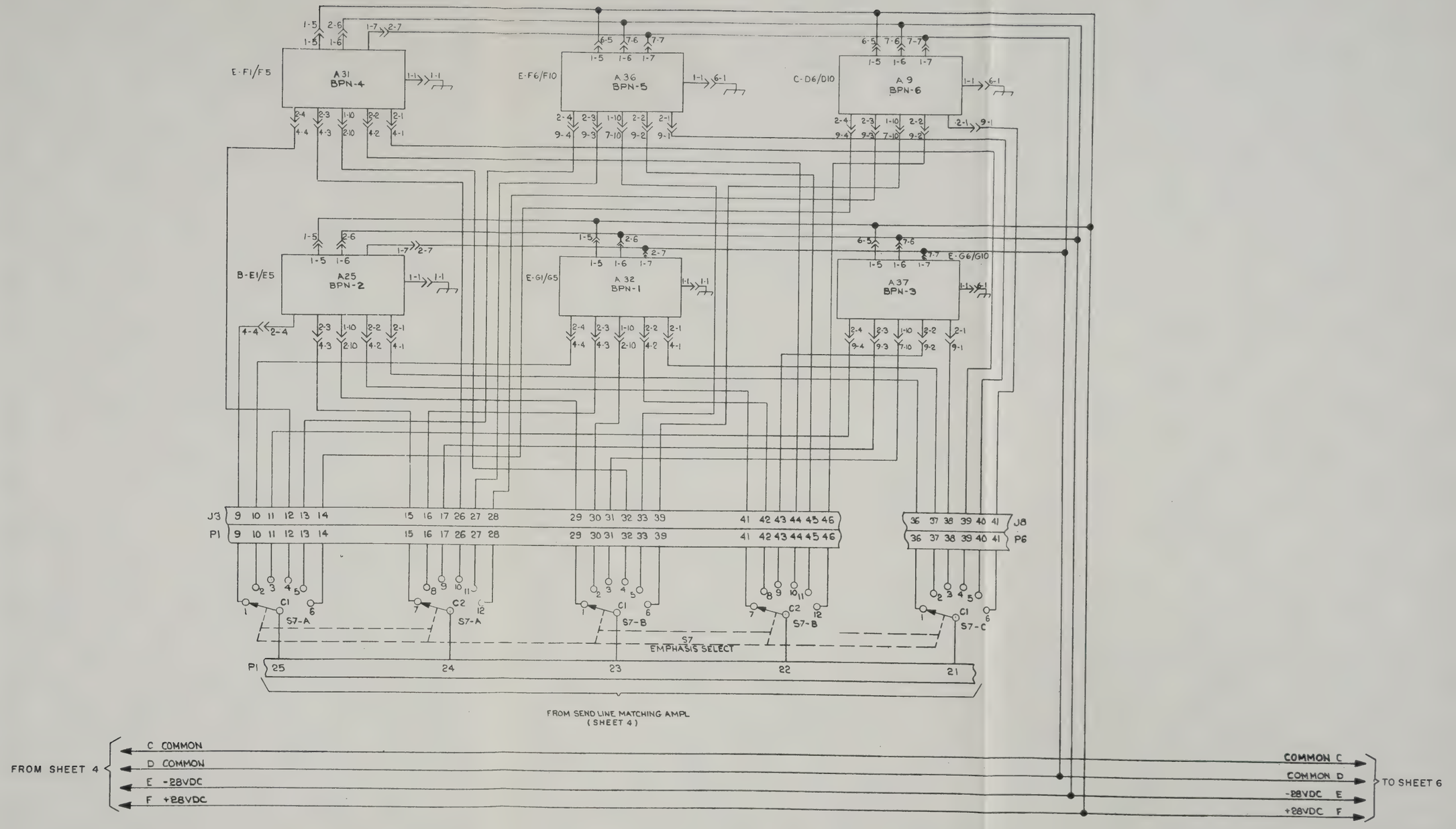
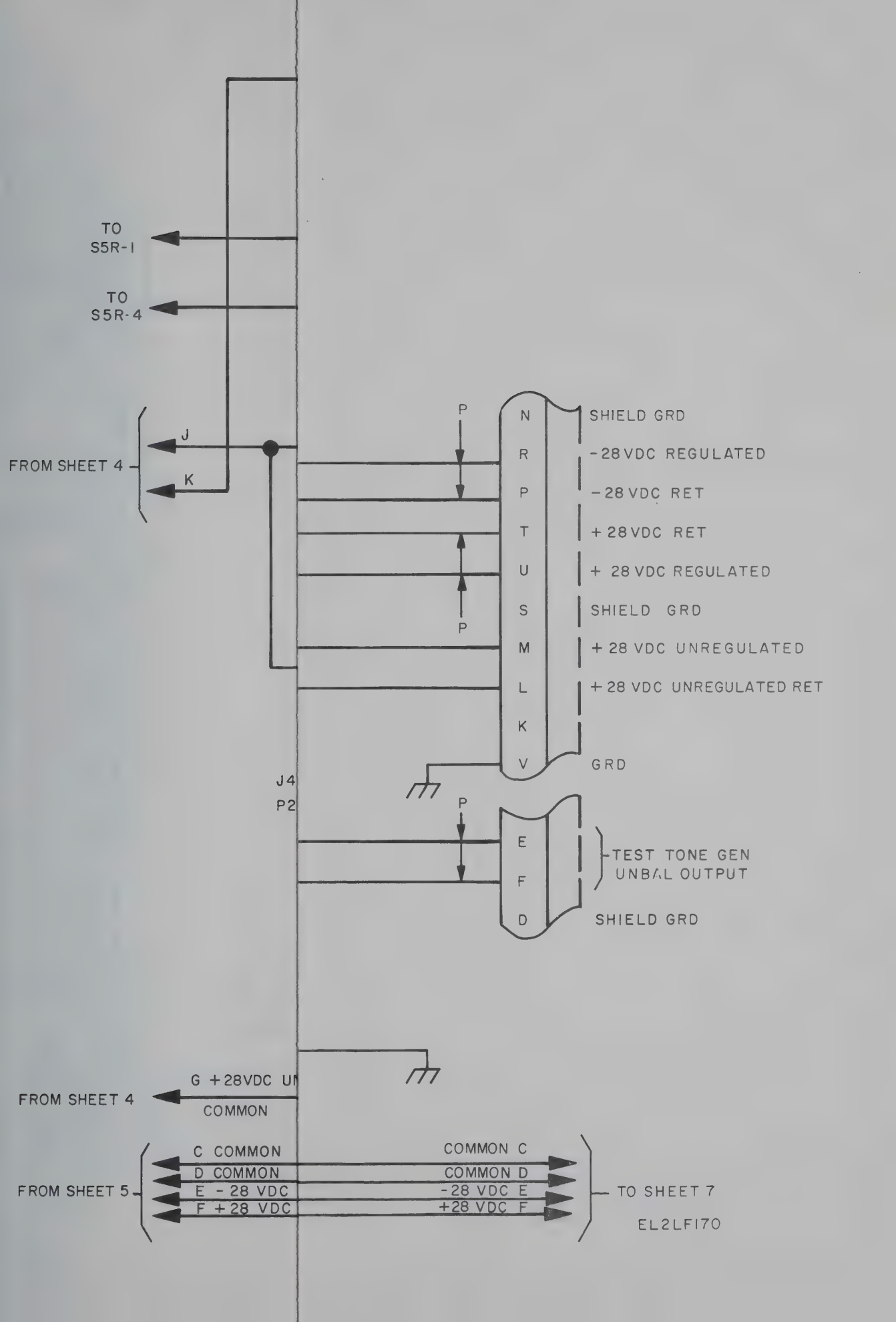


Figure FO 3-43.⑤ Baseband amplifier 1A3A15, schematic diagram (sheet 5 of 8).


TO S5R-1
TO S5R-4
FROM SHEET 4
J
K
P
P
N SHIELD GRD
R -28 VDC REGULATED
P -28 VDC RET
T +28 VDC RET
U +28 VDC REGULATED
S SHIELD GRD
M +28 VDC UNREGULATED
L +28 VDC UNREGULATED RET
K
V GRD
J4
P2
P
E
F
D
TEST TONE GEN UNBAL OUTPUT
SHIELD GRD
G +28VDC UN
FROM SHEET 4
COMMON
FROM SHEET 5
C COMMON
D COMMON
E -28 VDC
F +28 VDC
COMMON C
COMMON D
-28 VDC E
+28 VDC F
TO SHEET 7
EL2LF170

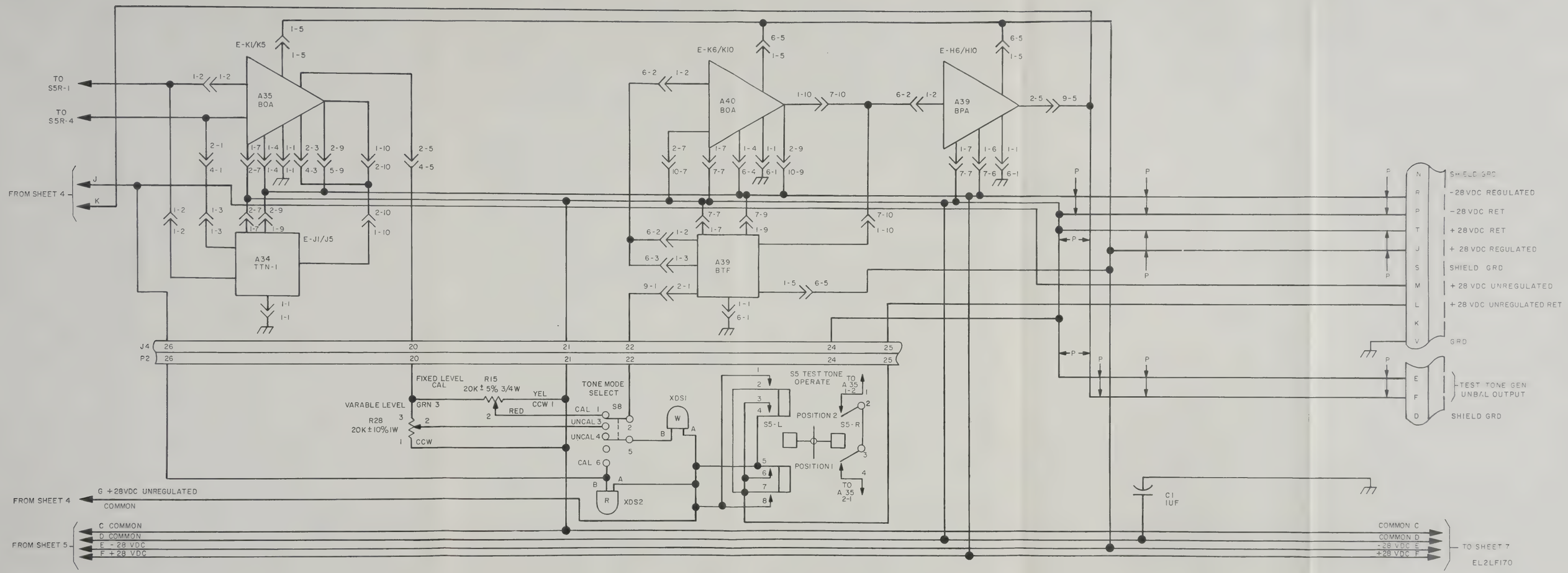
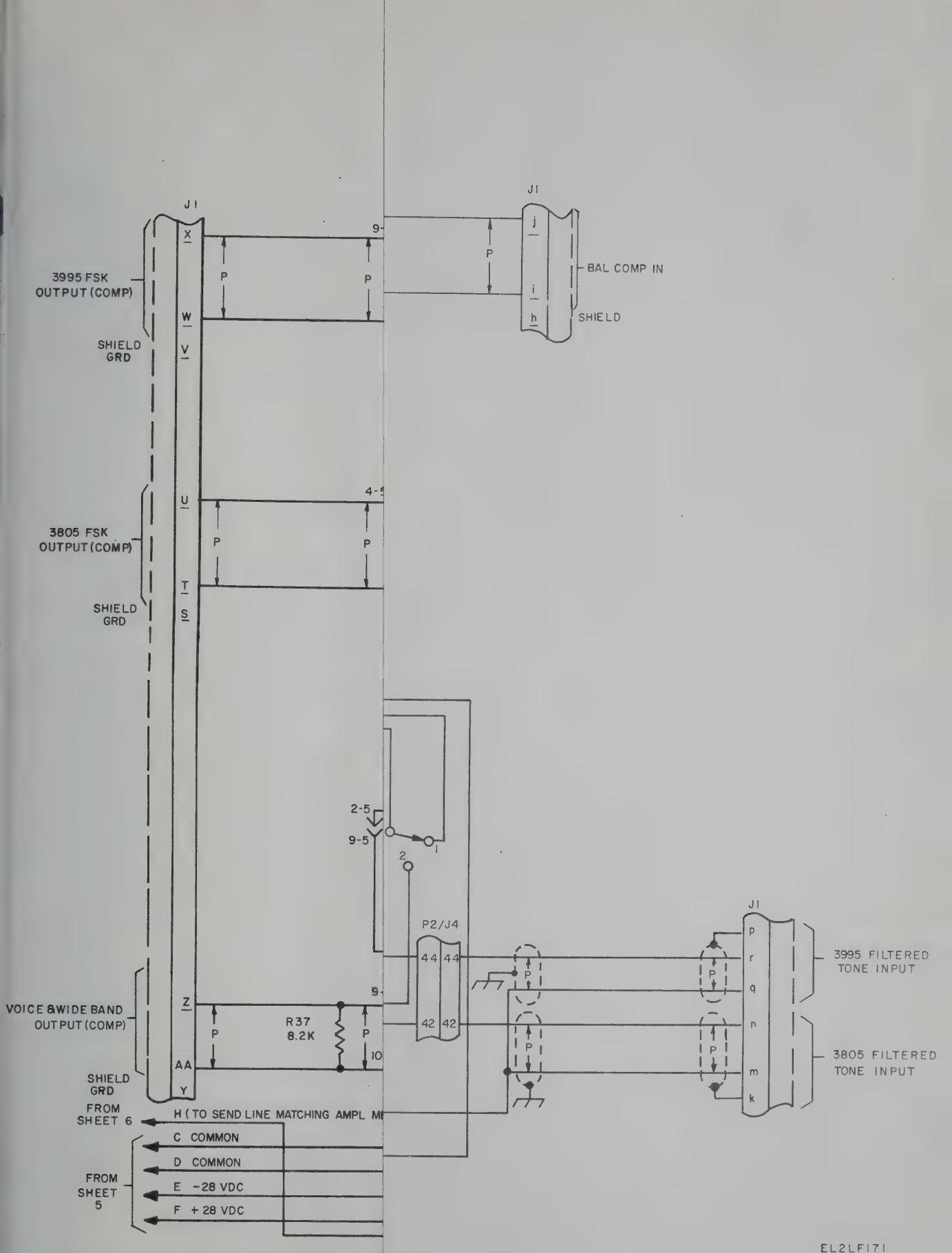


Figure FO 3-43.® Baseband amplifier 1A3A15, schematic diagram (sheet 6 of 8).


J1
X
W
V
U
T
S
Z
AA
Y
3995 FSK OUTPUT (COMP)
SHIELD GRD
3805 FSK OUTPUT (COMP)
SHIELD GRD
VOICE & WIDE BAND OUTPUT (COMP)
SHIELD GRD
P
9-
4-5
5-
10
R37 8.2K
J1
j
i
h
BAL COMP IN
SHIELD
2-5
9-5
2
1
P2/J4
44 44
42 42
J1
p
r
q
n
m
k
3995 FILTERED TONE INPUT
3805 FILTERED TONE INPUT
FROM SHEET 6
H (TO SEND LINE MATCHING AMPL M
FROM SHEET 5
C COMMON
D COMMON
E -28 VDC
F +28 VDC
EL2LF171

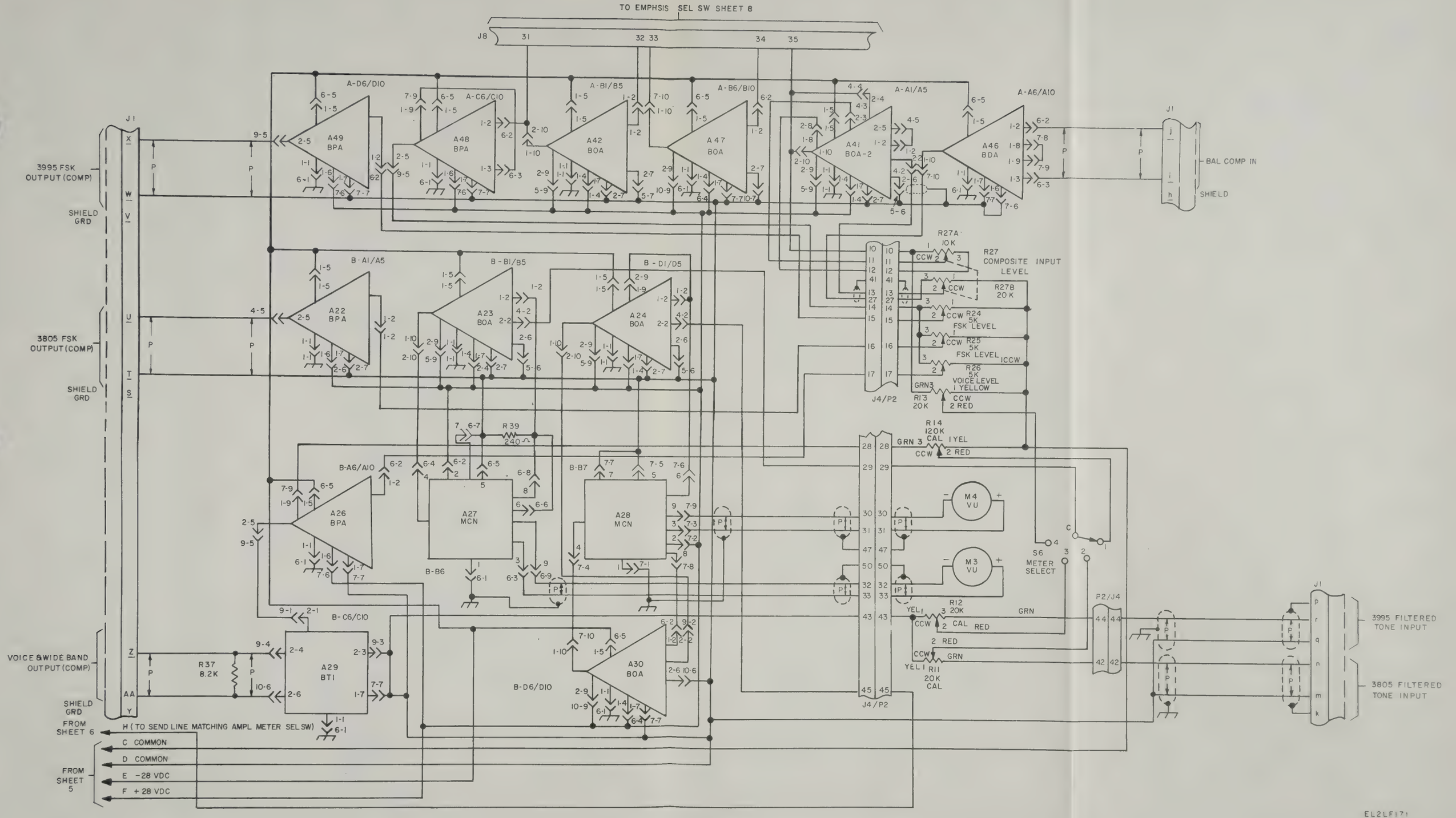
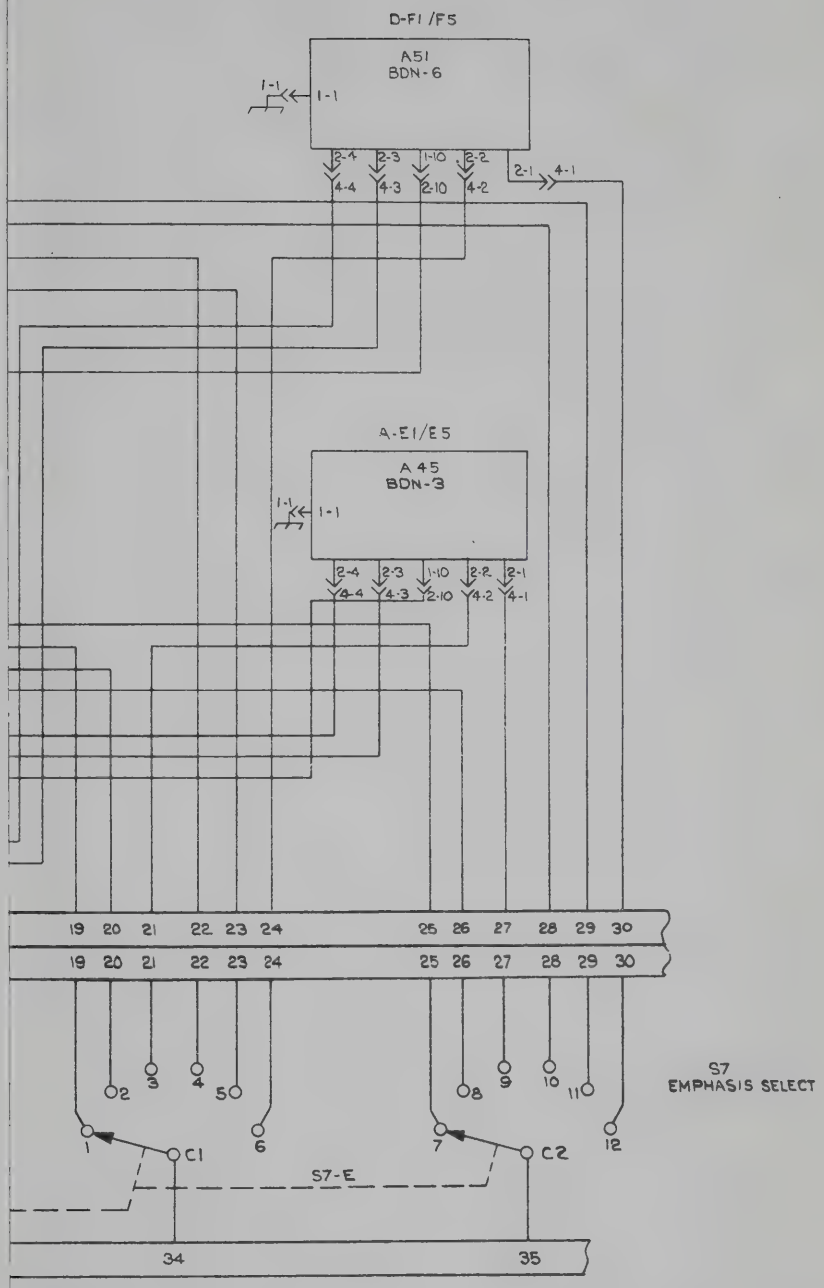


Figure FO 3-43.① Baseband amplifier 1A3A15, schematic diagram (sheet 7 of 8).



. (SHEET 7).

EL 2LF172

natic diagram (sheet 8 of 8).

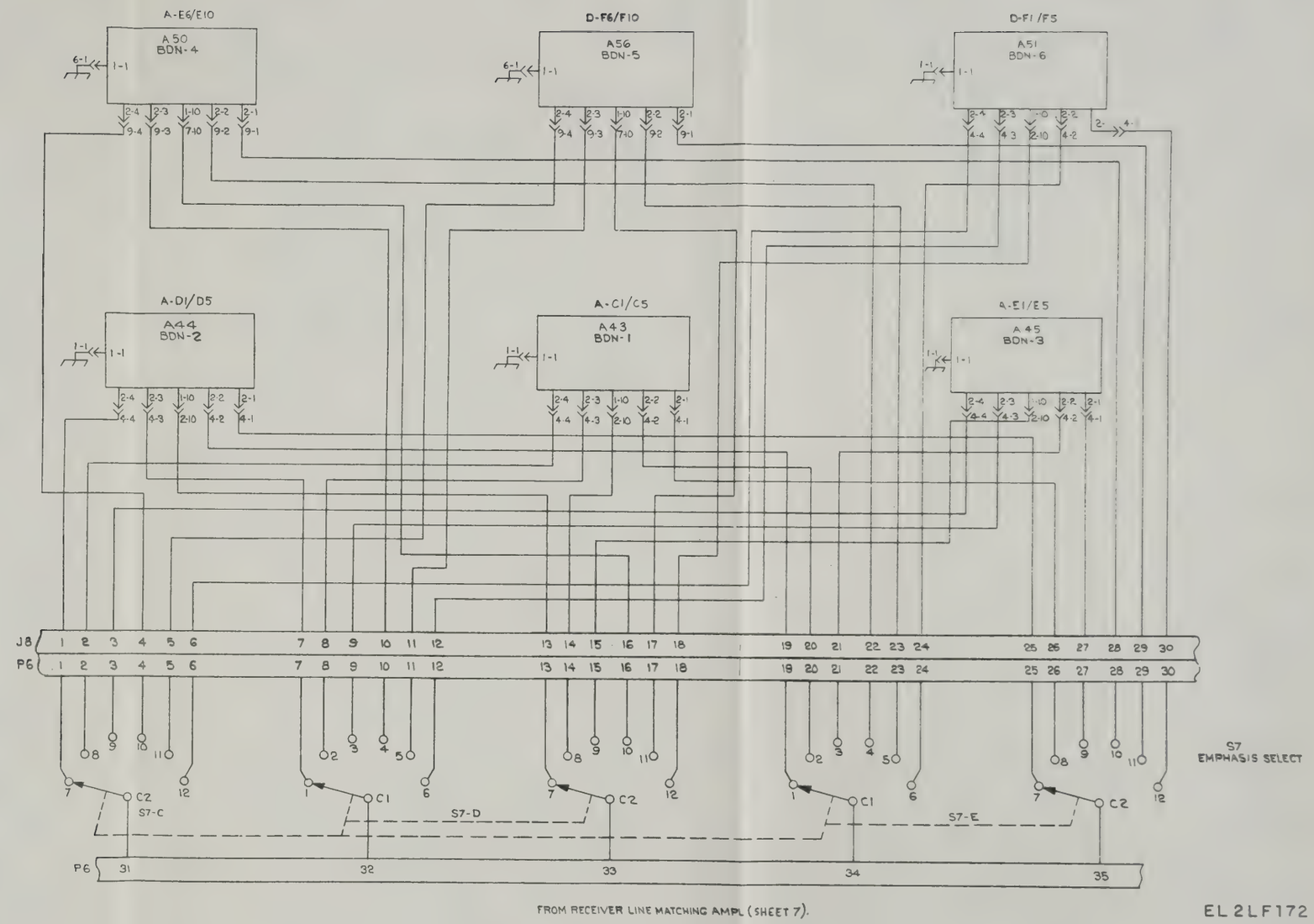
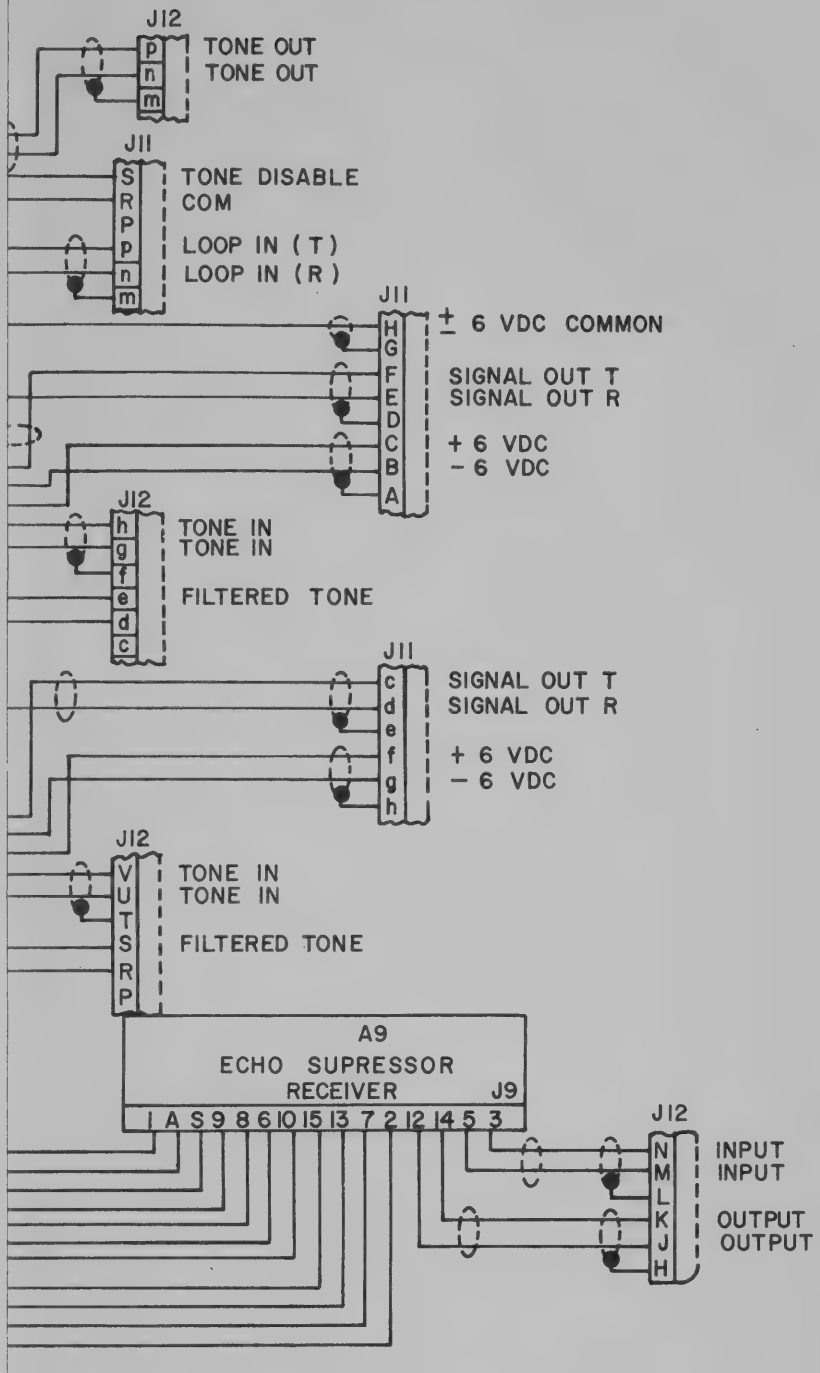


Figure FO 3-43.Ⓢ Baseband amplifier 1A3A15, schematic diagram (sheet 8 of 8).



NOTE:
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S).

EL2LF182

agram.

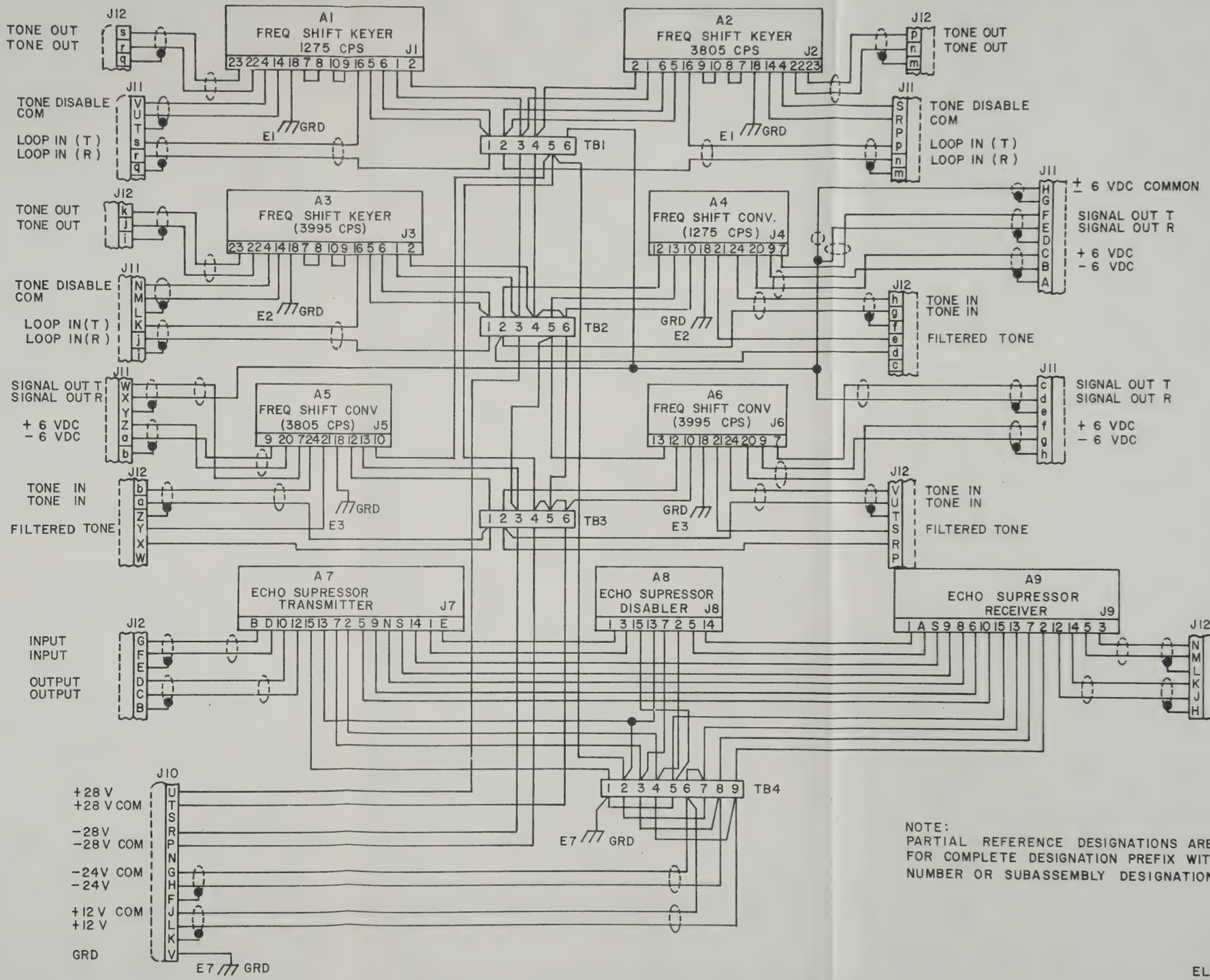
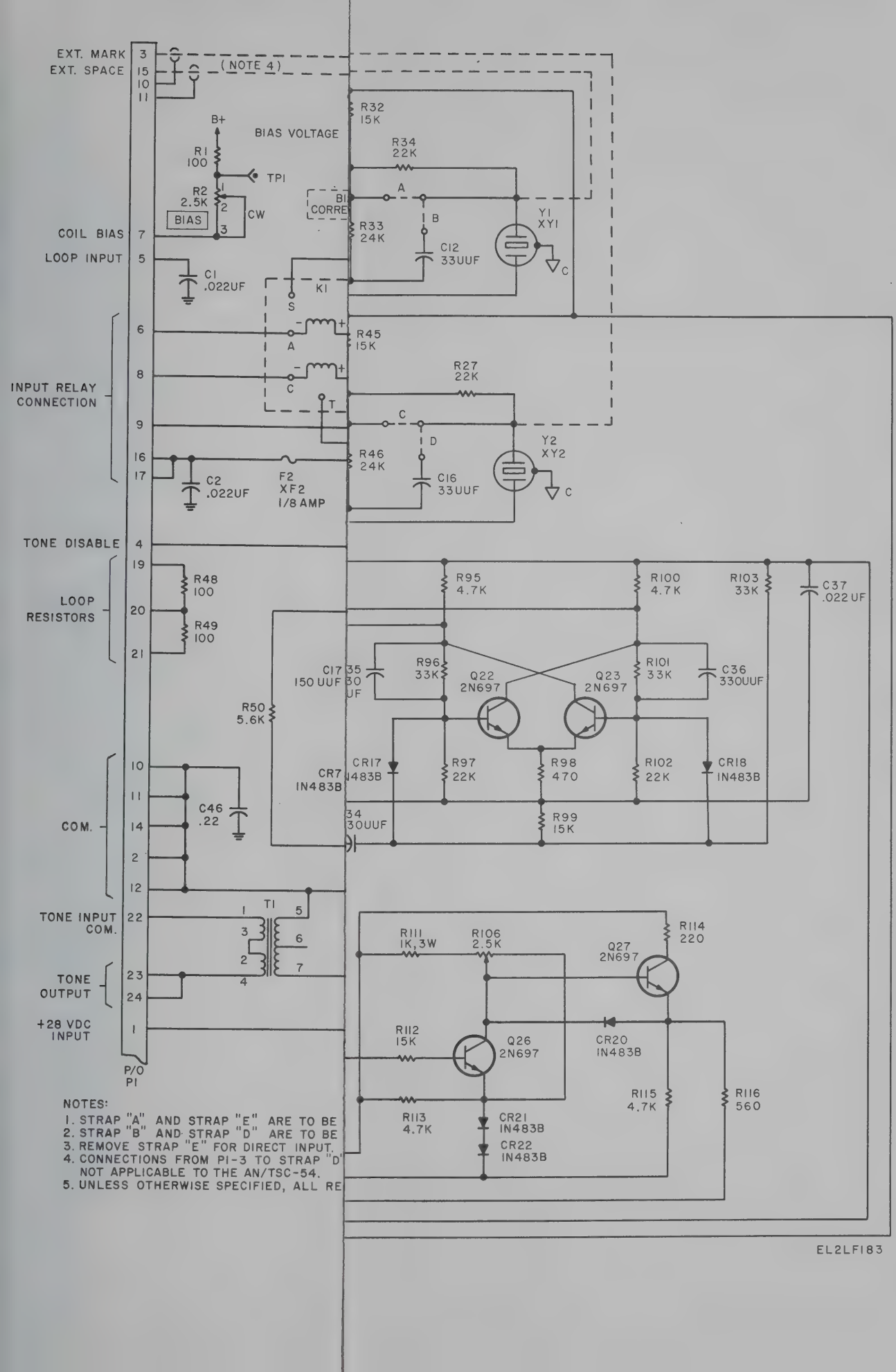


Figure FO 3-44. Converter-keyer and echo suppressor 1A3A16, schematic diagram.

NOTE:
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S).

EL2LF182


EXT. MARK
EXT. SPACE
(NOTE 4)
B+
BIAS VOLTAGE
R1 100
TP1
R2 2.5K
BIAS
CW
COIL BIAS
LOOP INPUT
C1 .022UF
R32 15K
R34 22K
R33 24K
C12 33UUF
Y1 XY1
K1
R45 15K
R27 22K
R46 24K
C16 33UUF
Y2 XY2
C2 .022UF
F2 XF2 1/8 AMP
INPUT RELAY CONNECTION
TONE DISABLE
LOOP RESISTORS
R48 100
R49 100
R95 4.7K
R100 4.7K
R103 33K
C37 .022 UF
R96 33K
R101 33K
C36 330UUF
Q22 2N697
Q23 2N697
C17 150 UUF
R50 5.6K
CR17 IN483B
CR18 IN483B
R97 22K
R98 470
R102 22K
R99 15K
C46 .22
COM.
TONE INPUT COM.
TONE OUTPUT
+28 VDC INPUT
T1
R111 1K,3W
R106 2.5K
R114 220
Q27 2N697
R112 15K
Q26 2N697
CR20 IN483B
R113 4.7K
CR21 IN483B
CR22 IN483B
R115 4.7K
R116 560
P/O P1
NOTES:
1. STRAP "A" AND STRAP "E" ARE TO BE
2. STRAP "B" AND STRAP "D" ARE TO BE
3. REMOVE STRAP "E" FOR DIRECT INPUT.
4. CONNECTIONS FROM P1-3 TO STRAP "D"
NOT APPLICABLE TO THE AN/TSC-54.
5. UNLESS OTHERWISE SPECIFIED, ALL RE
EL2LF183

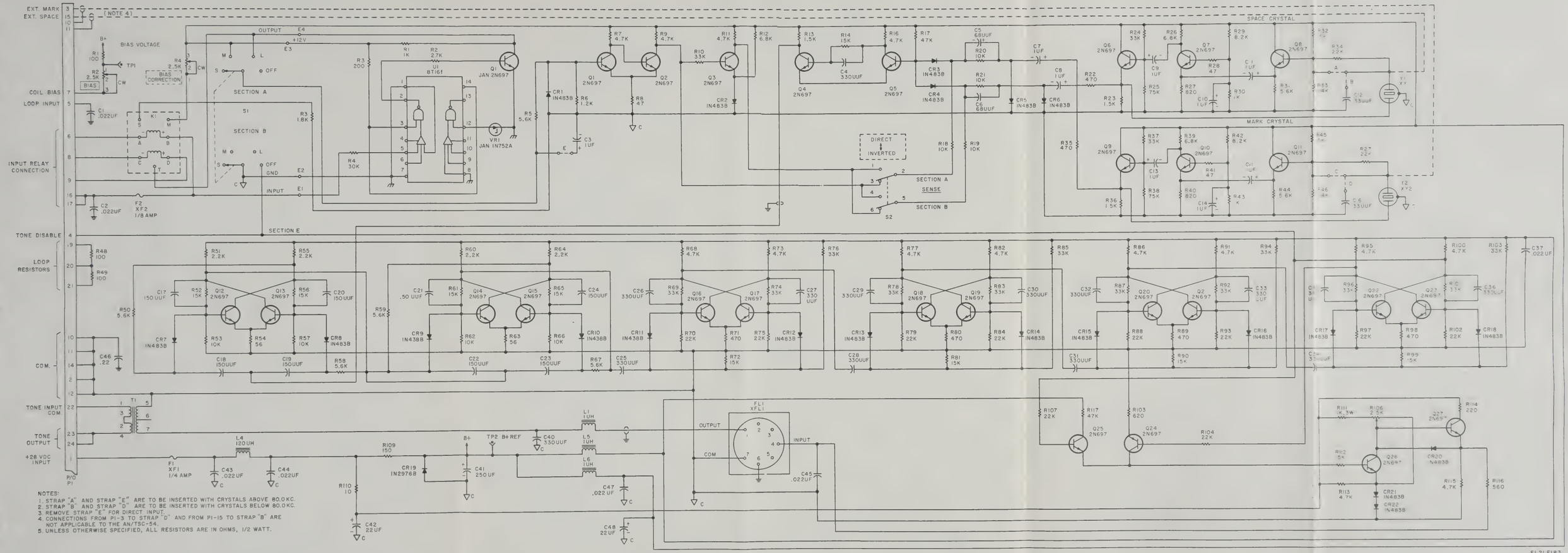
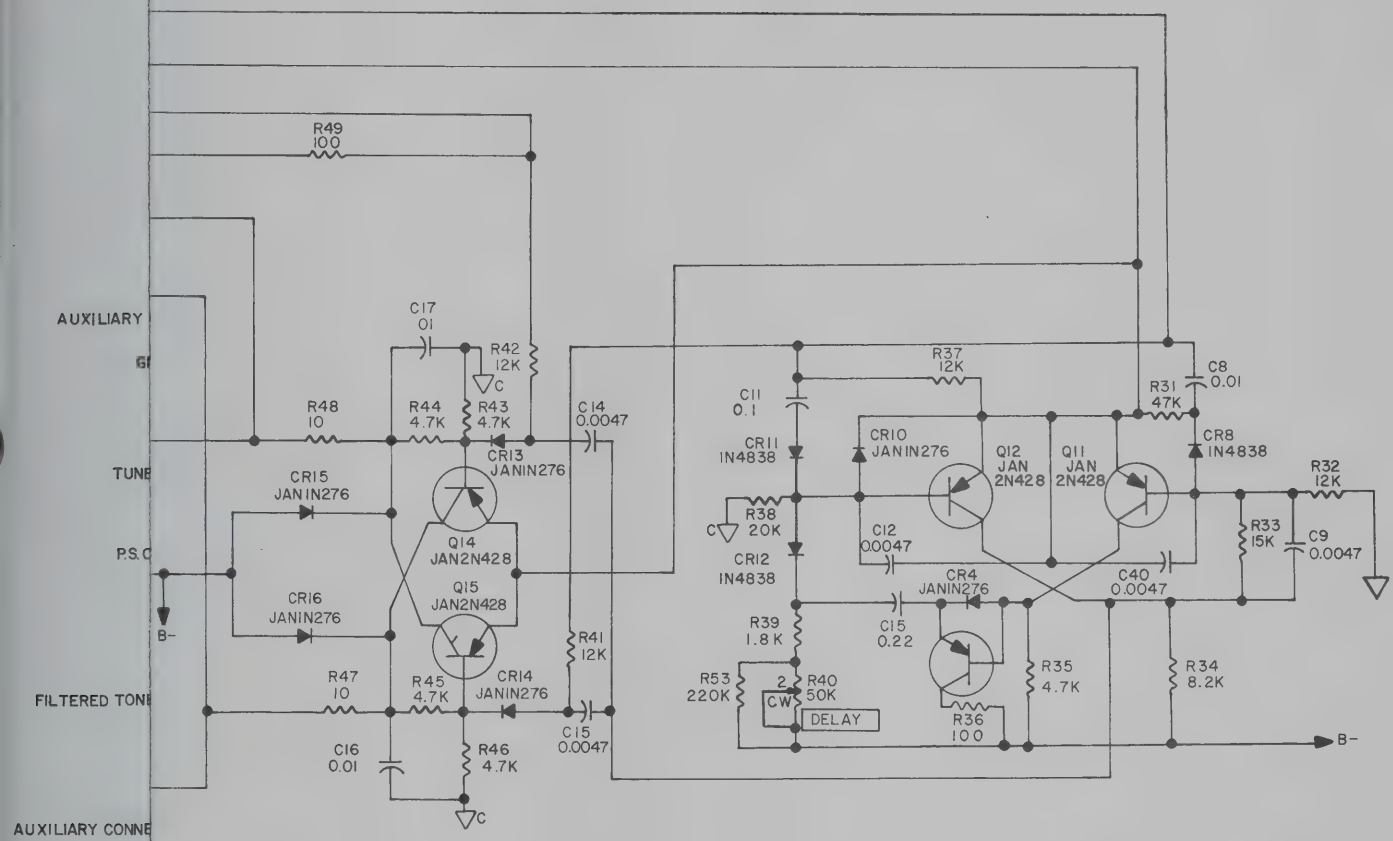


Figure FO 3-45. Frequency shift keyer, schematic diagram.


R49
100
AUXILIARY
GE
TUNE
P.S.C
B-
FILTERED TONE
AUXILIARY CONNE
C17
01
R42
12K
C
R48
10
R44
4.7K
R43
4.7K
C14
0.0047
CR13
JANIN276
CR15
JANIN276
Q14
JAN2N428
Q15
JAN2N428
CR16
JANIN276
R41
12K
R47
10
R45
4.7K
CR14
JANIN276
C15
0.0047
C16
0.01
R46
4.7K
C
C11
0.1
CR11
IN4838
R38
20K
C
CR12
IN4838
R39
1.8K
R53
220K
2
R40
50K
CW
DELAY
C15
0.22
R37
12K
CR10
JANIN276
Q12
JAN
2N428
Q11
JAN
2N428
C8
0.01
R31
47K
CR8
IN4838
R32
12K
R33
15K
C9
0.0047
C12
0.0047
CR4
JANIN276
C40
0.0047
R35
4.7K
R36
100
R34
8.2K
B-

EL2LF184

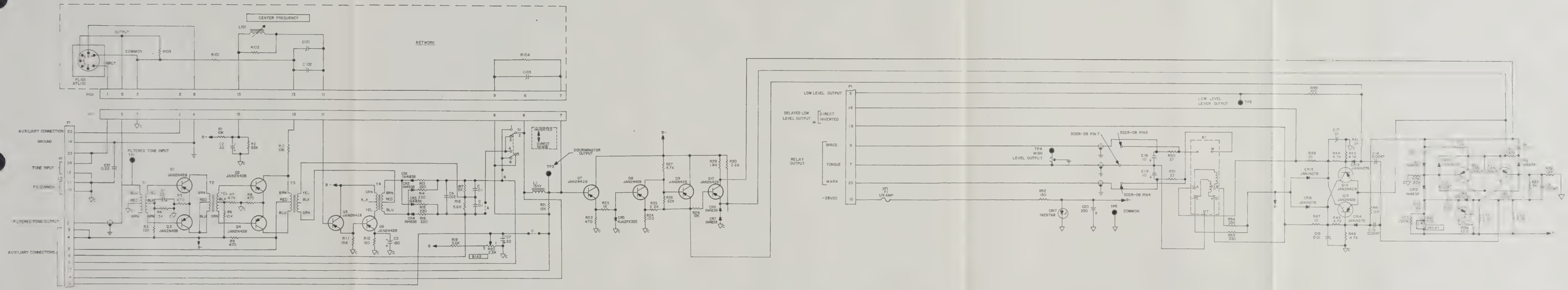
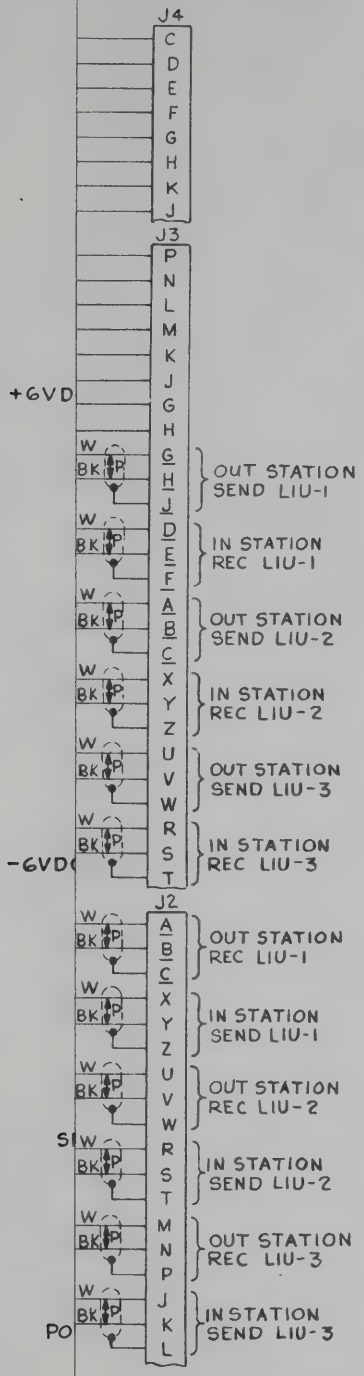


Figure FO 5-46. Frequency shift converter, schematic diagram.



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATIONS.
2. WIRE ROUTING IS OPTIONAL, ROUTE SHOWN IS FOR REFERENCE ONLY.
3. UNDERLINED LETTERS SIGNIFY LOWER-CASE LETTERS.
4. UNLESS OTHERWISE SPECIFIED; WIRE SIZE IS AWG 20, COLOR WHITE. SHIELDED TWISTED PAIR WIRE SIZE IS AWG 22, COLOR AS NOTED. SHIELD TERMINATION WIRE SIZE IS AWG 20, COLOR GREEN.

EL2LF190

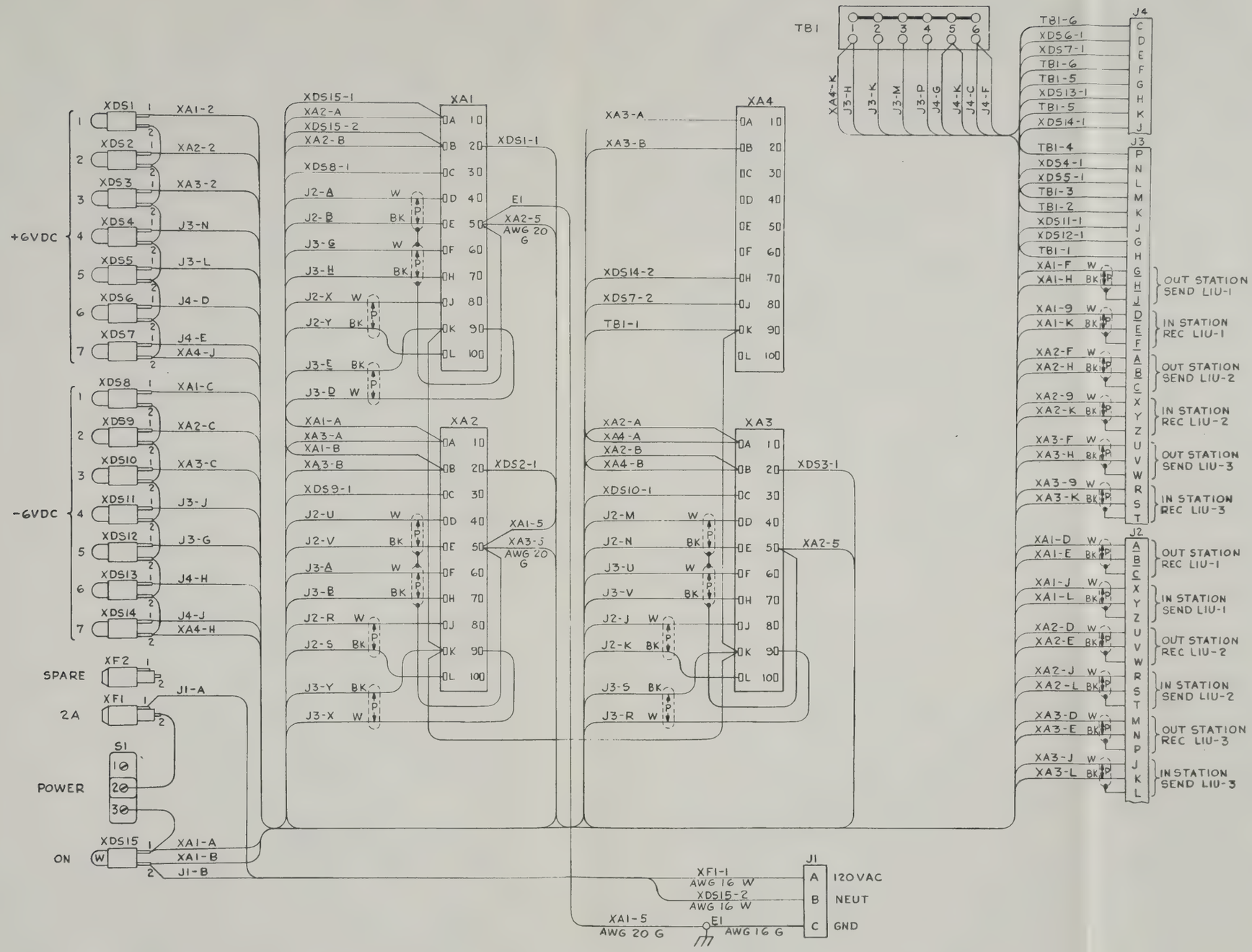
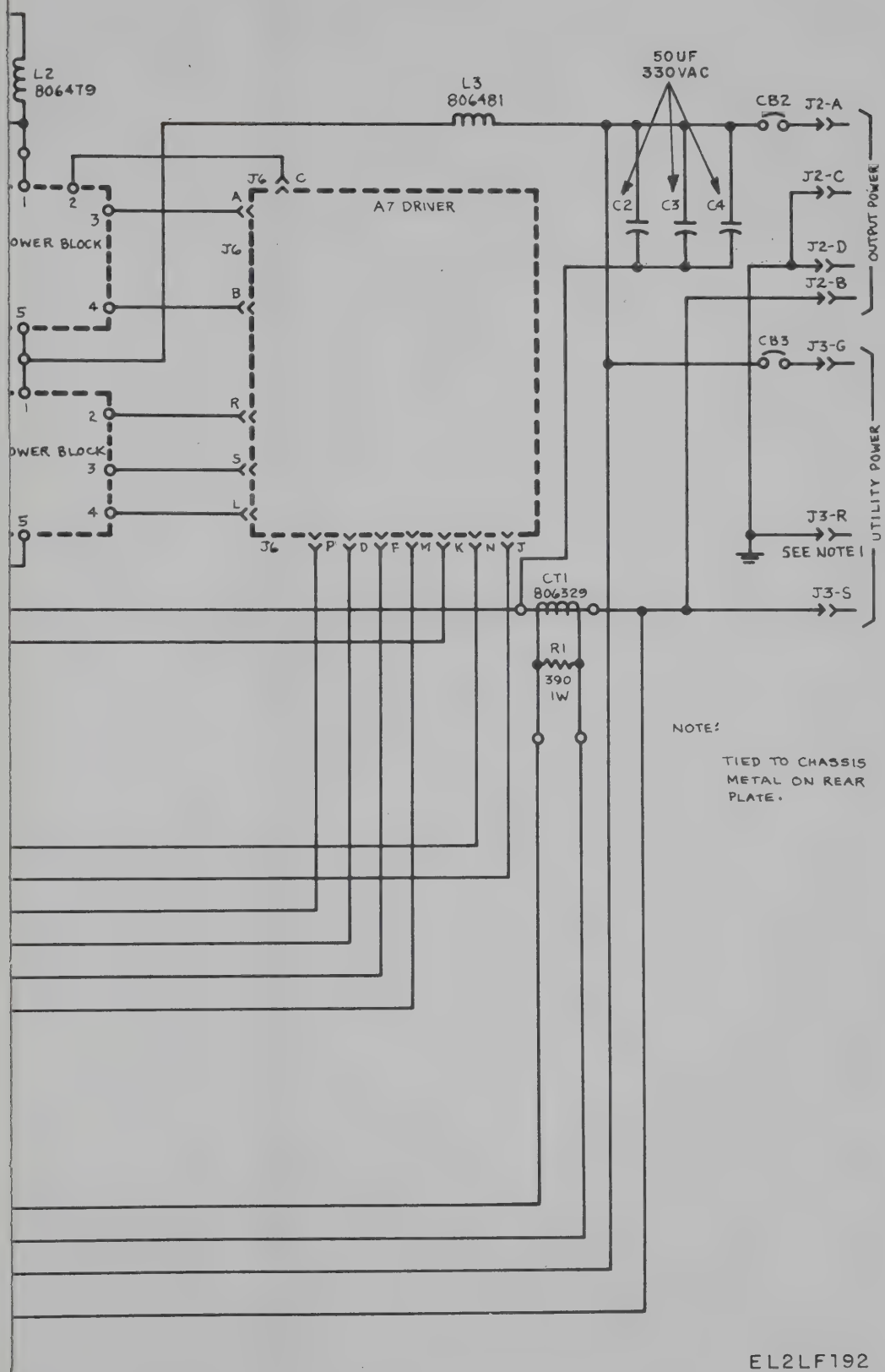


Figure FO 3-47. Line isolation panel 1A3A26, schematic diagram.


L2
806479
L3
806481
50UF
330VAC
CB2
J2-A
J2-C
J2-D
J2-B
OUTPUT POWER
C2
C3
C4
A7 DRIVER
J6
A
B
C
R
S
L
P
D
F
M
K
N
J
POWER BLOCK
POWER BLOCK
CB3
J3-G
J3-R
SEE NOTE 1
UTILITY POWER
CT1
806329
J3-S
R1
390
1W
NOTE:
TIED TO CHASSIS METAL ON REAR PLATE.

EL2LF192

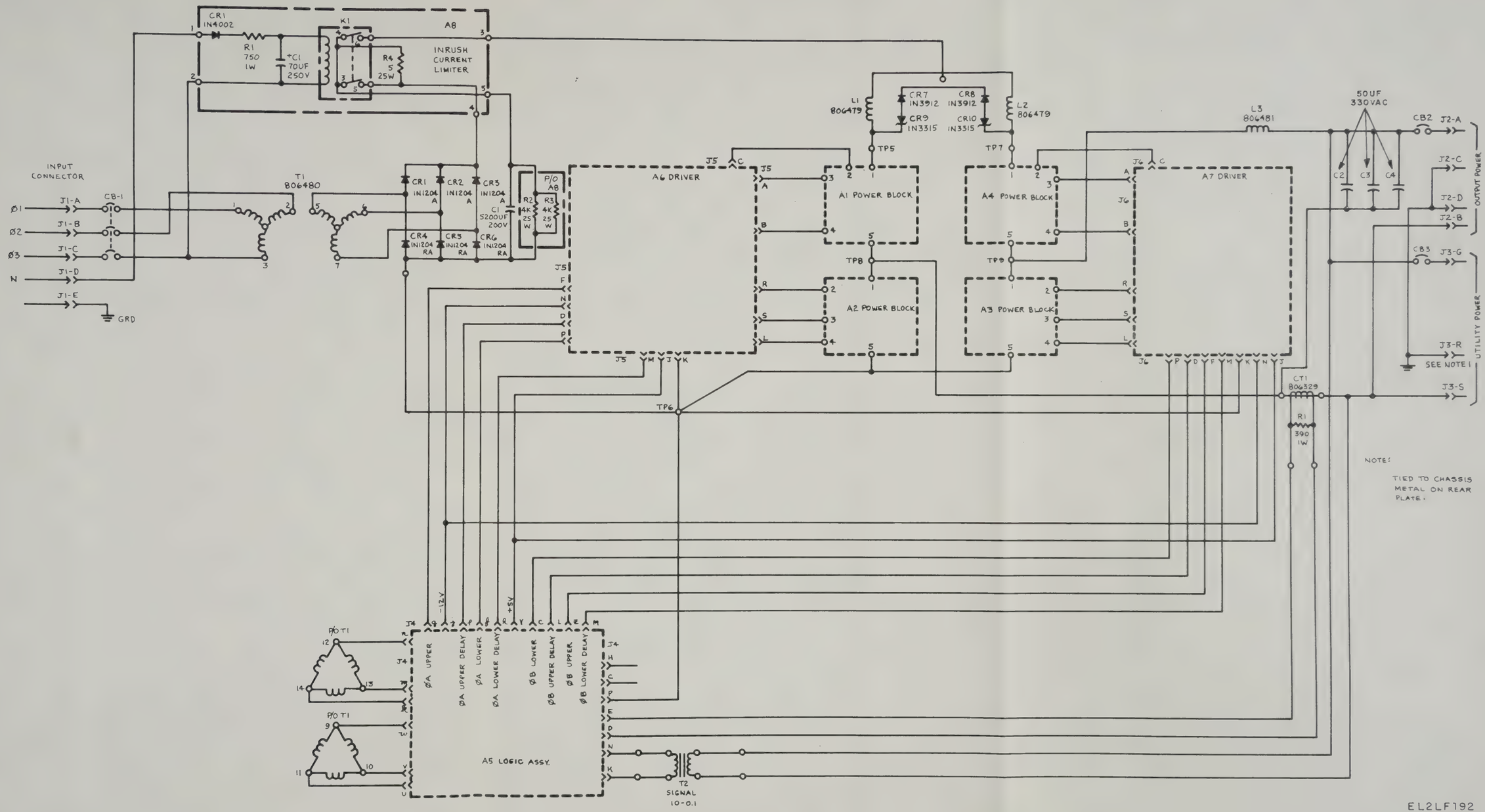


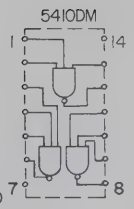
Figure FO 3-48. 2.0 KW static frequency converter, schematic diagram.

M
14
8
OF:
8

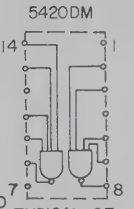
DM
14
8
OF:
,IC31
37

DDM
14
8
L OF:
2,IC32

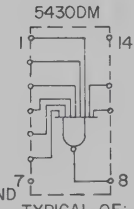
5DM
14
8
L OF:
34,IC36



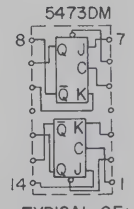
TYPICAL OF:
IC15,IC16,IC17
IC21,IC22,IC23
IC24,IC25



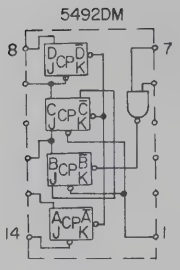
TYPICAL OF:
IC5



TYPICAL OF:
IC18,IC22,IC26



TYPICAL OF:
IC3,IC4,IC6
IC11,IC13,IC14



TYPICAL OF:
IC8

TYPICAL OF:
IC2

EL2LF193

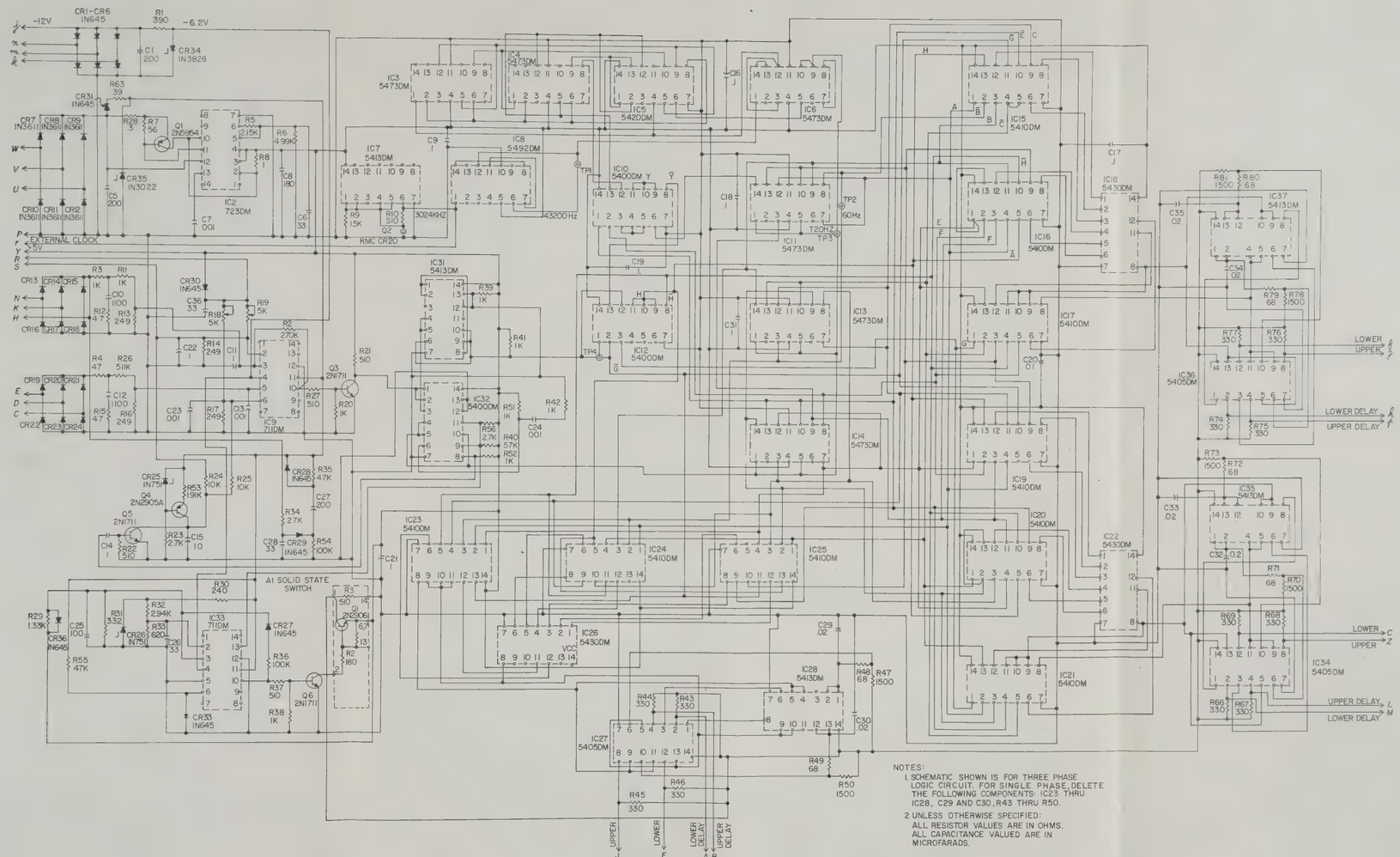
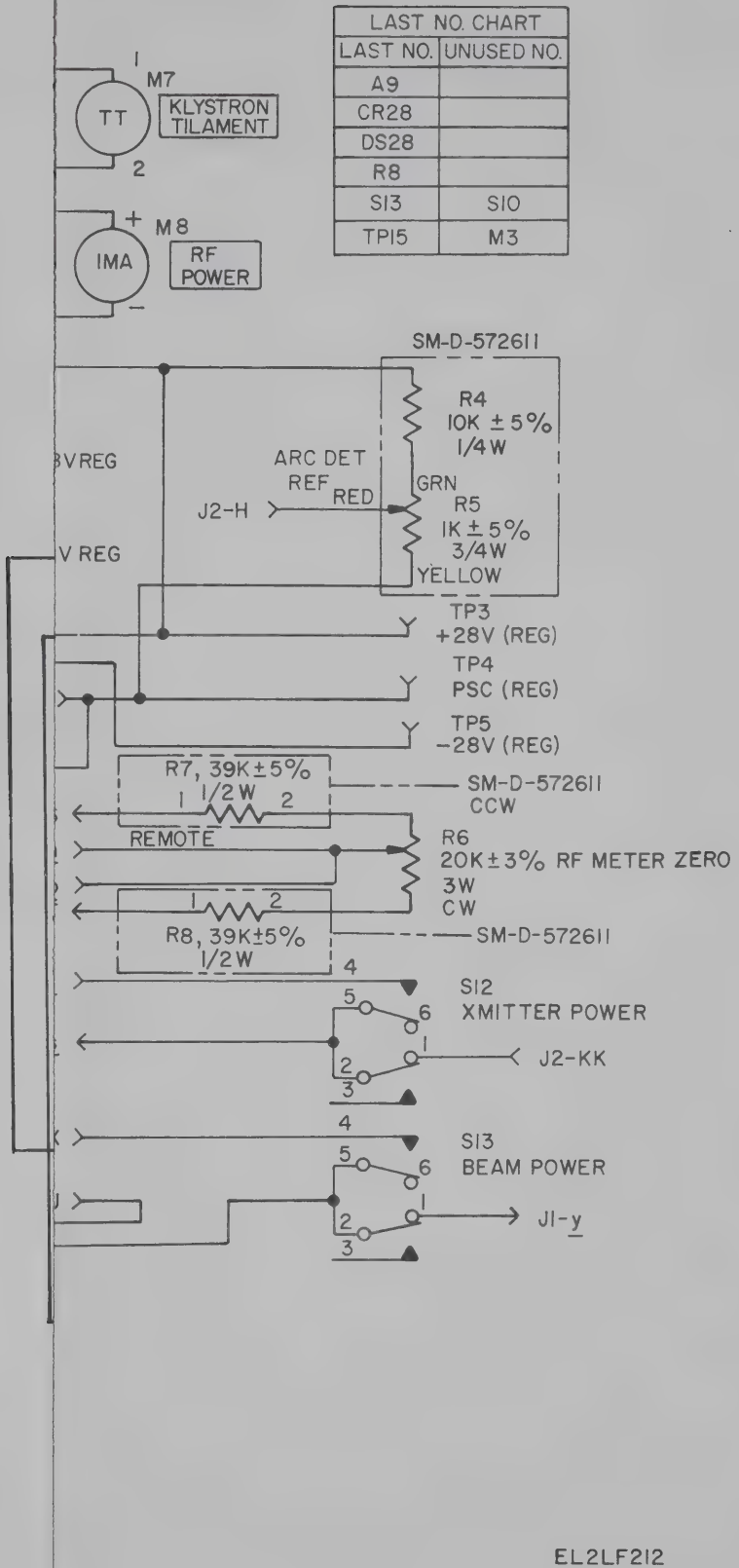


Figure FO 3-49. Logic assembly A5, schematic diagram.

LAST NO. CHART	
LAST NO.	UNUSED NO.
A9	
CR28	
DS28	
R8	
SI3	SIO
TPI5	M3



EL2LF212

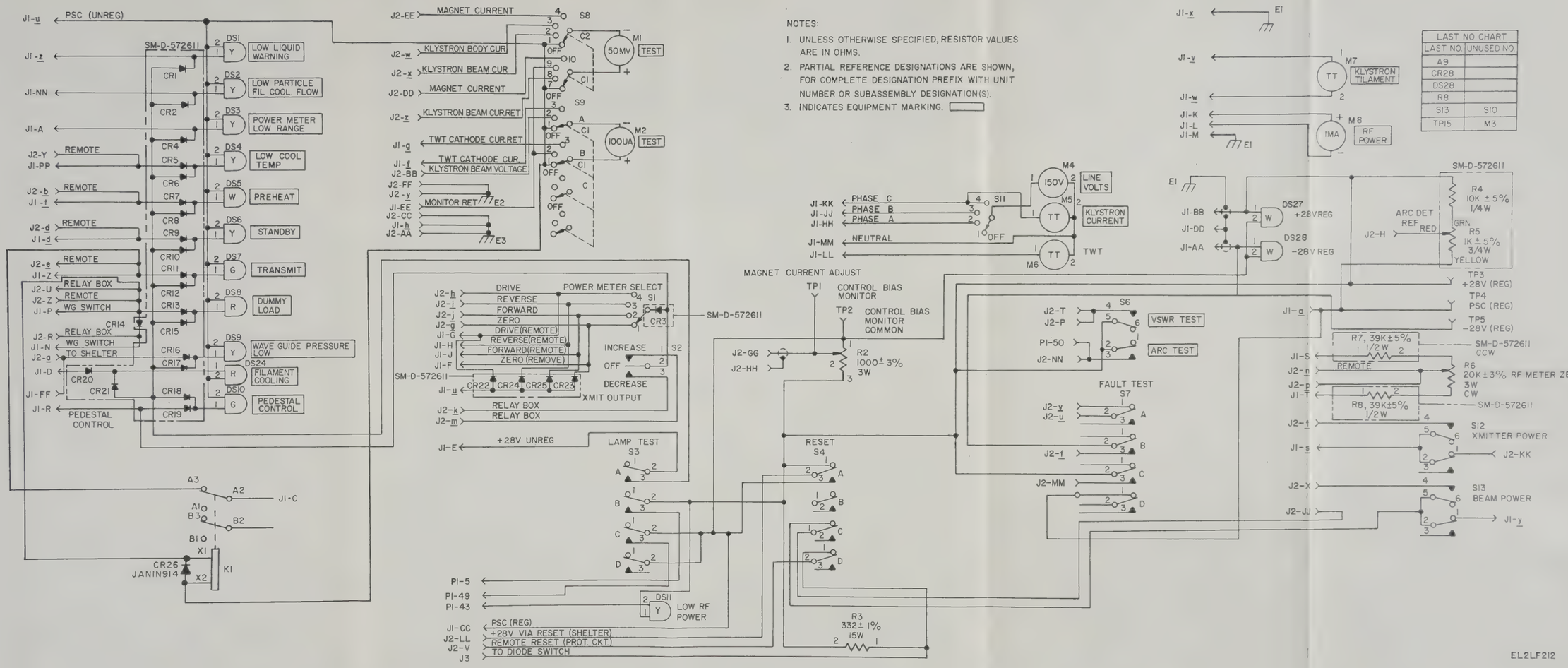
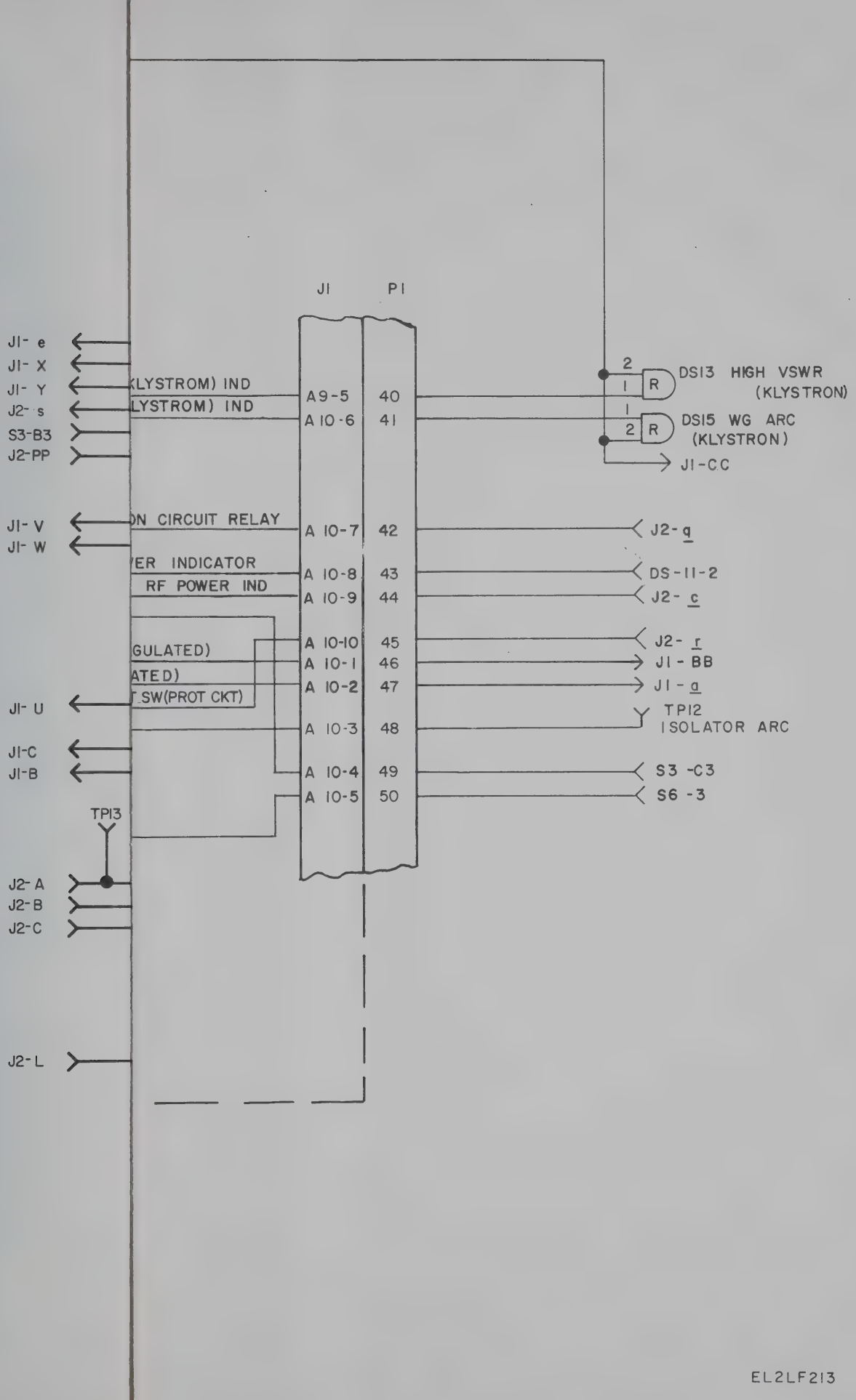


Figure FO3-52.1 Transmitter control panel, schematic diagram (sheet 1 of 2).


J1
P1
J1- e
J1- X
J1- Y
J2- s
S3-B3
J2-PP
J1- V
J1- W
J1- U
J1-C
J1-B
TP13
J2- A
J2- B
J2- C
J2- L
KLYSTROM) IND
LYSTROM) IND
ON CIRCUIT RELAY
VER INDICATOR
RF POWER IND
GULATED)
ATED)
T SW(PROT CKT)
A9-5
A10-6
A10-7
A10-8
A10-9
A10-10
A10-1
A10-2
A10-3
A10-4
A10-5
40
41
42
43
44
45
46
47
48
49
50
2
1
R
DSI3 HIGH VSWR
(KLYSTRON)
1
2
R
DSI5 WG ARC
(KLYSTRON)
J1-CC
J2- q
DS-11-2
J2- c
J2- r
J1 - BB
J1 - a
TP12
ISOLATOR ARC
S3 -C3
S6 -3

EL2LF213

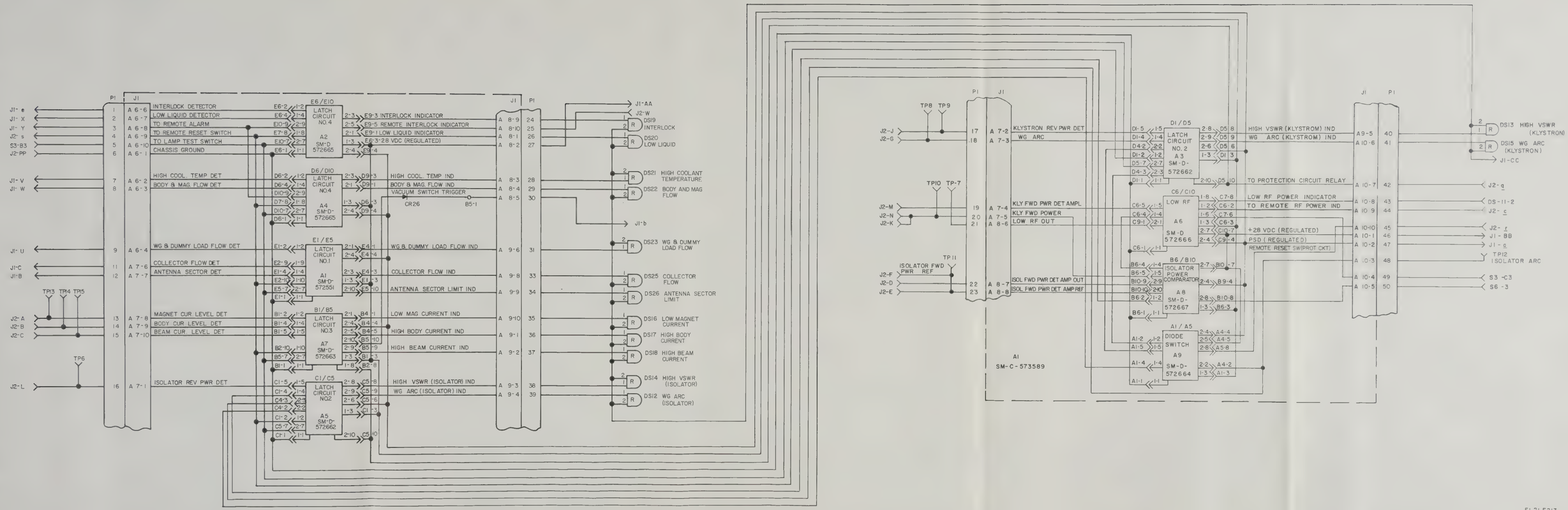
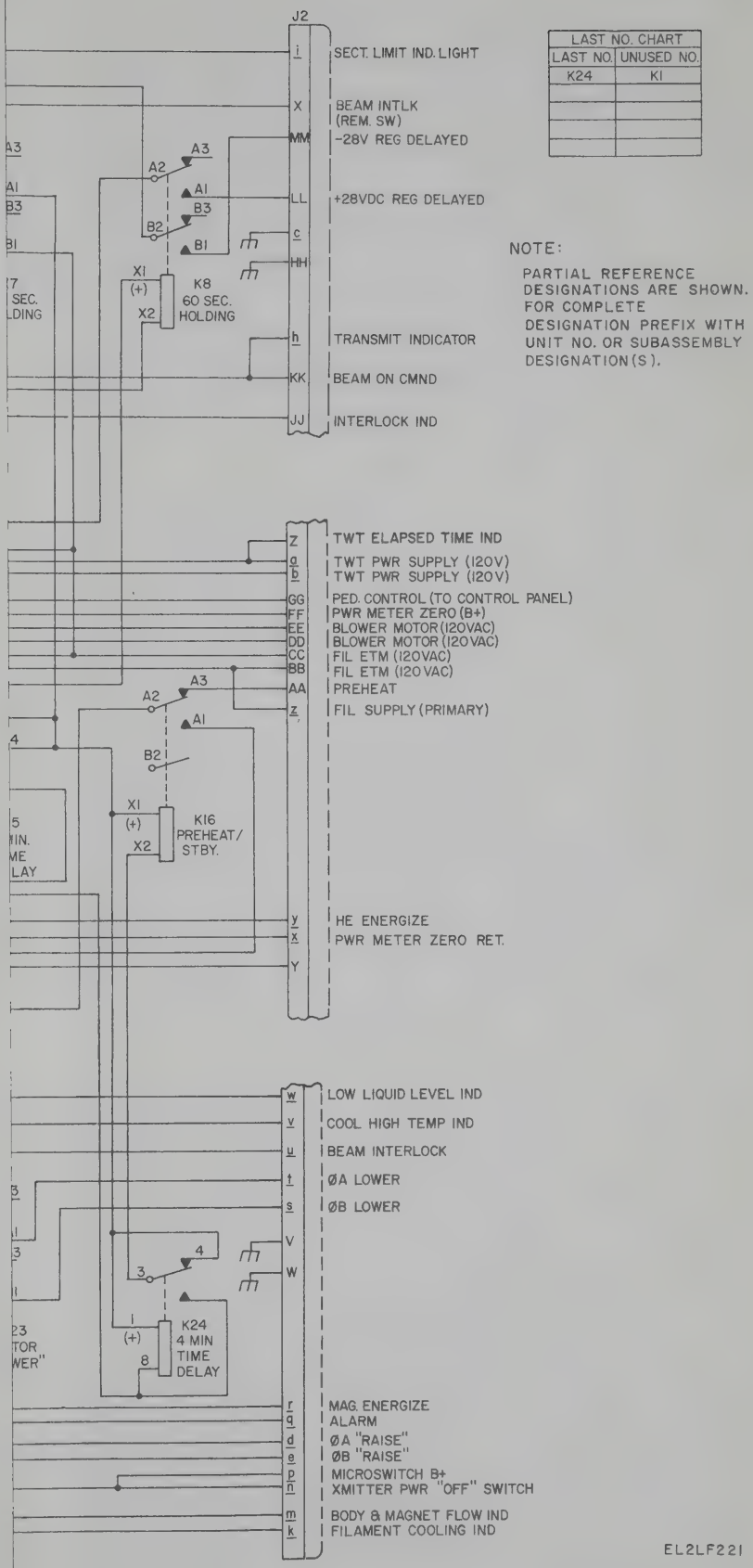


Figure FO 3-52.2: Transmitter control panel, schematic diagram (sheet 2 of 2).

EL2LF213



LAST NO. CHART	
LAST NO.	UNUSED NO.
K24	K1

NOTE:

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSEMBLY DESIGNATION(S).

EL2LF221

LAST NO. CHART	
LAST NO	UNUSED NO
K24	K1

NOTE:
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSEMBLY DESIGNATION(S).

J1
SECTOR LIMIT SWITCH — W
BEAM INTLK — V
−28V REG. — PP
+28VDC VIA SAFETY INTERLOCKS — NN
DUMMY LOAD INTERLOCK BYPASS — MM
CHASSIS GRD — HH
DUMMY LOAD OUTPUT — JJ

K2 SECTOR LIMIT
K3 DUMMY LOAD BYPASS
K4 TWT CONTACTOR
K5 INTERLOCK
K6 60 SEC. TIME DELAY
K7 60 SEC. HOLDING
K8 60 SEC. HOLDING

J2
L — SECT. LIMIT IND. LIGHT
X — BEAM INTLK (REM SW)
MM — −28V REG DELAYED
LL — +28VDC REG DELAYED
h — TRANSMIT INDICATOR
KK — BEAM ON CMND
JJ — INTERLOCK IND

SURGE PROT. RESISTOR — GG
SURGE PROT. RESISTOR — FF
120VAC BLOWER MOTOR — EE
XMTR PWR SWITCH "ON" — DD
REMOTE XMTR PWR. "ON" — CC
PWR METER ZERO (B+) — BB
REMOTE PWR METER ZERO (B+) — AA
U

K9 PEDESTAL CONTROL
K10 PEDESTAL CONTROL
K11 PEDESTAL CONTROL
K12 BLOWER MOTOR CONTACTOR
K13 FILAMENT CONTACTOR
K14 BLOWER MOTOR INTLK.
K15 4 MIN TIME DELAY
K16 PREHEAT/STBY

Z — TWT ELAPSED TIME IND
a — TWT PWR SUPPLY (120V)
b — TWT PWR SUPPLY (120V)
GG — PED. CONTROL (TO CONTROL PANEL)
FF — PWR METER ZERO (B+)
EE — BLOWER MOTOR (120VAC)
DD — BLOWER MOTOR (120 VAC)
CC — FIL ETM (120VAC)
BB — FIL ETM (120 VAC)
AA — PREHEAT
Z — FIL SUPPLY (PRIMARY)

REMOTE "KEY" SWITCH — Z
PWR METER ZERO RET — Y
REMOTE PWR METER ZERO RET — X
XMTR BEAM "ON" — W
REMOTE BEAM "ON" — V
120VAC BLOWER MOTOR — U
MICROSWITCH INTERLOCK — T
MAG. INTERLOCK — S

X — HE ENERGIZE
Y — PWR METER ZERO RET.

MOTOR SUPPLY ØA (120VAC) — r
MOTOR SUPPLY ØB (120VAC) — q
+28VDC REGULATED — p
REGULATED PSC — n
SHIELD GRD — m
SHIELD GRD — k
+28VDC UNREGULATED — j
REGULATED PSC — i
LOW LIQUID LEVEL INTERLOCK — h

K17 LOW LIQUID
K18 BODY & MAG. FLOW
K19 FLOW SWITCHES
K20 PROT CKT
K21 SYSTEM COOLANT HIGH TEMP.
K22 MOTOR "RAISE"
K23 MOTOR "LOWER"
K24 4 MIN TIME DELAY

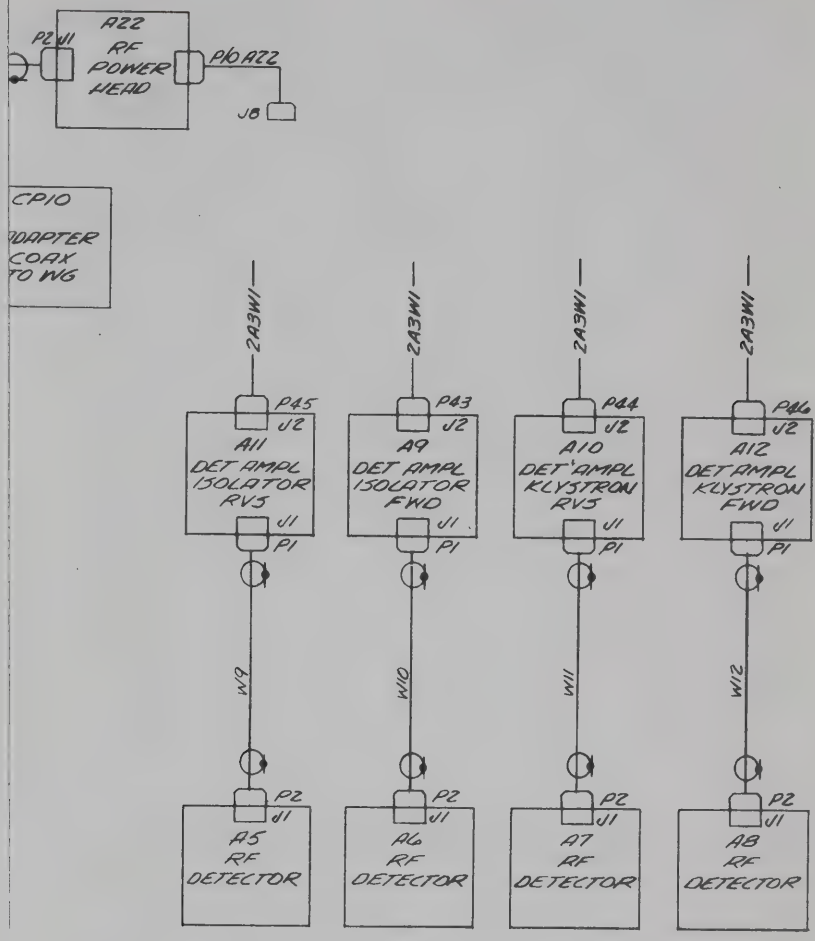
w — LOW LIQUID LEVEL IND
v — COOL HIGH TEMP IND
u — BEAM INTERLOCK
t — ØA LOWER
s — ØB LOWER

BODY & MAG. FLOW INTERLOCK — g
FLOW SWITCH INTERLOCK — f
PROT. CKT. RELAY — e
SYSTEM COOL HIGH TEMP. INTERLOCK — d
MOTOR CONTROL "RAISE" — c
REMOTE MOTOR CONTROL "RAISE" — b
MOTOR CONTROL "LOWER" — a
REMOTE MOTOR CONTROL "LOWER" — Z
ALARM — Y

r — MAG. ENERGIZE
q — ALARM
d — ØA "RAISE"
e — ØB "RAISE"
p — MICROSWITCH B+
n — XMITTER PWR "OFF" SWITCH
m — BODY & MAGNET FLOW IND
k — FILAMENT COOLING IND

EL2LF221

Figure FO 3-53. Relay box, schematic diagram.


A22
RF
POWER
HEAD
P2 J1
P1 P6 A22
J8
CP10
ADAPTER
COAX
TO WG
2A3W11
P45
J2
A11
DET AMPL
ISOLATOR
RV3
J1
P1
W9
P2
J1
A5
RF
DETECTOR
P43
J2
A9
DET AMPL
ISOLATOR
FWD
J1
P1
W10
P2
J1
A6
RF
DETECTOR
P44
J2
A10
DET AMPL
KLYSTRON
RV3
J1
P1
W11
P2
J1
A7
RF
DETECTOR
P46
J2
A12
DET AMPL
KLYSTRON
FWD
J1
P1
W12
P2
J1
A8
RF
DETECTOR

EL2LF222

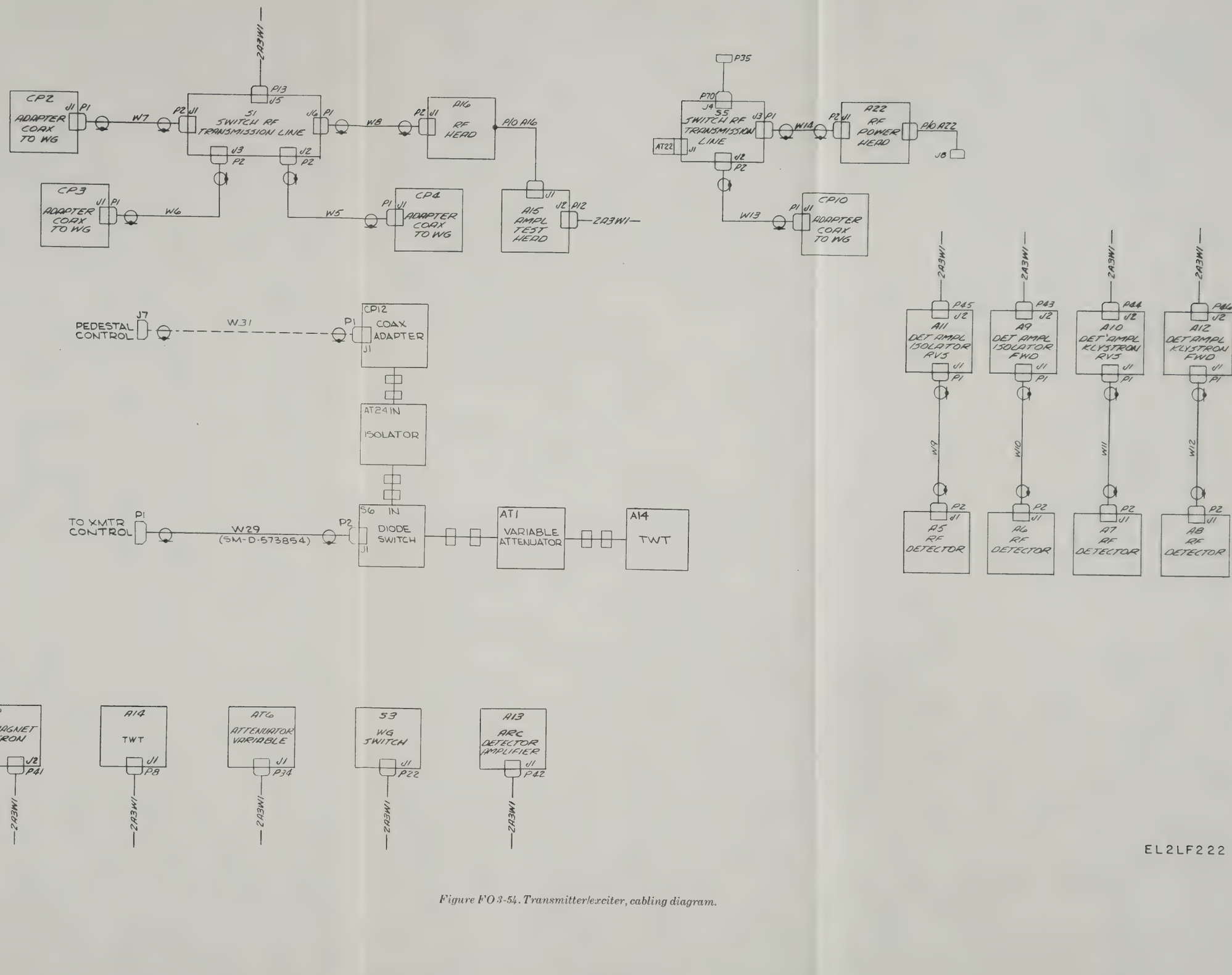
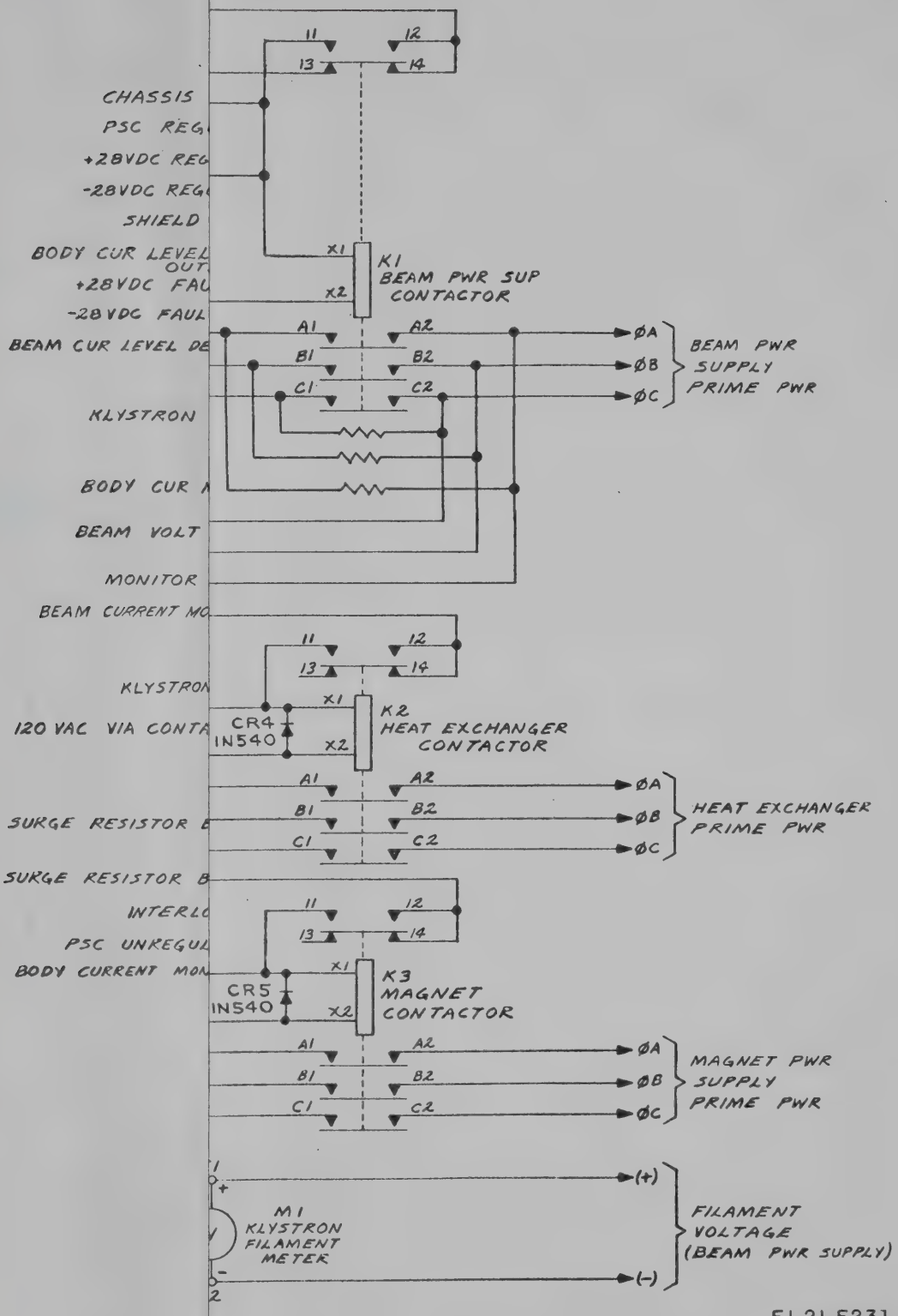


Figure FO 3-54. Transmitter/exciter, cabling diagram.


11
12
13
14
CHASSIS
PSC REG
+28VDC REG
-28VDC REG
SHIELD
BODY CUR LEVEL
OUT
+28VDC FAU
-28VDC FAUL
X1
X2
K1
BEAM PWR SUP
CONTACTOR
BEAM CUR LEVEL DE
A1
A2
B1
B2
C1
C2
ØA
ØB
ØC
BEAM PWR
SUPPLY
PRIME PWR
KLYSTRON
BODY CUR
BEAM VOLT
MONITOR
BEAM CURRENT MO
KLYSTRON
120 VAC VIA CONTA
CR4
IN540
K2
HEAT EXCHANGER
CONTACTOR
SURGE RESISTOR
HEAT EXCHANGER
PRIME PWR
SURGE RESISTOR B
INTERLO
PSC UNREGUL
BODY CURRENT MON
CR5
IN540
K3
MAGNET
CONTACTOR
MAGNET PWR
SUPPLY
PRIME PWR
M1
KLYSTRON
FILAMENT
METER
(+)
(-)
FILAMENT
VOLTAGE
(BEAM PWR SUPPLY)

EL2LF231

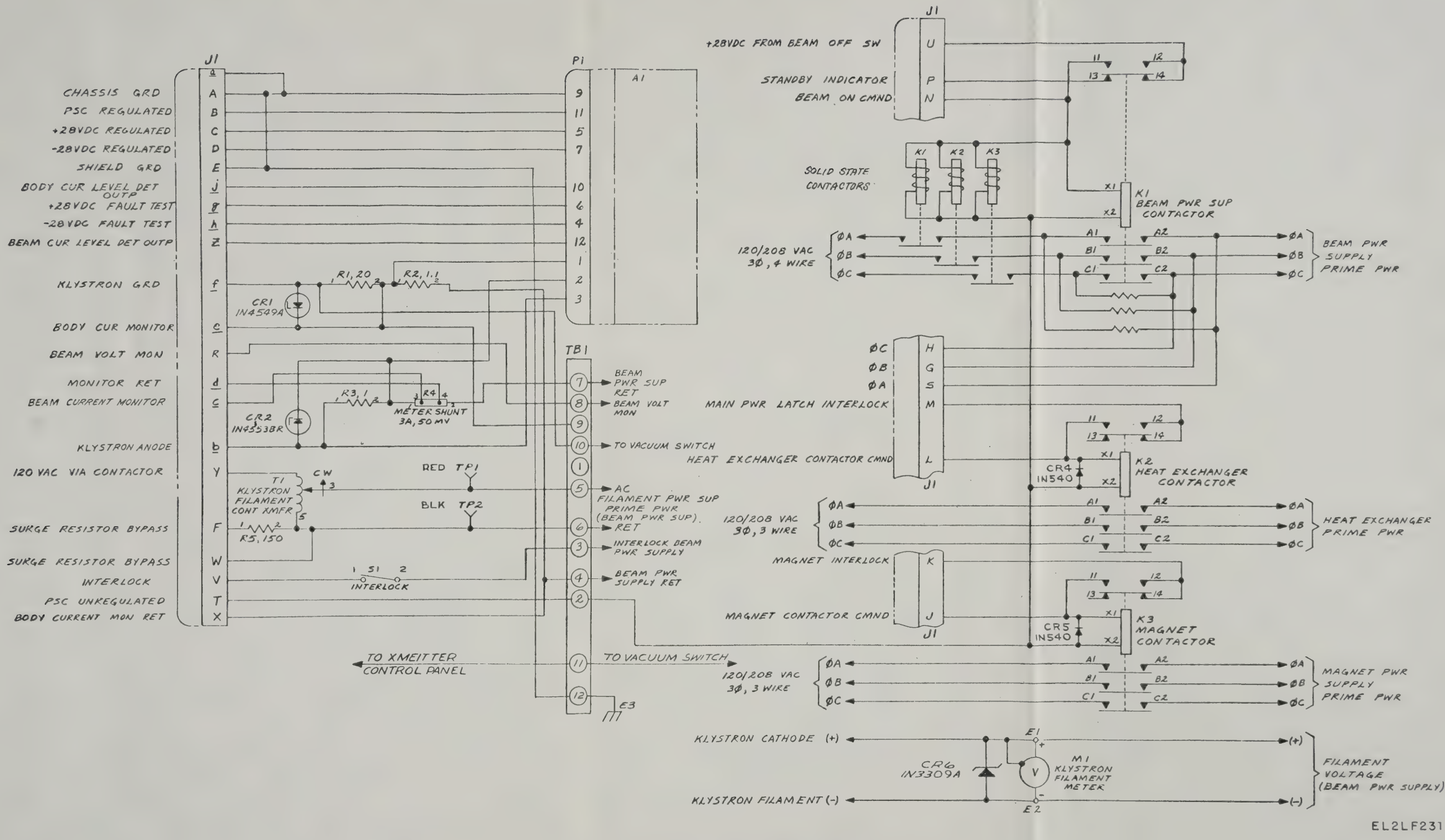
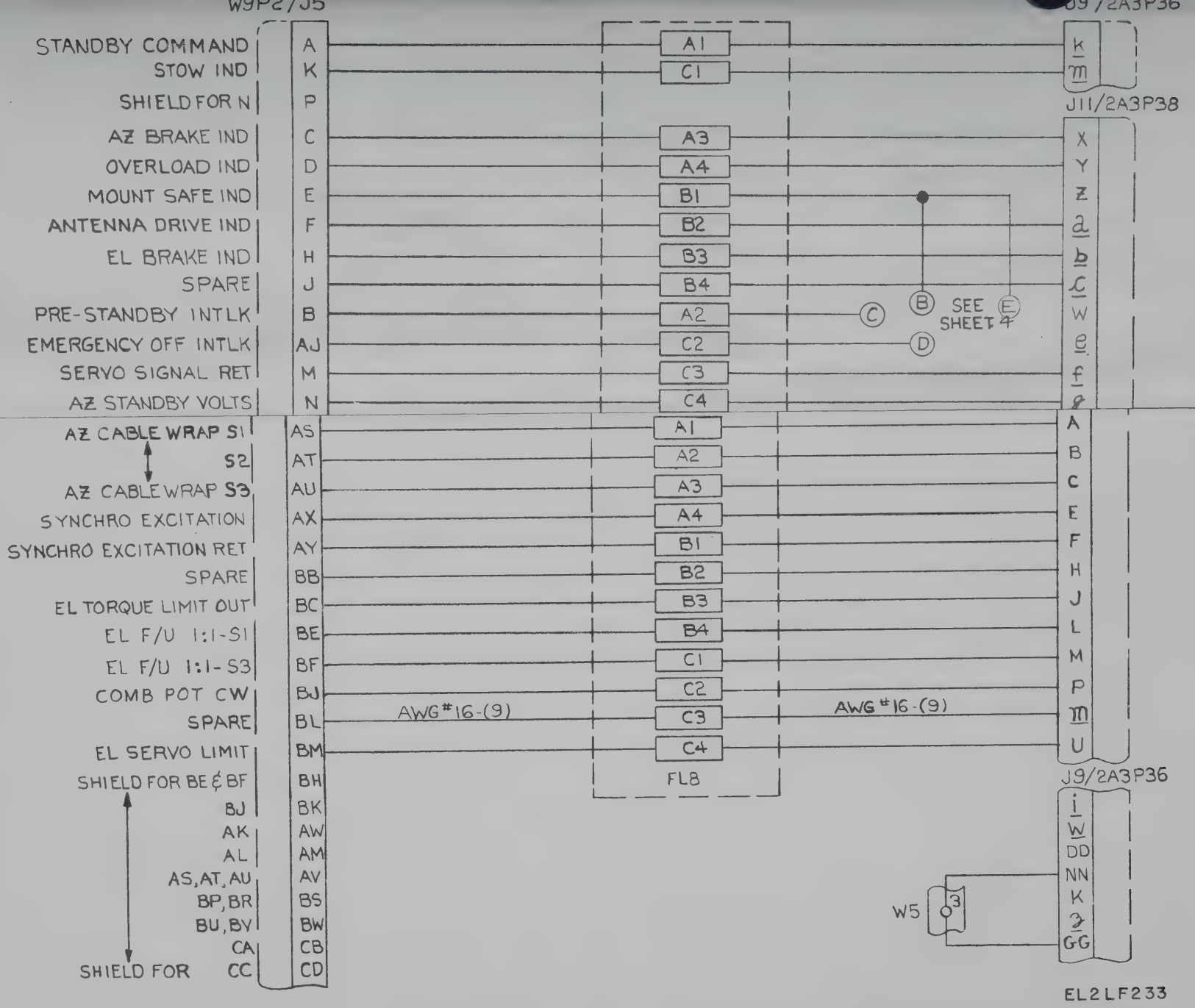


Figure FO 3-55. High voltage cage, interconnection diagram.


W9P2/J5
STANDBY COMMAND
STOW IND
SHIELD FOR N
AZ BRAKE IND
OVERLOAD IND
MOUNT SAFE IND
ANTENNA DRIVE IND
EL BRAKE IND
SPARE
PRE-STANDBY INTLK
EMERGENCY OFF INTLK
SERVO SIGNAL RET
AZ STANDBY VOLTS
A
K
P
C
D
E
F
H
J
B
AJ
M
N
A1
C1
A3
A4
B1
B2
B3
B4
A2
C2
C3
C4
J9/2A3P36
J11/2A3P38
k
m
X
Y
Z
a
b
c
W
e
f
g
SEE SHEET 4
AZ CABLE WRAP S1
S2
AZ CABLE WRAP S3
SYNCHRO EXCITATION
SYNCHRO EXCITATION RET
SPARE
EL TORQUE LIMIT OUT
EL F/U 1:1-S1
EL F/U 1:1-S3
COMB POT CW
SPARE
EL SERVO LIMIT
SHIELD FOR BE & BF
BJ
AK
AL
AS, AT, AU
BP, BR
BU, BV
CA
SHIELD FOR CC
AS
AT
AU
AX
AY
BB
BC
BE
BF
BJ
BL
BM
BH
BK
AW
AM
AV
BS
BW
CB
CD
AWG #16-(9)
AWG #16-(9)
FL8
A
B
C
E
F
H
J
L
M
P
m
U
i
W
DD
NN
K
3
GG
W5
3
EL2LF233

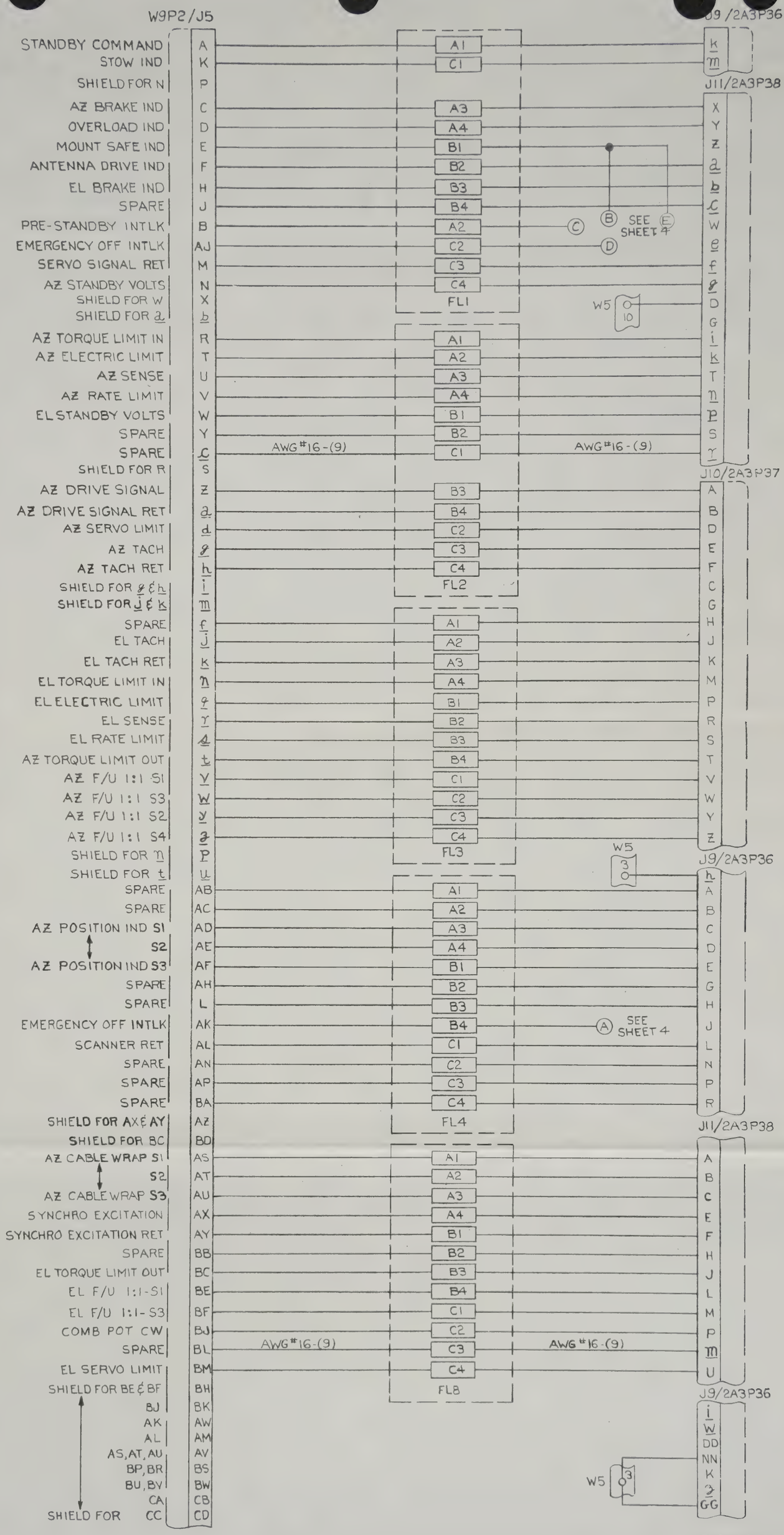
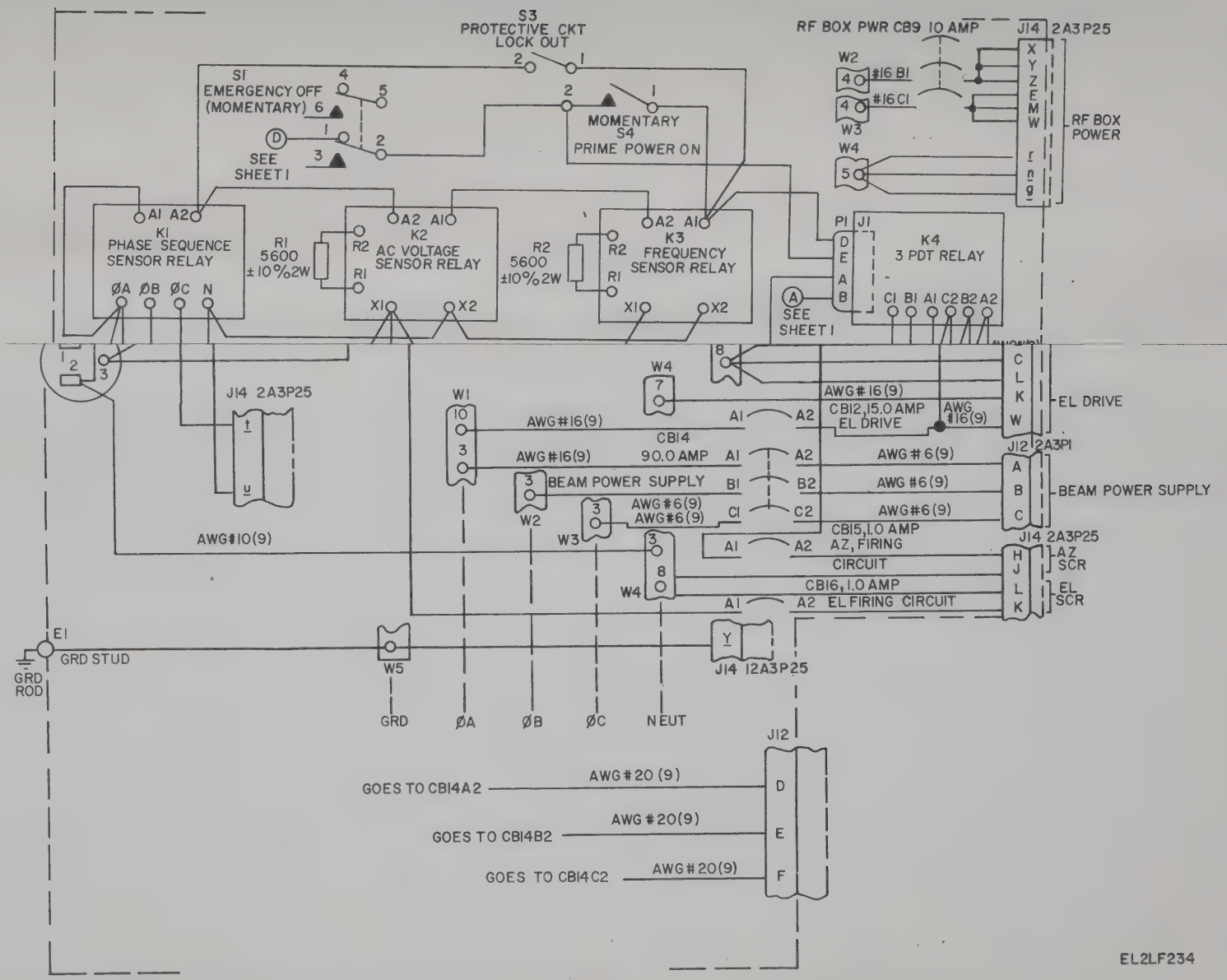
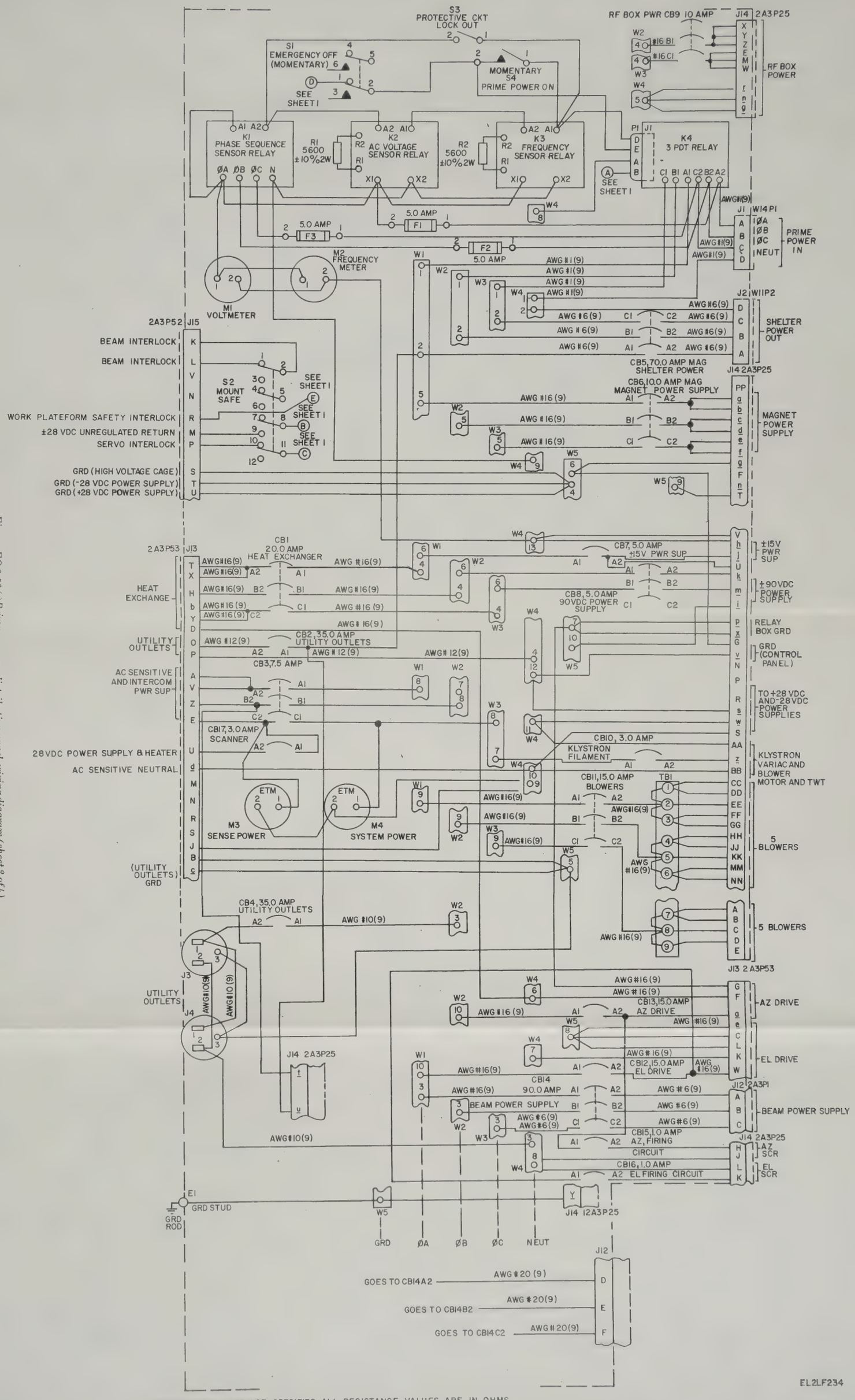


Figure FO 8-56. ① Primary power distribution panel, wiring diagram (sheet 1 of 4).



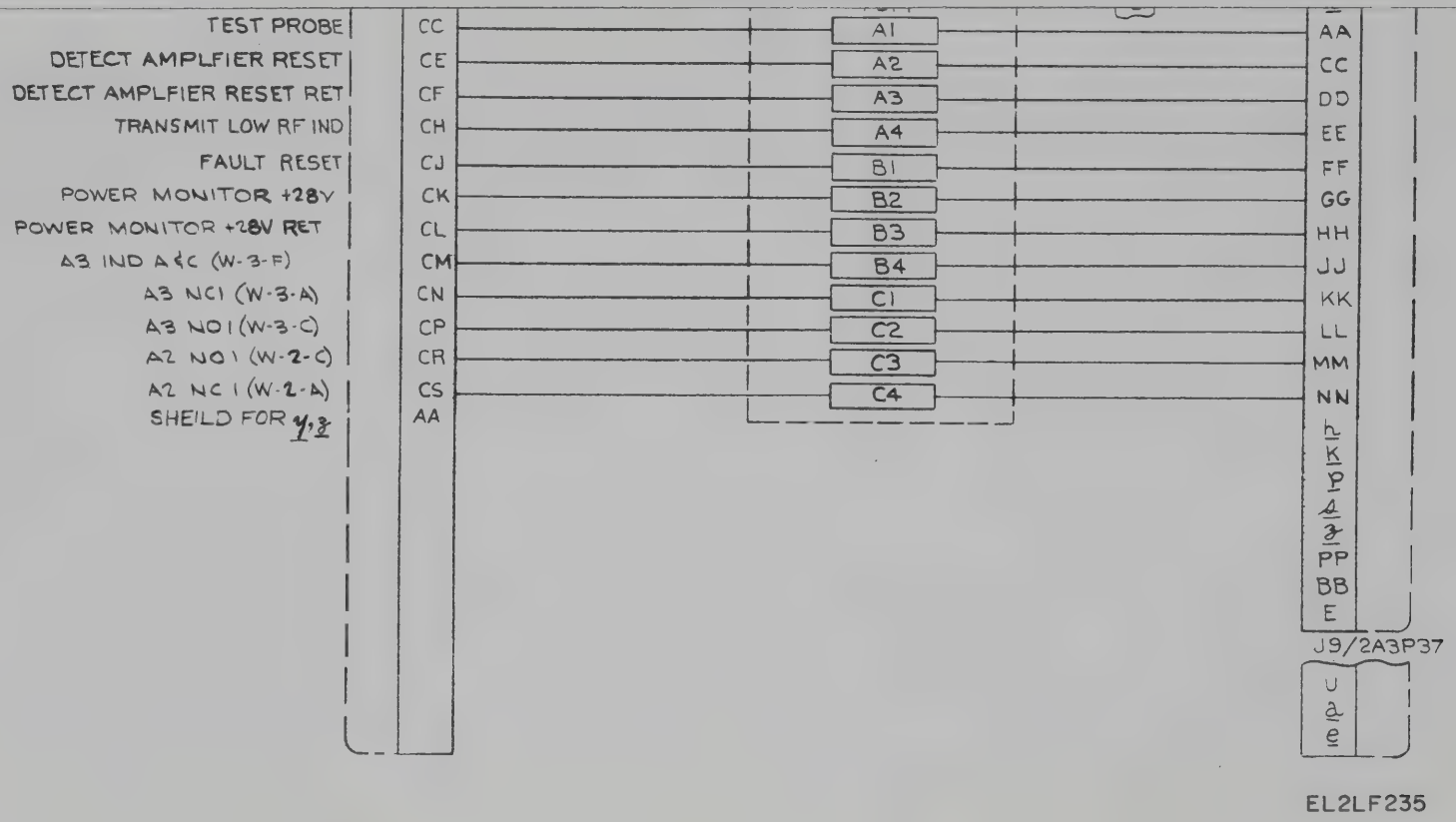
NOTE: UNLESS OTHERWISE SPECIFIED, ALL RESISTANCE VALUES ARE IN OHMS.



NOTE: UNLESS OTHERWISE SPECIFIED, ALL RESISTANCE VALUES ARE IN OHMS.

Figure FO 3-56.(3) Primary power distribution panel, wiring diagram (sheet 2 of 4).

sheet 3 of 4).


TEST PROBE
DETECT AMPLFIER RESET
DETECT AMPLFIER RESET RET
TRANSMIT LOW RF IND
FAULT RESET
POWER MONITOR +28V
POWER MONITOR +28V RET
A3 IND A&C (W-3-F)
A3 NC1 (W-3-A)
A3 NO1 (W-3-C)
A2 NO1 (W-2-C)
A2 NC1 (W-2-A)
SHEILD FOR Y,Z
CC
CE
CF
CH
CJ
CK
CL
CM
CN
CP
CR
CS
AA
A1
A2
A3
A4
B1
B2
B3
B4
C1
C2
C3
C4
AA
CC
DD
EE
FF
GG
HH
JJ
KK
LL
MM
NN
PP
BB
E
J9/2A3P37
EL2LF235

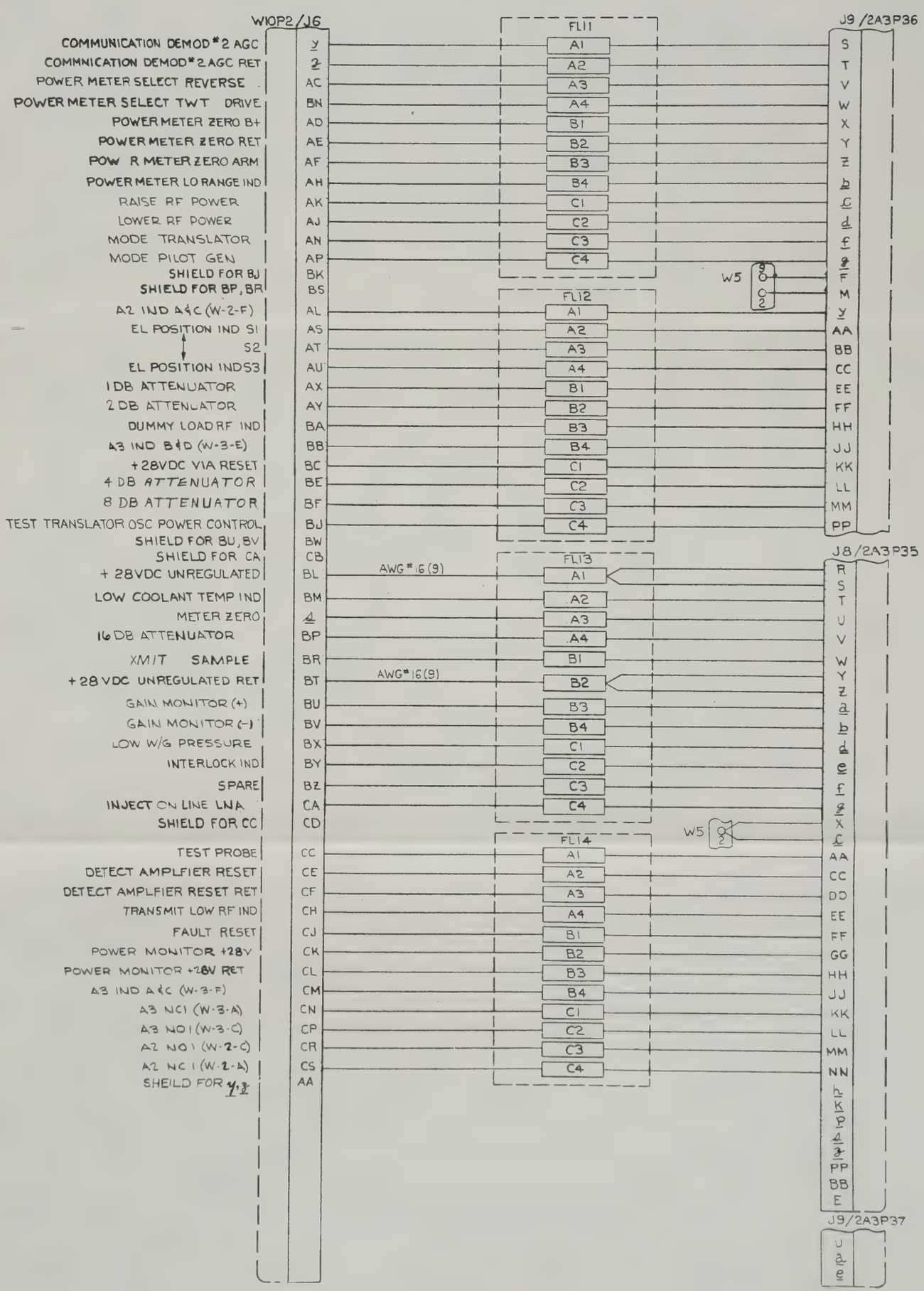
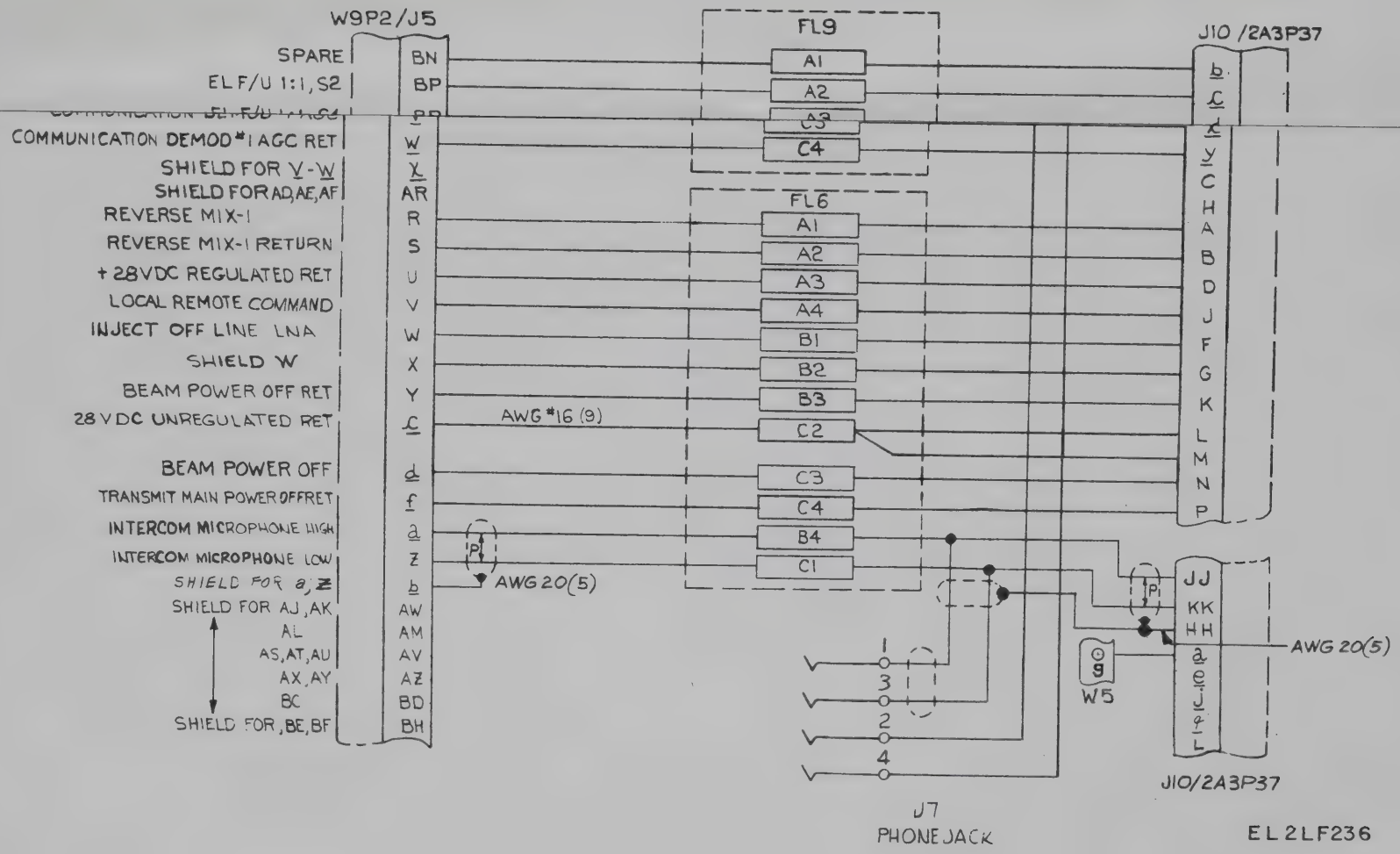


Figure FO 8-56. ③ Primary power distribution panel, wiring diagram (sheet 8 of 4).


W9P2/J5
SPARE
EL F/U 1:1, S2
COMMUNICATION DEMOD *1 AGC RET
SHIELD FOR V-W
SHIELD FOR AD, AE, AF
REVERSE MIX-1
REVERSE MIX-1 RETURN
+28VDC REGULATED RET
LOCAL REMOTE COMMAND
INJECT OFF LINE LNA
SHIELD W
BEAM POWER OFF RET
28 V DC UNREGULATED RET
BEAM POWER OFF
TRANSMIT MAIN POWER OFF RET
INTERCOM MICROPHONE HIGH
INTERCOM MICROPHONE LOW
SHIELD FOR a, Z
SHIELD FOR AJ, AK
AL
AS, AT, AU
AX, AY
BC
SHIELD FOR, BE, BF
BN
BP
W
X
AR
R
S
U
V
W
X
Y
C
d
f
a
Z
b
AW
AM
AV
AZ
BD
BH
FL9
A1
A2
A3
C4
FL6
A1
A2
A3
A4
B1
B2
B3
C2
C3
C4
B4
C1
AWG *16 (9)
AWG 20(5)
P1
J10 /2A3P37
b
C
d
V
C
H
A
B
D
J
F
G
K
L
M
N
P
JJ
KK
HH
a
Z
b
f
L
AWG 20(5)
W5
J10/2A3P37
1
3
2
4
J7
PHONE JACK
EL 2LF236

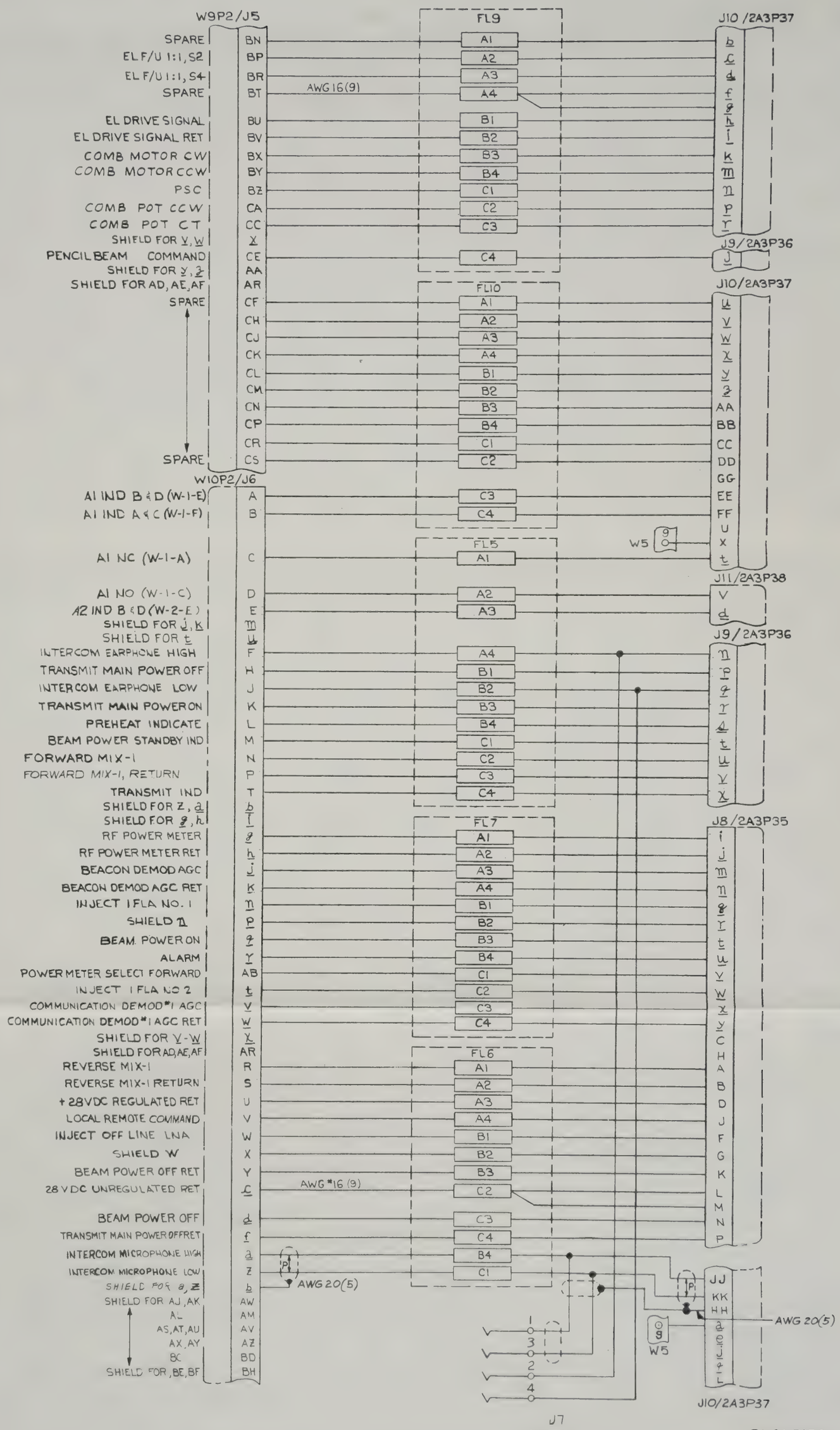
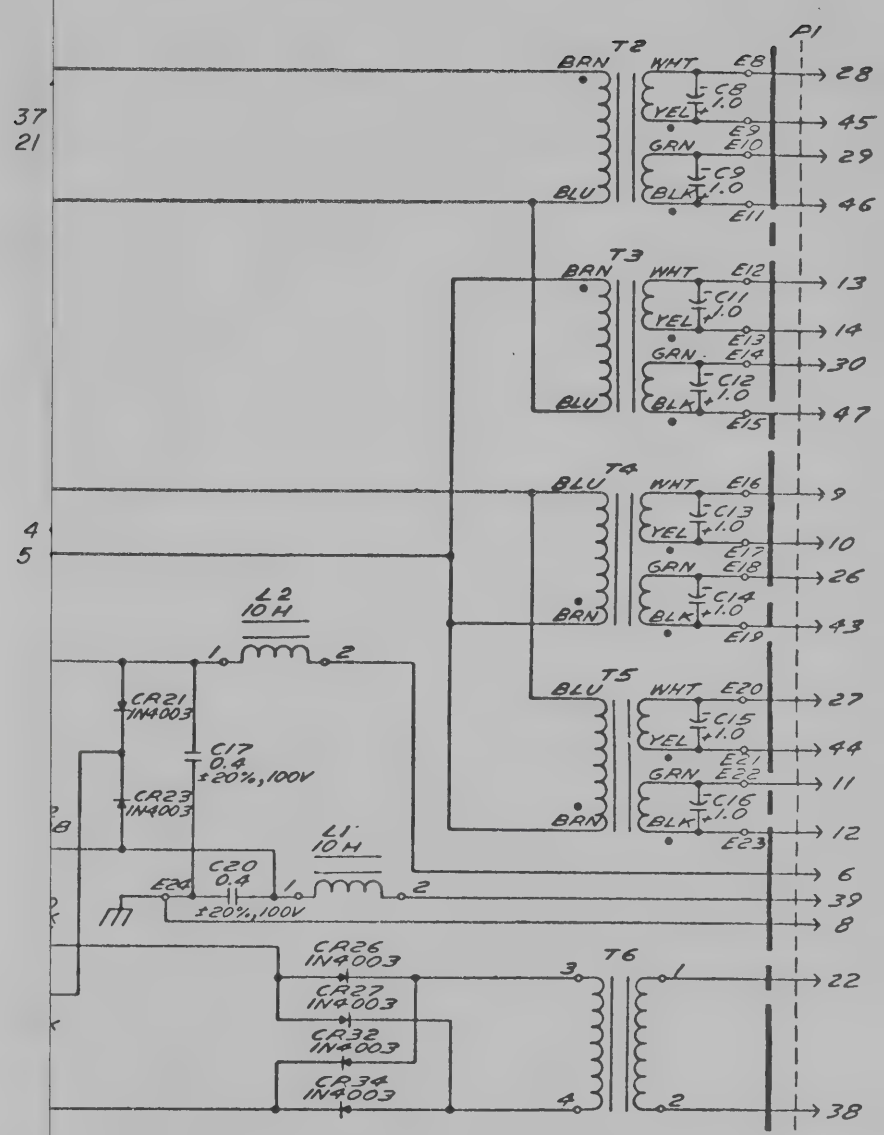
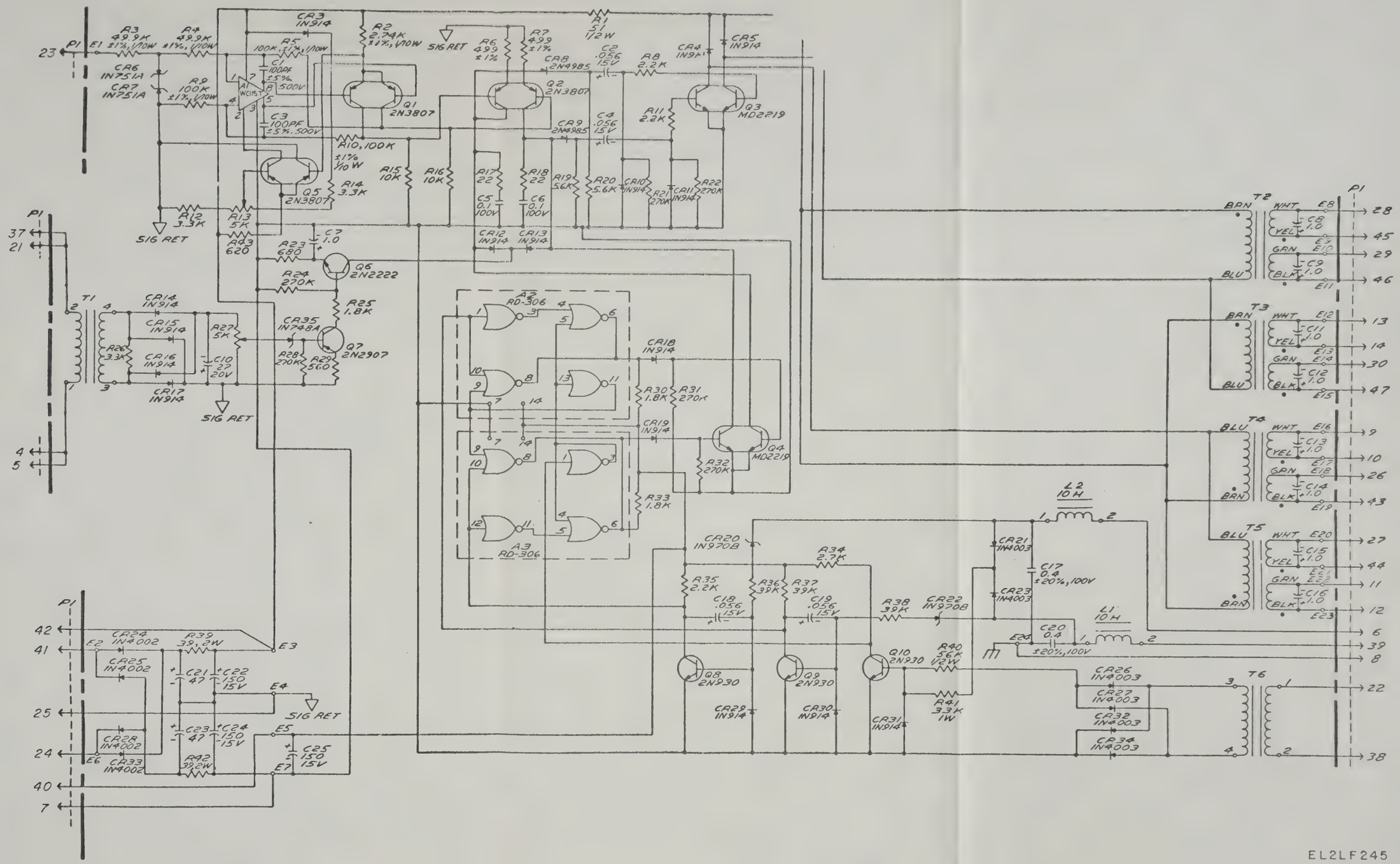


Figure FO 3-56. ① Primary power distribution panel, wiring diagram (sheet 4 of 4).


P1
T2
BRN
WHT
E8
C8 1.0
YEL
E9
GRN
E10
C9 1.0
BLK
BLU
E11
28
45
29
46
37
21
T3
E12
C11 1.0
E13
E14
C12 1.0
E15
13
14
30
47
T4
E16
C13 1.0
E17
E18
C14 1.0
E19
9
10
26
43
4
5
T5
E20
C15 1.0
E21
E22
C16 1.0
E23
27
44
11
12
L2
10 H
CR21
1N4003
C17
0.4
±20%, 100V
CR23
1N4003
L1
10 H
C20
0.4
E24
±20%, 100V
6
39
8
CR26
1N4003
CR27
1N4003
CR32
1N4003
CR34
1N4003
T6
22
38

EL2LF245

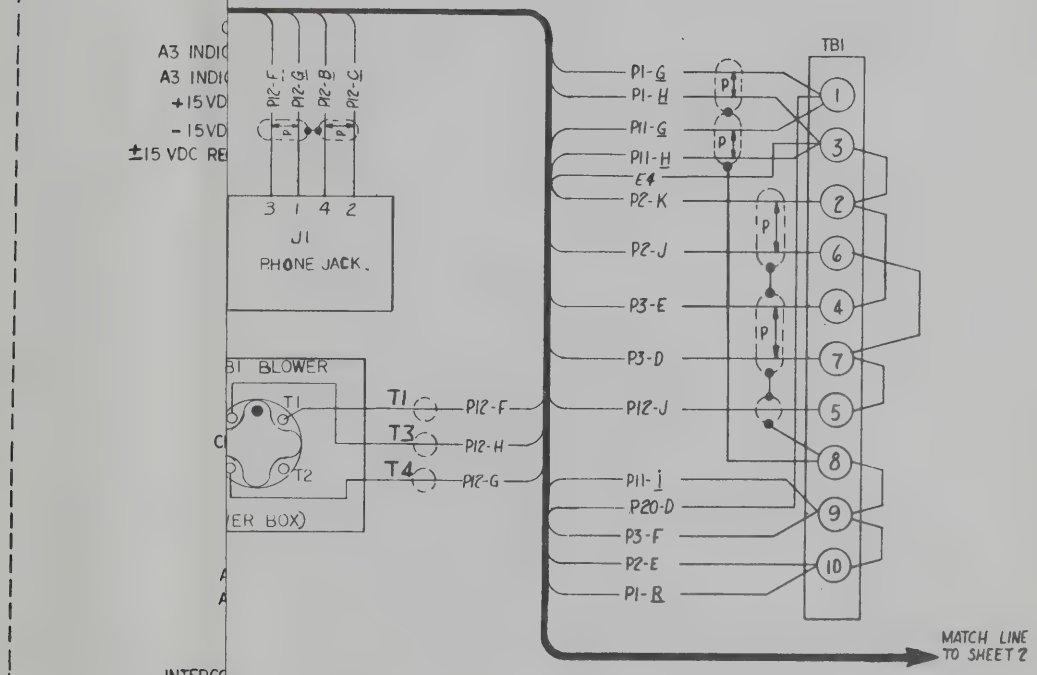


EL2LF245

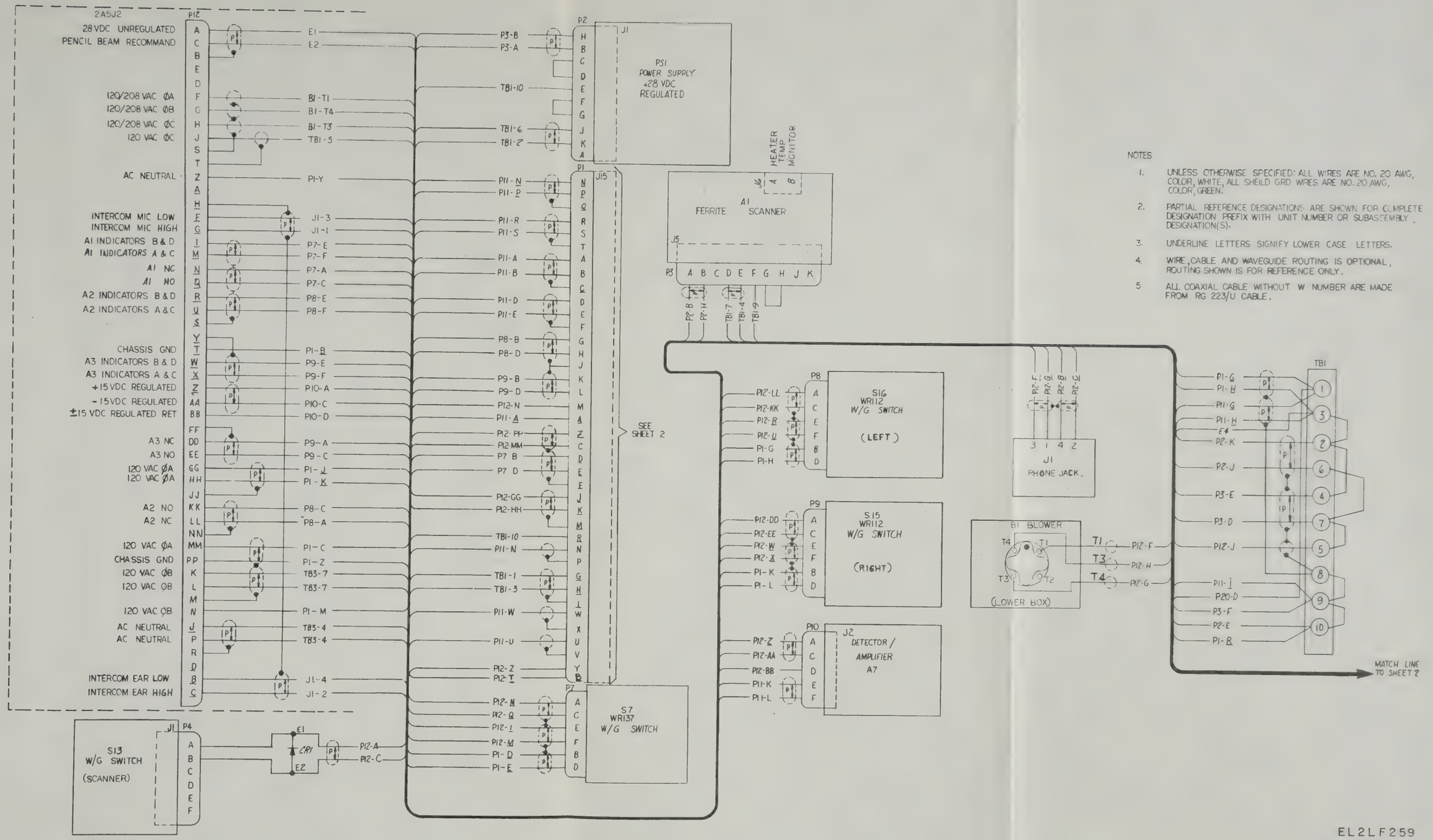
Figure FO 3-57. Dc power amplifier component board, schematic diagram.

NOTES

1. UNLESS OTHERWISE SPECIFIED: ALL WIRES ARE NO. 20 AWG, COLOR, WHITE, ALL SHEILD GRD WIRES ARE NO. 20 AWG, COLOR, GREEN.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S).
3. UNDERLINE LETTERS SIGNIFY LOWER CASE LETTERS.
4. WIRE, CABLE AND WAVEGUIDE ROUTING IS OPTIONAL, ROUTING SHOWN IS FOR REFERENCE ONLY.
5. ALL COAXIAL CABLE WITHOUT W NUMBER ARE MADE FROM RG 223/U CABLE.



EL2LF259

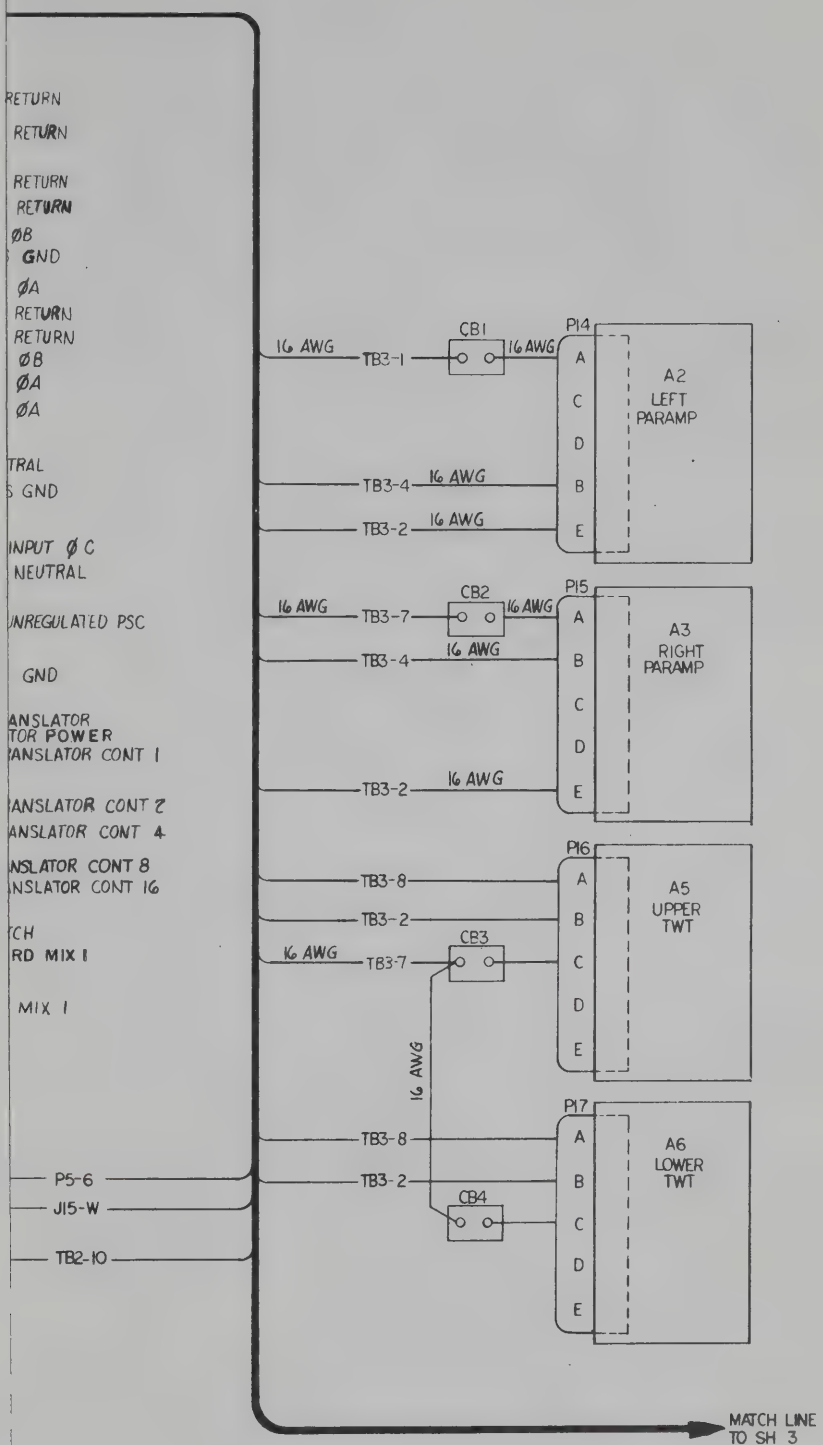


NOTES

1. UNLESS OTHERWISE SPECIFIED: ALL WIRES ARE NO. 20 AWG, COLOR, WHITE, ALL SHEILD GRD WIRES ARE NO. 20 AWG, COLOR, GREEN.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S).
3. UNDERLINE LETTERS SIGNIFY LOWER CASE LETTERS.
4. WIRE, CABLE AND WAVEGUIDE ROUTING IS OPTIONAL, ROUTING SHOWN IS FOR REFERENCE ONLY.
5. ALL COAXIAL CABLE WITHOUT W NUMBER ARE MADE FROM RG 223/U CABLE.

EL2LF259

Figure FO 3-58. ① Rf box, schematic diagram (sheet 1 of 6).


RETURN
RETURN
RETURN
RETURN
ØB
GND
ØA
RETURN
RETURN
ØB
ØA
ØA
TRAL
GND
INPUT Ø C
NEUTRAL
UNREGULATED PSC
GND
ANSLATOR
TOR POWER
ANSLATOR CONT 1
ANSLATOR CONT 2
ANSLATOR CONT 4
NSLATOR CONT 8
NSLATOR CONT 16
CH
RD MIX 1
MIX 1
P5-6
J15-W
TB2-10
16 AWG
TB3-1
CB1
16 AWG
P14
A
C
D
B
E
A2
LEFT
PARAMP
TB3-4
16 AWG
TB3-2
16 AWG
16 AWG
TB3-7
CB2
16 AWG
P15
A
B
C
D
E
A3
RIGHT
PARAMP
TB3-4
16 AWG
TB3-2
16 AWG
TB3-8
P16
A
B
C
D
E
A5
UPPER
TWT
TB3-2
16 AWG
TB3-7
CB3
16 AWG
TB3-8
P17
A
B
C
D
E
A6
LOWER
TWT
TB3-2
CB4
MATCH LINE
TO SH 3

EL2LF260

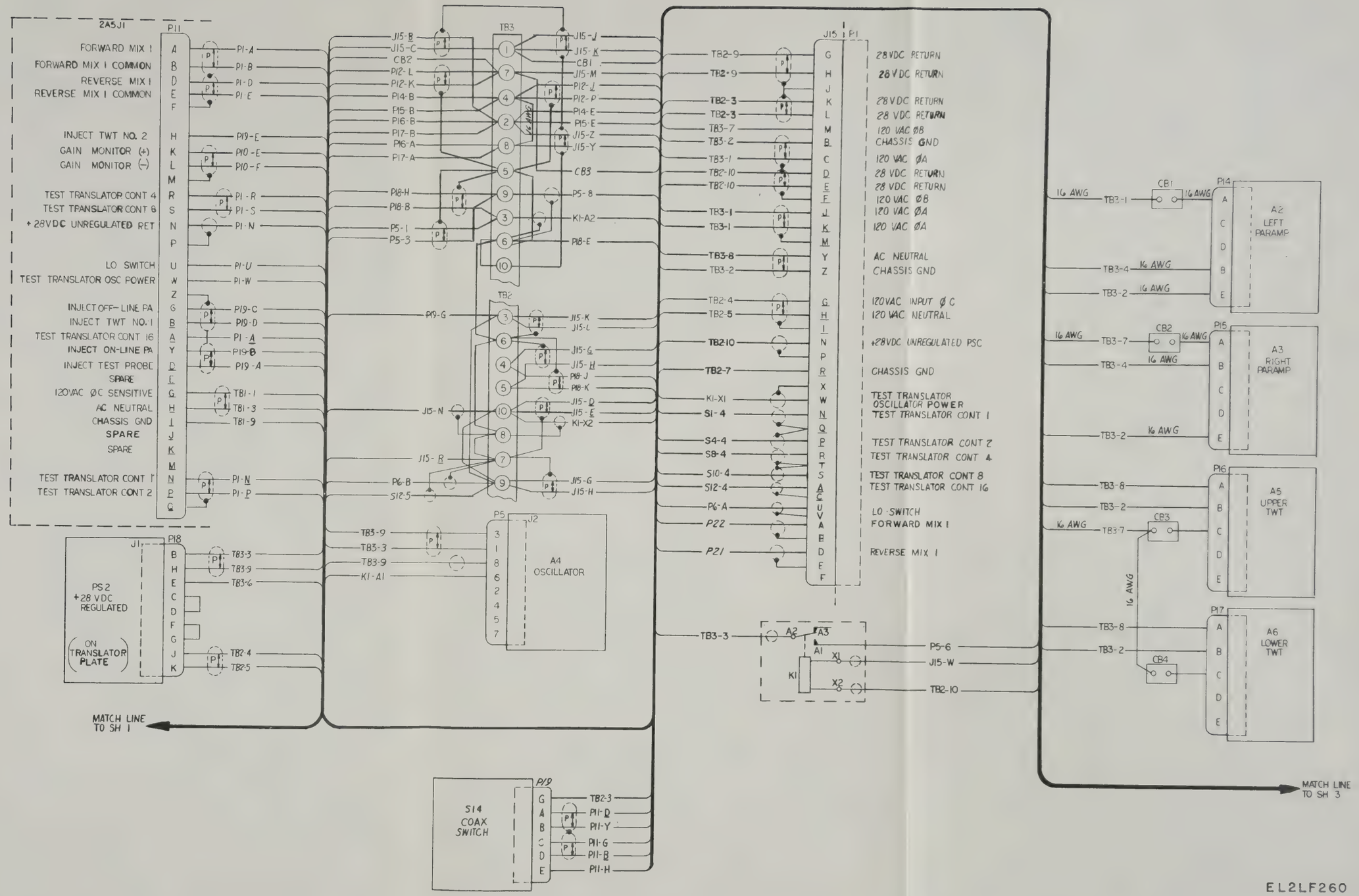
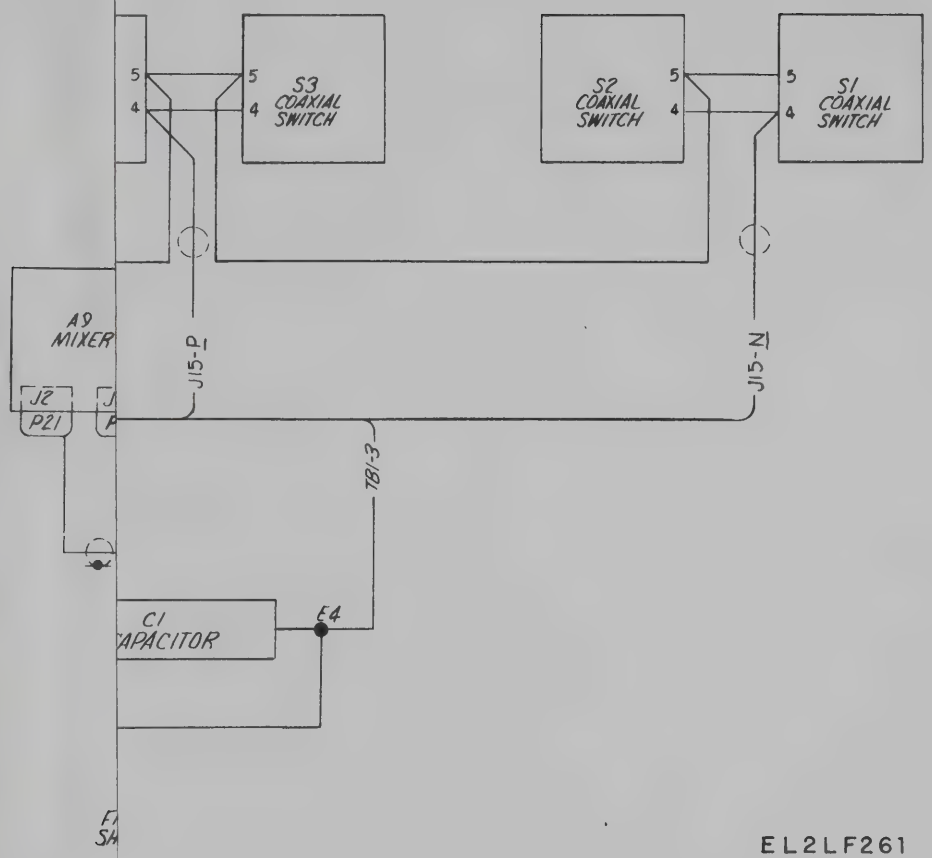
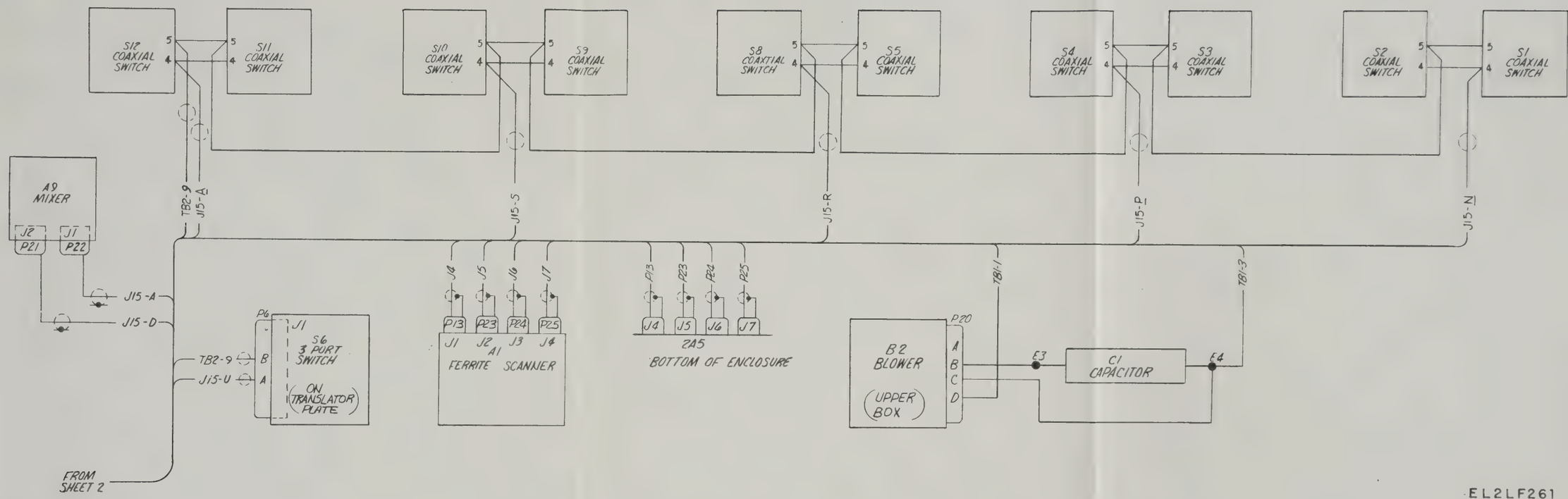


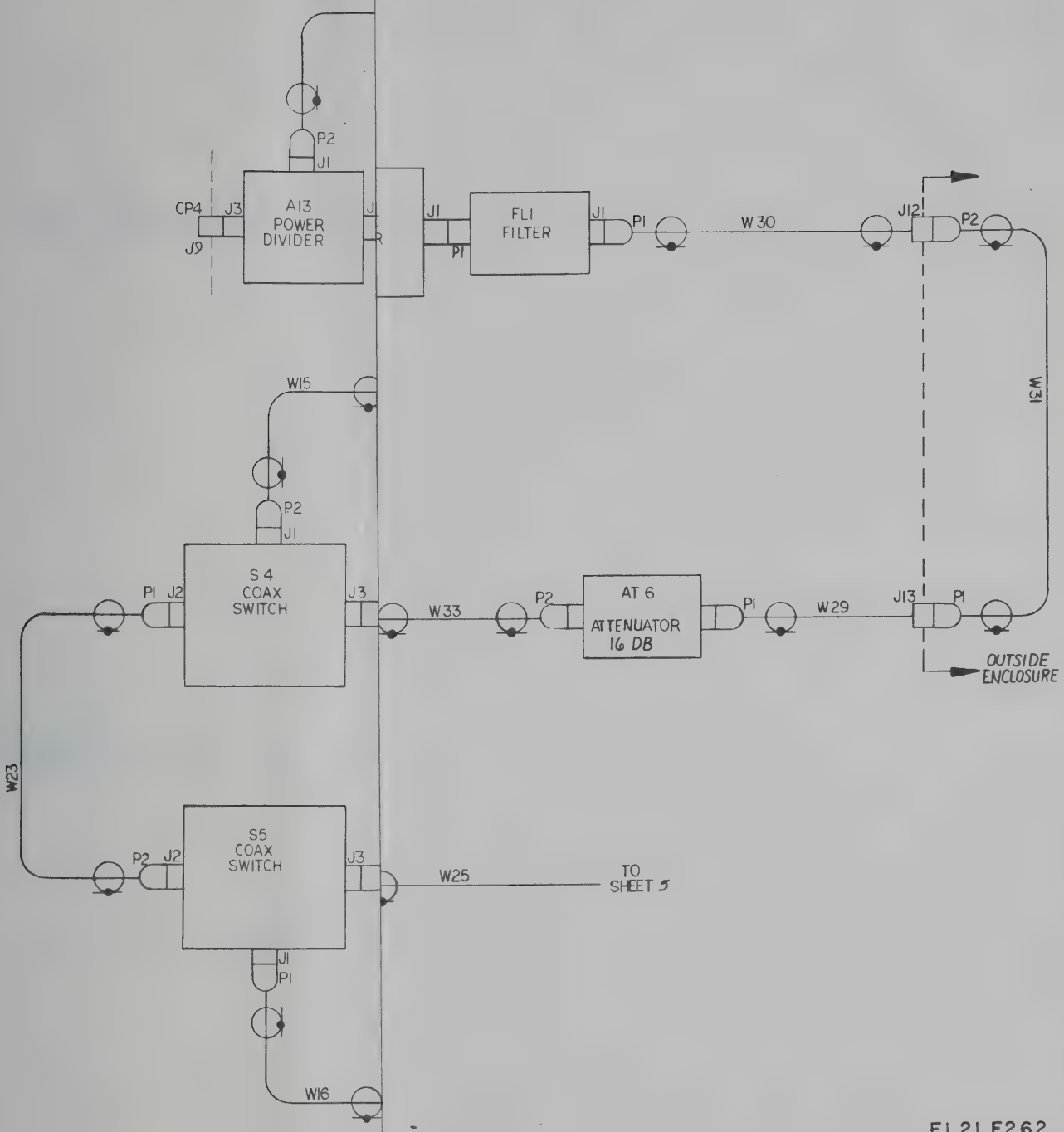
Figure FO 3-58.②Rf box, schematic diagram (sheet 2 of 6).


5
4
S3
COAXIAL
SWITCH
5
4
S2
COAXIAL
SWITCH
5
4
S1
COAXIAL
SWITCH
A9
MIXER
J2
P21
J15-P
J15-N
781-3
C1
CAPACITOR
E4
EL2LF261



EL2LF261

Figure FO 3-58.③Rf box, schematic diagram (sheet 3 of 6).


P2
J1
CP4
J3
J9
A13
POWER
DIVIDER
J1
P1
FL1
FILTER
J1
P1
W30
J12
P2
W31
W15
P2
J1
P1
J2
S4
COAX
SWITCH
J3
W33
P2
AT 6
ATTENUATOR
16 DB
P1
W29
J13
P1
OUTSIDE
ENCLOSURE
W23
P2
J2
S5
COAX
SWITCH
J3
W25
TO
SHEET 5
J1
P1
W16

EL2LF262

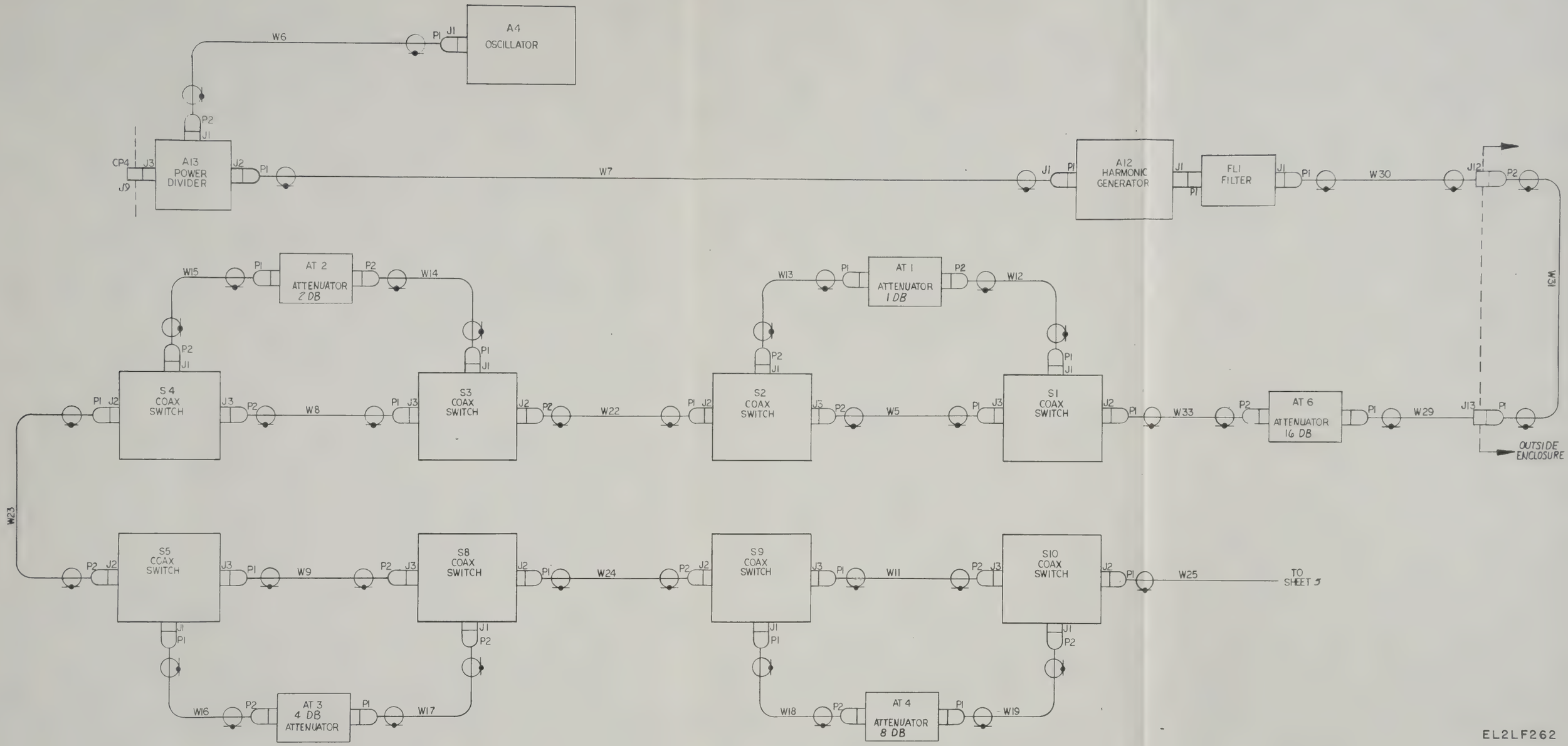
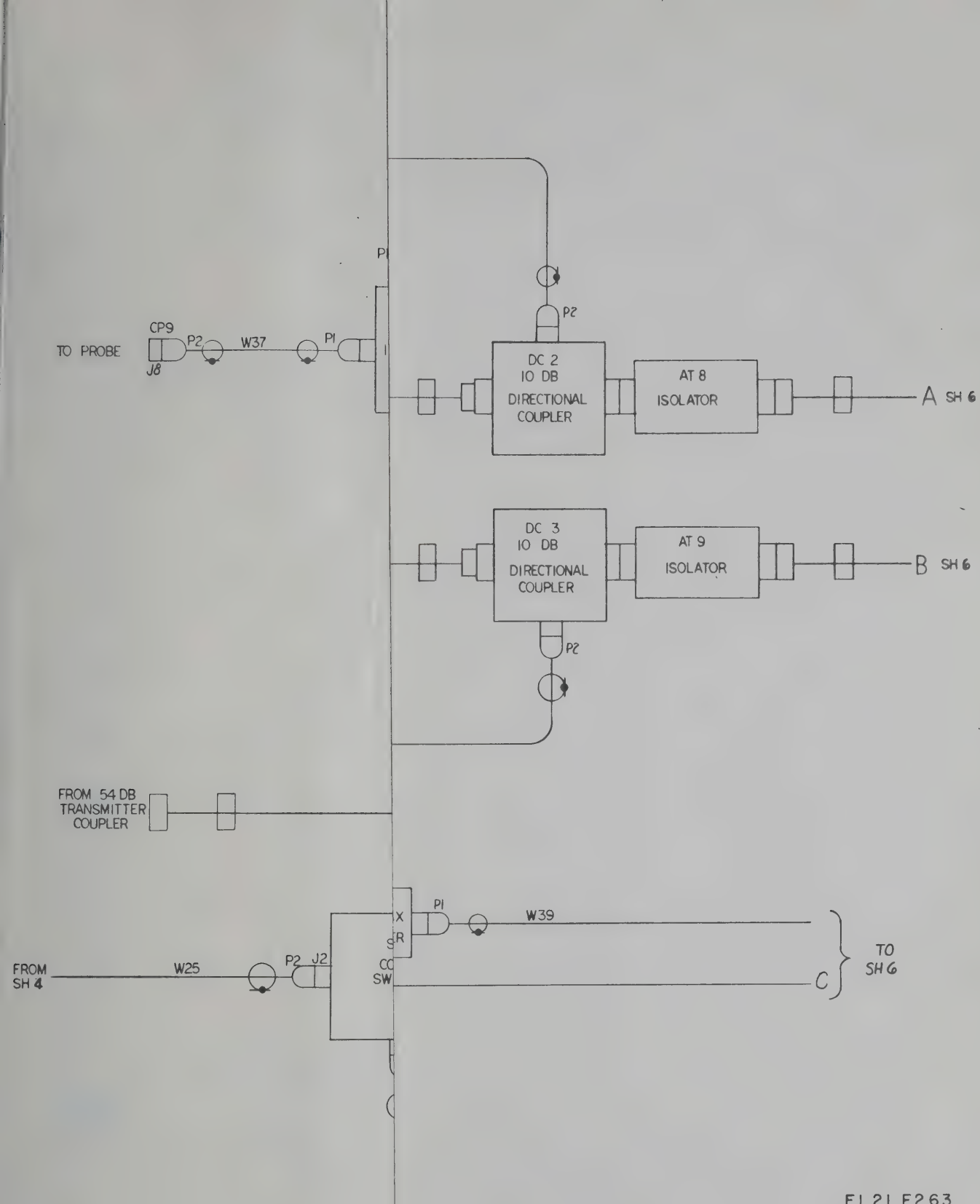


Figure FO 3-58. ④ Rf box, schematic diagram (sheet 4 of 6).


TO PROBE
CP9
J8
P2
W37
P1
P1
P2
DC 2
10 DB
DIRECTIONAL
COUPLER
AT 8
ISOLATOR
A SH 6
DC 3
10 DB
DIRECTIONAL
COUPLER
AT 9
ISOLATOR
B SH 6
P2
FROM 54 DB
TRANSMITTER
COUPLER
P1
W39
TO
SH 6
C
FROM
SH 4
W25
P2
J2
SW

EL2LF263

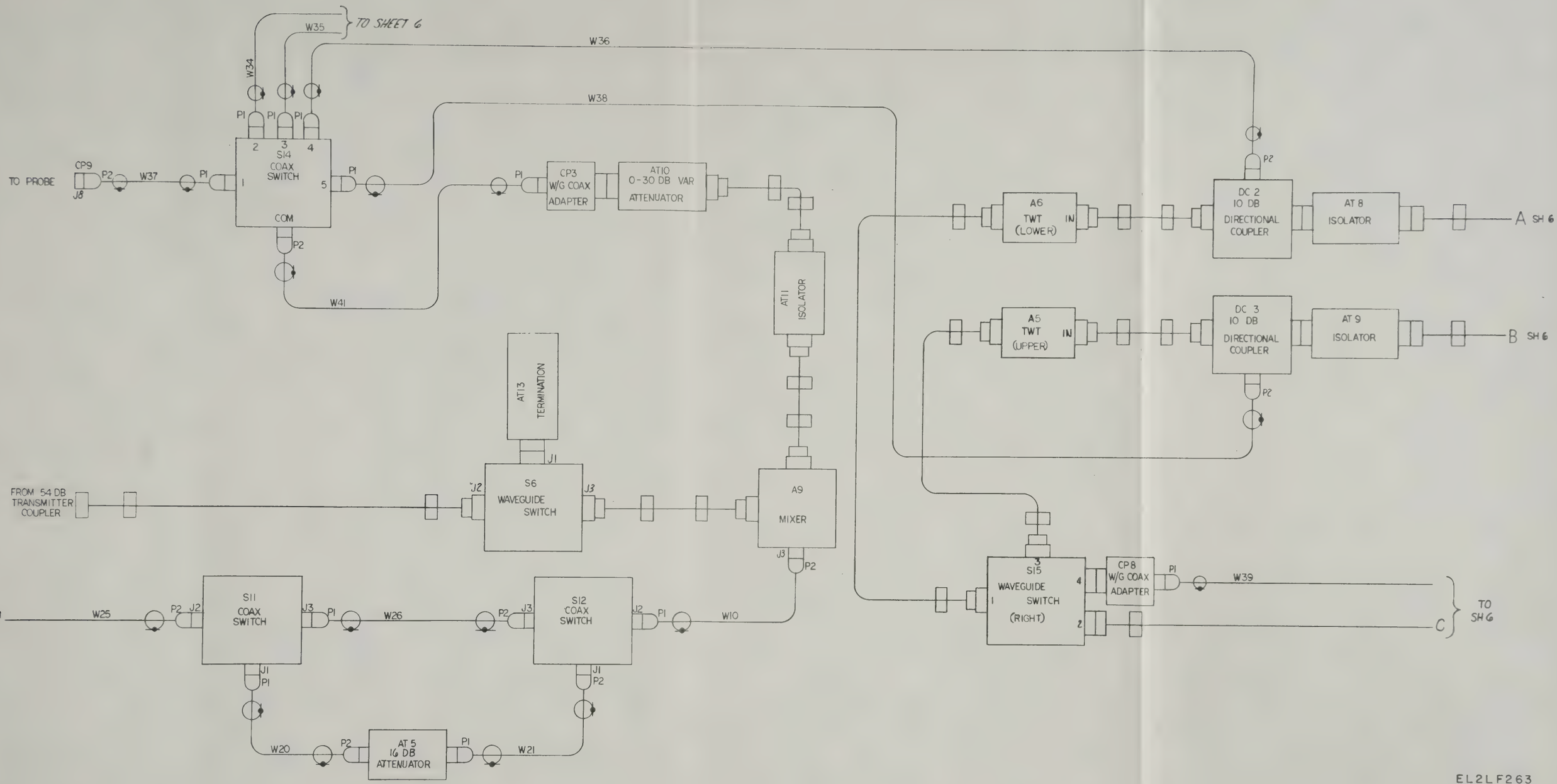
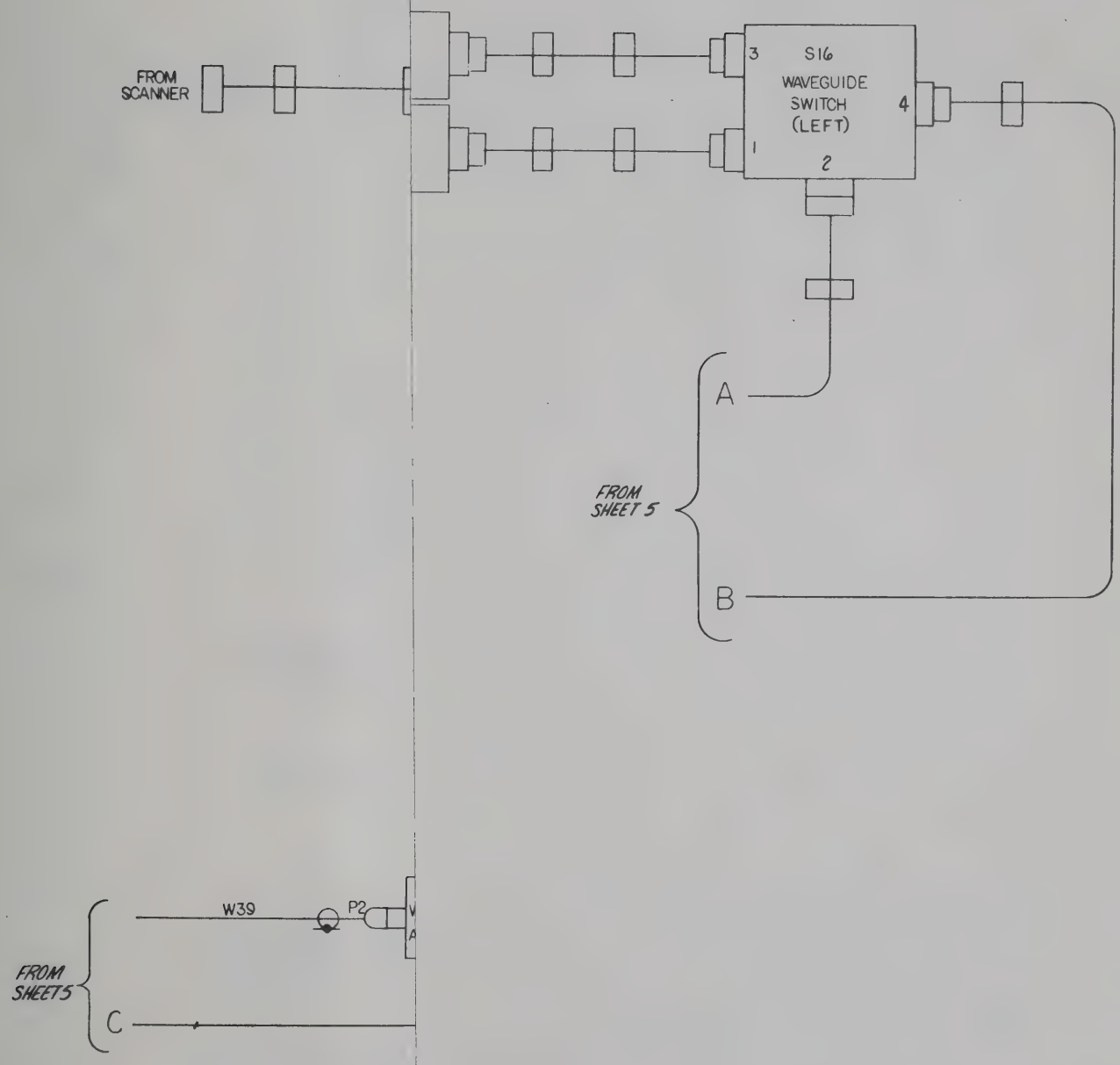


Figure FO 3-58. ⑤ Rf box, schematic diagram (sheet 5 of 6).


FROM SCANNER
S16
WAVEGUIDE SWITCH (LEFT)
3
4
1
2
A
FROM SHEET 5
B
W39
P2
FROM SHEETS
C

EL2LF264

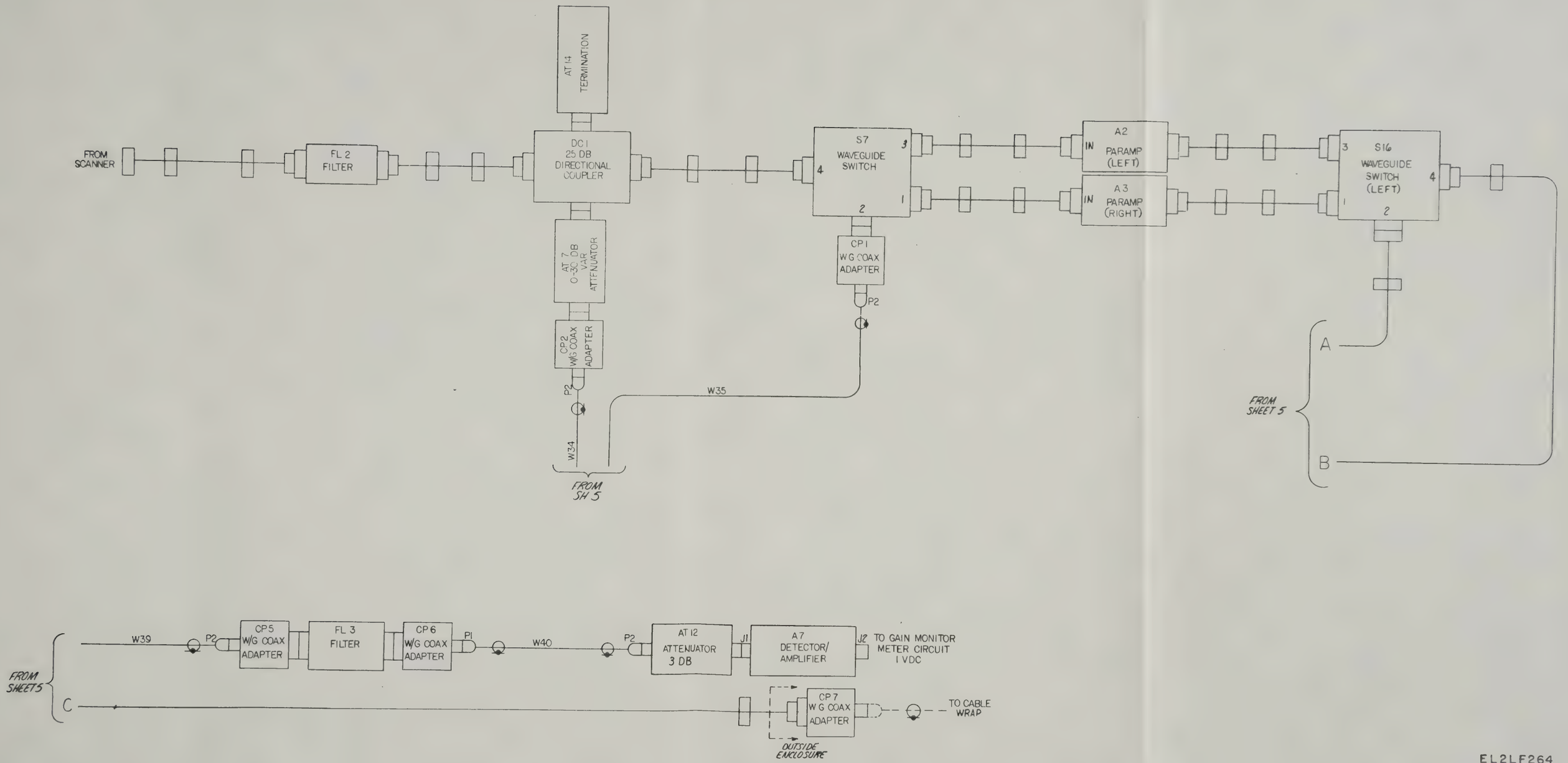
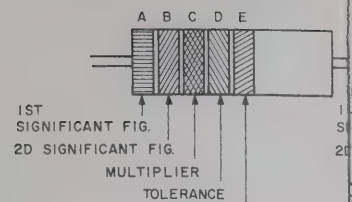


Figure FO 3-58. ⑥ Rf box, schematic diagram (sheet 6 of 6).

(ER)



USE WITH STYLES CM, CN, CY AND CB.

1ST SIG. FIG.	2D SIG FIG.	MULTIPLIER[1]	CAPACITANCE TOLERANCE				CHARACTERISTIC[2]			DC WORKING VOLTAGE	OPERATING TEMP. RANGE	VIBRATION GRADE
			CM	CN	CY	CB	CM	CN	CB	CM	CY, CM	CM
0	0	1			±20%	±20%		A			$-55°_{TO}+70°C$	10-55 Hz
	1	10					B	E	B			
2	2	100	±2%		±2%	±2%	C				$-55°_{TO}+85°C$	
	3	1,000		±30%			D		D	300		
4	4	10,000					E				$-55°_{TO}+125°C$	10-2,000Hz
5	5		±5%				F			500		
6	6										$-55°_{TO}+150°C$	
7	7											
8	8											
9	9											
		0.1			±5%	±5%						
		0.01	±10%	±10%	±10%	±10%						

COLOR CODE MARKING FOR COMPOS

COLOR CODE FO

BAND A		BAND B	
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECO SIGNIF FIGU
BLACK	0	BLACK	0
BROWN	1	BROWN	1
RED	2	RED	2
ORANGE	3	ORANGE	3
YELLOW	4	YELLOW	4
GREEN	5	GREEN	5
BLUE	6	BLUE	6
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7
GRAY	8	GRAY	8
WHITE	9	WHITE	9

BAND A — THE FIRST
(BANDS
BAND B — THE SECO
BAND C — THE MULT
TWO SIGN
NOMINAL
BAND D — THE RESI
BAND E — WHEN USE
ESTABLIS
PER 1,000
1-1/2 TIMES

RESISTAN

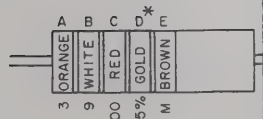
SOME RESISTORS ARE
DESIGNATORS. THE
FRACTIONAL VALUES

FOR WIRE-WOUND-T
FICATION MARKING I

PERATURE COMPENSATING, STYLE CC.

RATURE CIENT[4]	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
				CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
0	0	0	1		± 2.0 UUF	CC
-30	1	1	10	± 1%		
-80	2	2	100	± 2%	± 0.25 UUF	
-150	3	3	1,000			
-220	4	4				
-330	5	5		± 5 %	± 0.5 UUF	
-470	6	6				
-750	7	7				
	8	8	0.01*			
	9	9	0.1*	± 10%		
+100			0.1		± 1.0 UUF	
			0.01			

(ER)



NOMINAL RESISTANCE 3,900 OHM
RESISTANCE TOLERANCE ±5%
FAILURE RATE LEVEL M

COMPOSIT

* IF BAND D IS OMITTED, T

A. COLOR CODE

IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN
E IN UUF.

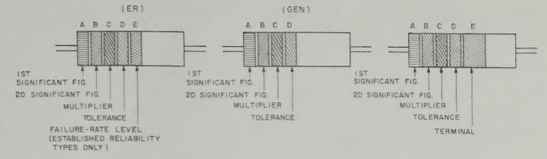
E THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS: MIL-C-5,
-C-11272B, AND MIL-C-10950C RESPECTIVELY.

TE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN

COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE.

G WHERE METALLIC PIGMENTS ARE UNDESIRABLE.

☆U.S. GOVERNMENT PRIN



COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS.

COLOR-CODE MARKING FOR FILM-TYPE RESISTORS.

TABLE I
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS.

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM.
BLACK	0	BLACK	0	BLACK	1			BROWN	M=1.0	
BROWN	1	BROWN	1	BROWN	10			RED	P=0.1	
RED	2	RED	2	RED	100			ORANGE	R=0.01	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S=0.001	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP. TYPE ONLY)	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY).			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE.

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE.

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS). ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL.

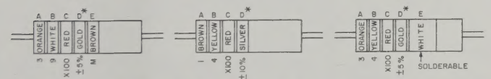
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODED.)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS 10R0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED. IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS.

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3,900 OHMS
RESISTANCE TOLERANCE ±5%
FAILURE RATE LEVEL M

NOMINAL RESISTANCE 1,400 OHMS
RESISTANCE TOLERANCE ±10%

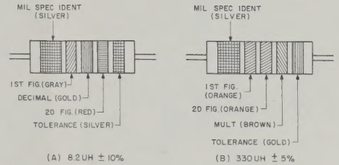
NOMINAL RESISTANCE 3,400 OHMS
RESISTANCE TOLERANCE ±5%
TERMINAL SOLDERABLE

COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD.

A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS.



(A) 8.2UH ± 10%

(B) 330UH ± 5%

COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES. AT A, AN EXAMPLE OF THE CODING FOR AN 8.2UH CHOKE IS GIVEN. AT B, THE COLOR BANDS FOR A 330 UH INDUCTOR ARE ILLUSTRATED.

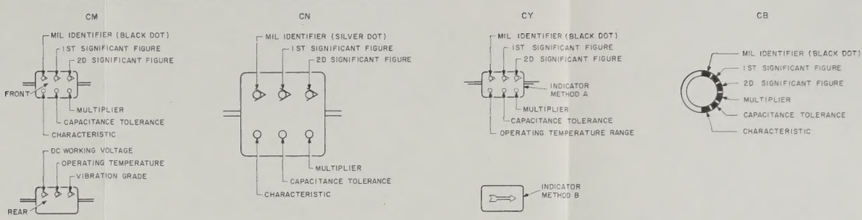
TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES.

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL.

B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS.

CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB.



MICA-DIELECTRIC

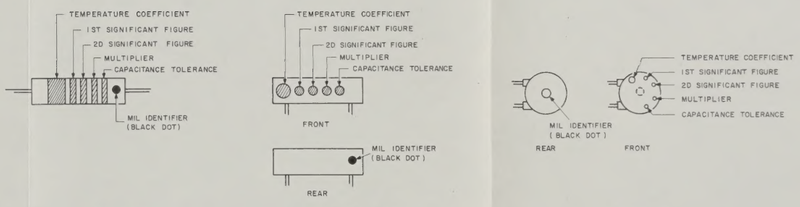
PAPER-DIELECTRIC

GLASS-DIELECTRIC, GLASS CASE

MICA, BUTTON TYPE

TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB.

COLOR	MIL ID	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER	CAPACITANCE TOLERANCE				CHARACTERISTIC				DC WORKING VOLTAGE	OPERATING TEMP. RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CB	CY	CM	CY, CM	CM
BLACK	CM,CY,CB	0	0	1			±20%	±20%		A				-55°C to +70°C	10-55 HZ
BROWN		1	1	10					B	E	B				
RED		2	2	100	±2%		±2%	±2%	C					-55°C to +85°C	
ORANGE		3	3	1,000	±30%				D		D	300			
YELLOW		4	4	10,000					E					-55°C to +125°C	10-2,000HZ
GREEN		5	5		±5%				F			500			
BLUE		6	6											-55°C to +50°C	
PURPLE (VIOLET)		7	7												
GRAY		8	8												
WHITE		9	9												
GOLD				0.1			±5%	±5%							
SILVER	CN			0.01	±10%	±10%	±10%	±10%							



AXIAL LEAD

RADIAL LEAD

DISK-TYPE

TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC.

COLOR	TEMPERATURE COEFFICIENT[3]	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	-30	1	1	10	±1%		
RED	-80	2	2	100	±2%	±0.25 UUF	
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5		±5%	±0.5 UUF	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GRAY		8	8	0.01*			
WHITE		9	9	0.1*	±10%		
GOLD	+100			0.1		±1.0 UUF	
SILVER				0.01			

1. THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.

2. LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS: MIL-C-5, MIL-C-25D, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY.

3. LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D.

4. TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE.

* OPTIONAL CODING WHERE METALLIC PIGMENTS ARE UNDESIRABLE.

C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS.

Figure FO 3-59. Color code markings for MIL-STD resistors, inductors and capacitors.

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